FAULT DIAGNOSIS OF ANALOG INTEGRATED CIRCUITS
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by

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Dedication

To our wives

Indrani,

Mausumi

and Gita

To our children

Priyasha,

Arpita,

Santanu and Sandipan
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Preface

The field of integrated circuit has undergone remarkable changes over the past decade. Integrated circuits incorporating both digital and analog function have become more and more popular in semiconductor industry. These combined circuits are called “Mixed Signal Circuits”. Fault diagnosis and testing of integrated circuit has grown into a special field of interest in semiconductor industry. The methodologies for testing of digital circuits are well established. However the methodologies for fault diagnosis of analog integrated circuits are relatively unexplored. Some of the reasons for this under development are lack of proper fault model of the devices operating in the continuous time domain, multiple value of the signal at each node of the circuit, etc.

This book, Fault Diagnosis of Analog Integrated Circuits, is primarily intended as a comprehensive text book at the graduate level, as well as a reference book for practicing engineers in the area of analog integrated circuit testing. Unlike other books, this book does not assume any solid background in analog circuits. A working knowledge of PSpice and MATLAB is necessary. An exposure to artificial neural network (ANN) is desirable.

The prime objective of the book is to provide insight into the different fault diagnosis techniques of analog integrated circuits.

The text is divided into five chapters. Chapter 1 presents an introduction to the basic concepts of fault diagnosis. Both simulation-after-test and simulation-before-test, have been discussed. Fault modelling is presented in Chapter 2. The choice of optimum test stimulus is the key to success in fault diagnosis. All classical and state of the art techniques of test stimulus generation have been discussed in Chapter 3. Chapter 4 presents a feasible
fault diagnosis methodology. The state of the art model based observer technique, is discussed in detail. The integrated circuit, particularly the operational amplifier is the most used building block of analog signal processing. This chapter presents a detailed overview of fault diagnosis of operational amplifiers (at the device or component level) using model based observer technique. Simulation results for the fault in bipolar and MOS operational amplifiers are given here. Besides, fault diagnosis of simple analog system-on-chip (SOC) is also presented. An experimental setup for fault detection and diagnosis in analog ICs and SOCs, is also presented in Chapter 4. Chapter 5 rounds off the text with Design-for-test (DfT) techniques and development of Built-in Self-test (BIST) facilities in analog ICs.

The problems at the end of the chapters 2, 3 and 4 may be assigned to the students for work out.

Three appendices present BJT spice parameter values of the µA 741 operational amplifier, MOSFET spice parameter values of the MOS operational amplifier and an introduction to artificial neural network (ANN).

Although an immense effort and attention to detail were exerted to prepare the manuscript, the book may still have some errors due to human nature. The authors welcome suggestions from the readers for improvement of the content and the presentation, for future incorporation.

We take this opportunity to express our appreciation to our numerous students and colleagues whose ideas and suggestions lead to this book. We would also like to acknowledge the support extended by our families; in particular we are grateful to our wives and children for tolerating many absences while we spent hours on this book.

February, 2005
Kharagpur

P. Kabisatpathy
A. Barua
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Chapter 1

INTRODUCTION

System-on-chip (SOC) technology has boosted the importance of analog circuitry, moving it into mainstream integrated circuit (IC) design. ICs with digital and analog circuits on the same substrate are now common [1]. Advances in deep sub-micron technologies have fuelled the explosive increase in IC complexity. The increasing functional complexity and smaller size of these chips makes testing a challenging task, particularly under the constraints of high quality and low price. Considering that testing represents a key cost factor in the production process (a proportion of up to 70% of total product cost is reported in [2]), an optimal test strategy can give substantial competitive edge in the market.

Electronic tests are system dependent and are classified as digital, analog and/or mixed-signal. Current methodologies for the testing of digital circuits are well developed. These include D-Algorithm [3], level sensitive scan design (LSSD) [4], IEEE Standard 1149.1 [5] and built-in logic block observer (BILBO) [6]. By contrast, methodologies for the testing of analog circuits remain relatively underdeveloped due to the complex nature of analog signals. Despite the translation of many analog electronic functions into their digital equivalents, there still exists a need to incorporate analog sections on many chips. In a primarily digital system, analog circuitry is still used to convert speech signals to digital signals, sensor signals are conditioned into microprocessors, digital bit streams are converted to radio frequency (RF) modulation patterns or horizontal scan lines on a computer graphics screen and microprocessors send control signals to actuators. Even with a pure digital system, there still exist power supplies, pull-up resistors to do level shifting and capacitors for electromagnetic compatibility (EMC). All these analog components on a digital system need to be tested during production and field service. In addition, “when digital clock rates get really high, the 0’s and 1’s don’t have real meaning anymore. The behaviour is essentially analog” [7]. Therefore, the importance of analog testing cannot
be underrated and there is a requirement to develop strategy, which will allow the analog and digital parts of the circuit to be tested simultaneously.

Analog and mixed-signal (AMS) ICs are gaining popularity in applications such as consumer electronics, biomedical equipments, wireless communication, networking, multimedia, automotive process control and real-time control systems. With such wide applications, AMS ICs will constitute the bulk of future electronic devices, making it imperative to research AMS testing, which include digital and analog testing. Compared to digital testing, analog testing lags far behind in both methodologies and tools and therefore demands substantial research and development effort. The objective of this book is to study testing and fault diagnosis of analog and/or the analog portion in AMS ICs. New analog test methodologies need to be compatible with existing digital test methods and be practical in compromising test coverage and test overhead.

1.1 Basic concepts

Historically, digital and analog testing techniques have developed at very different paces, causing analog test methodology to lag behind its digital counterpart. Computer-aided design (CAD) tools for automatic test generation and test circuitry insertion are available since two decades for digital circuits. The main reason for this is the ease of formulating the test generation as a mathematical problem due to the discrete signal and time values. The distinction between what does and what does not work is crisp and clear for digital circuitry. For analog, on the other hand, the question can better be stated as ‘how good’ the circuitry works. Does an analog-to-digital converter (ADC) work correctly, when it delivers a signal-to-noise ratio (SNR) of 69.99dB, when the specified minimum performance figure is 70dB? Does the system application suffer from this underperformance? For analog designs, the definition of fault-free and faulty circuits is much more a matter of specification thresholds and sensitivity of application than a sharp distinction as in the case of digital circuits.

For analog circuitry, generation of optimal test signals based on design topology is still not fully automated. As opposed to the digital approach based on the gate-level net-list, analog testing still relies mainly on a black-box approach, where the specifications of the circuitry are verified without paying attention to the structure or circuit layout. Another unresolved issue is the usage of standard design methods like the design-for-testability (DfT), to make the circuitry easily or better, testable. Scan chains are used in synchronous digital circuitry for this purpose. A comparable analog approach does not exist. Similarly, modelling of process defects and the use of these models for developing and improving test signals is already
standard practice for digital circuits whereas similar methods for analog circuitry are just beginning to be applied by some manufacturers. For some of these issues, alternative approaches are still in research phase. For some others, there are technically feasible alternatives but the existing production infrastructure and cost of changing present test methods is slowing down the acceptance of these methods.

For digital circuits, algorithms for the generation of test patterns based on gate-level net-list exist since as early as 1960’s [8][9]. Without the so-called automatic test pattern generation (ATPG) methods, it would have been impossible to produce the large digital ICs of the last twenty years at reasonable costs and quality. A similar test generation solution for analog testing became necessary with the increasing integration of analog and digital functionality on one chip. The analog test community has also been aiming at a solution comparable to that in digital, but the analog version of the problem is not solvable by similar analytical techniques. In the case of digital circuits, the discreteness in time and signal values, the well-defined fault propagation paths and topological boundaries of fault influence have simplified the problem to some extent when compared to the analog case. As a result, algorithms have been developed based on calculating the signal changes introduced by faults and logic rules to find input combinations to create changes between fault-free and faulty behaviour (path sensitisation) and propagate these changes to the primary outputs. A similar approach cannot be applied to analog circuits. The main reasons for this are:

1. There are not only two choices of analog signal values to choose from, but in principle, an infinite number of signal values are possible. The choice between two specific signal values can cause better or less good results related to observing the fault at the outputs.

2. The time variation properties of analog signals bring an extra dimension to the problem, since applying an AC, DC or transient test can be more or less efficient depending on the circuit and the targeted fault.

3. It is not possible to make a one-to-one link between the function and structure of analog circuitry such as in digital circuits. Given a particular topology, there is no general way of determining which part of the functionality is of interest and what the related performance limits are.

4. The propagation of fault effects to the output in analog circuits is not as simple as in the digital case, because of two reasons. First, the effect of a fault cannot be modelled to propagate in one direction, as is the case in digital. The fault effect propagates in all directions and the calculation of this propagation pattern becomes therefore much more complex than in the digital case. Secondly, in analog circuits,
the information that a fault is present at a certain node does not readily comprise the signal value information for that node, making time-consuming calculations of signal values necessary. Nonlinearity, loading between circuit blocks, presence of energy-storing components and parasitic elements further complicate these calculations.

The obstacles presented above have prevented analog net-list based (i.e., structural) test generation from being applied in practice. Unfortunately, a satisfying solution to the analog problem has not been found to this day. The research on this subject [10][11][12] has been going on for decades already, and the results are not good enough such that any analog block design can be made from a net-list description [13]. The alternative of solving the analog test generation problem based on these methods remains unfeasible for the time being and the application of net-list based test generation in practice requires a breakthrough in terms of the computational costs and general applicability. Today, specification based testing (checking whether the specifications are met) and functional testing (checking the functioning of the circuit with a standard input) are the dominating methods in analog testing.

Tests can be performed at several levels including wafer level, package level, module level, and system level or even in the field service level. A commonly mentioned rule of thumb test is the rule of ten which suggests that the cost of detecting a bad component in a manufactured part increases tenfold at each level [14]. Therefore, a fault should be detected as early as possible. Even though it is better to find a fault earlier, some later process changes may introduce additional failures. Therefore, an optimisation of testing effort or some compromise should be incorporated in the test procedures.

Tests can be classified into fault detection, fault location or fault prediction. In the manufacturing process or during maintenance, a quick check is needed to pass the good parts and reject the bad parts for maximum product throughput. So only fault detection is needed to evidence the faults. At other times, fault location is needed to detect failed modules or components for repair. Fault prediction is used mainly with highly reliable products or safety related products. Fault prediction continuously monitors the circuit under test (CUT) to identify whether any of its elements are about to fail allowing for a preventive repair. The choice between fault location and fault detection calls for a compromise. Fault location needs better isolation of the components and provides better test coverage. It may be used during both production and repair, but it may slow down the testing process and the throughput. The IEEE 1149.1 [5] standard provides decent fault isolation in digital circuits. For AMS circuits, the proposed IEEE P1149.4
standard [15] is still not widely used. In order to locate every fault, most nodes need to be accessed in the circuit, a requirement that may be impossible to meet in modern fabrication process.

The current approach to detect manufacturing faults in electronic circuits uses several forms of automatic test equipment (ATE), in-circuit tester (ICT) and functional tester. After assembly, the in-circuit testing is done to check for part orientation, part value, part type, and correct connections between all parts. Software models of each part are used to generate the test patterns used by the ICT. The main assumption is that in-circuit testers require physical access to nodes or points on the circuit in order to perform the necessary testing. A functional tester is usually customised to a particular product. The test is performed after packaging the product to check the functionality of the product. Due to the shrinkage in dimension of the electronic components and circuits, it is impossible to access every test point by an ATE. Therefore, alternative methods must be found to address these challenges. IEEE standard 1149.1 [5] and IEEE proposed standard P1149.4 [15] are such alternatives, which provide virtual probes.

\[ 	ext{FUNDAMENTAL TEST PROBLEMS} \]

- **INSUFFICIENT TESTING BANDWIDTH**
  - INSUFFICIENT SPEED OF TESTING
  - DECREASING CIRCUIT OBSERVABILITY
  - Tester Pin Electronics
  - Tester Architecture
  - Growing Die Size
  - Costly DFT Scheme

- **INADEQUATE TEST QUALITY**
  - INCOMPLETE TEST SET
  - SIMPLISTIC FAULT MODELS
  - Immature Test Generation Methodologies
  - High Complexity of Fault Simulation
  - Lack of Understanding of Fault Mechanism

\[ \text{Figure 1.1: The fundamental test problems and their causes [16].} \]

In Figure 1.1, an analysis of the fundamental problems in testing is depicted by Maly [16]. In this diagram, the two fundamental problems are identified as test bandwidth and test quality and specific challenges are pointed out for solving these problems. For mixed-signal testing specifically, other test hardware-related challenges such as noise level and accuracy of timing-measurements will have to be added to this picture. To summarise, the important issue here can be defined as developing the concept of a
frame linking analog and mixed-signal IC design and test environment. This framework must enable an IC development team to

- develop test programs in shorter time,
- debug test programs in shorter time,
- automatically generate test programs that will guarantee high IC quality.

1.2 Historical Background

Algorithms aimed at diagnosing component failures on printed circuit board (PCB) can be applied to identify faulty components in analog ICs. Given limited accessibility to internal nodes in analog ICs, a large number of algorithms and theoretical findings for fault diagnosis and test signal selection have been developed during the past three decades [17]. Duhamel and Rault [18], and Bandler and Salama [19] have presented two outstanding reviews of analog fault diagnosis. Duhamel and Rault [18] reviewed and assessed the techniques available before 1979 for automatic test generation of analog systems by classifying different methods and providing an extensive bibliography. Bandler and Salama [19] summarised various fault location techniques and algorithms developed before 1985 and added most algorithms developed after 1979. They discussed the fault dictionary approach, the parameter identification approach, the fault verification approach, and the approximation approach. Two excellent books have been published recently covering representative methodologies in analog fault diagnosis and modern approaches to mixed-signal testing [20][21].

The measures of testability and the degree of algorithm complexity are the basic theoretical topics for fault diagnosis. The testability studies tell whether a CUT is testable or not, for a given methodology, while the degree of complexity tells the effectiveness of the proposed algorithm. Both are related to the specific algorithms and the ways the test equations are formulated. Their effectiveness relates to the kind of faults being targeted. The testability measures can be defined in DC, frequency domain, and time domain.

Analog fault diagnosis methods are generally classified into simulation-after-test (SAT) and simulation-before-test (SBT) [18][19]. SAT methods focus on parameter identification and fault verification and they are very efficient for soft fault diagnosis because they are based on linear network models. However, the major problem in parameter identification is the ability to access test points. Very often, there are not enough test points to test all components or each added test point is too expensive to accept. As an alternative, the fault verification method addresses the problem with limited number of measurements, by which not all parameters of the circuit can be
identified at a time. The method assumes that only a few components are faulty and the rest of the network components are within design tolerances.

Checking the consistency of certain network equations identifies faulty components. The ability to test multiple faults is limited by large number of choices of faulty components, which result in combinatorial explosion for large design. The SAT approaches have the disadvantage of high on-line computational complexity, inability to deal with catastrophic faults, error proneness to component tolerances, and high numerical sensitivity. To compromise test coverage and test simulation, SBT methods emphasise on building a fault dictionary in which the nominal circuit behaviours in DC, frequency or time domain are stored. In the test stage, the measured circuit behaviour is compared with the nominal case and the faults are diagnosed. In manufacturing testing, a DC test is reliable and effective. However, when higher test coverage is needed, a frequency test or time domain test provides more information about the circuit under test without adding test nodes. In the following sections the SAT and SBT methods are discussed.

### 1.2.1 Simulation-after-test methods

Two most representative methods in SAT namely parameter identification and fault verification are discussed. The first task of parameter identification technique is to formulate sufficient number of independent equations from the measurements to determine all component values. A component value that lies outside the design tolerance range specification is identified as a faulty component.

Berkowitz [22] introduced the concept of network-element-value solvability by presenting the necessary conditions for passive networks in 1962. Even without an algorithm, Berkowitz’s studies heralded a new research area, analog fault diagnosis. Saeks et al. [23] proposed a method to determine parameter values using voltage and current measurements when a single excitation is applied. Multiple current excitations are applied to a network and voltage measurements are used to identify network parameters by Biernacki and Bandler [24]. Biernacki and Starzyk [25] gave test conditions, which are sufficient conditions for network solvability problems. Trick et al. [26] researched the necessary and sufficient test conditions for a single test frequency and introduced the adjoint circuit concept into fault diagnosis. In this study, the branch voltages of the unknown components should be available so that the component values can easily be found by a linear method. Navid and Willson [27] have given the necessary and sufficient conditions for the element-value solvability of a linear resistive network. They show that one can determine if it is possible to compute the element values from the test terminals by considering only the circuit
topology. Ozawa and Kajitani [28] studied the problem of diagnosability of linear active networks using a voltage and current graph. Starzyk et al. [29] used Coates graph and presented topological and graph-theoretic conditions to determine the required number of excitations and voltage measurements for evaluation of faulty elements within a sub network. Ozawa et al. [30] researched generalised Y-Δ transformation with a voltage controlled current source and its application to element-value solvability problems. The inaccessible nodes in a network are eliminated one by one by the transformation and a sequence of networks is obtained. They researched the backward process of Y-Δ transformation to determine the solvability problem. Visvanathan and Sangiovanni-Vincentelli [31] developed a theory for the diagnosability of non-linear circuits with DC inputs. They derived conditions for the local diagnosability and showed that for diagnosable systems, it is possible to obtain a finite number of test inputs that are sufficient to diagnose the system.

All the methods mentioned above deal with DC domain or single frequency excitation. The multi-frequency techniques include research on the test point selection and test frequency selection. Sen and Saeks [32] introduced a testability measure via multi-frequency measurements for linear systems and its applications to test point selection. Sen and Saeks [33], and Chen and Saeks [34] further discussed and refined this approach. Sen and Saeks’ measure is appealing because it provides a quantitative measure of testability and it leads to an efficient computational algorithm. Priester and Clary [35] proposed a testability measure based on optimal experiment designs borrowed from system identification theory. Their measure provides more information on the degree of difficulties about the testability. Rapisarda and Decarlo [36] proposed the tableau approach with multi-frequency excitation for analog fault diagnosis instead of transfer function oriented algorithms. Abderrahman et al. [37] used optimisation techniques to generate multi-frequency test sets for parametric and catastrophic failures. Sheu and Chang [38] proposed an efficient frequency domain relaxation pseudo-circuit approach and the associated solvability conditions with reduced dimension and practical implementation scheme.

The time domain approach includes formulating testable equations, which are solvable from time domain measurements. Saeks et al [39] published an excellent work on dynamic testing. They extended their diagnosability theory for linear systems [33] and memory-less non-linear systems [31] by presenting a necessary and sufficient condition for the local diagnosability of non-linear dynamical systems. Based on a discrete-time circuit description, Visvanathan and Sangiovanni-Vincentelli [40] derived a necessary and sufficient condition for the local diagnosability of a class of non-linear dynamical circuits whose branch relations are analytic functions.
of their argument. Dai and Souders [41] proposed an efficient approach for functional testing and parameter estimation of analog circuits in time domain based on a sensitivity matrix. Salama and Amer [42] developed a technique based on identifying the discrete time transfer function coefficients of the circuit under test from time domain response. Walker et al. [43] developed a two stage SAT fault diagnosis technique based on bias modulation. The first stage, which diagnoses and isolates faulty network nodes, resembles the node fault location method [44]. The second stage, a sub-network branch diagnosis extracts faulty network parameters. The branch diagnosis is achieved by element modulation, a technique to vary the value of the element externally as a modulated element.

Other studies on parametric identification methods include, parametric testing by artificial neural network processing of transient responses [45], parametric fault diagnosis using functional mapping [46], methods using wavelet transform of the response signal of the device under test and non-deterministic parametric fault model [47], the aggregation of the digitised output values for detecting parametric faults in linear time-invariant circuits [48].

The works discussed so far focussed on the parameter identification method. The fault verification methods use almost the same equations as are used in the parameter identification approaches, except that in the fault verification approaches, circuit components are partitioned into two classes, a fault-free class (class1) and a faulty class (class2). It is assumed that all components in class1 are fault-free and all faults are localised in class2. Using the measurement data and the nominal characteristics of all circuit components, test equations are formulated and expressed as functions of deviations of class2 components. Test equations are over determined and can be satisfied only if all faults are indeed localised in class2. This technique of making assumptions on faults and checking their validity is called fault verification.

Another quantitative testability measure, which is based on sensitivity was introduced by Temes [49] and was further studied by Dejka [50]. Skala et al. [51] studied a sensitivity algorithm for checking the consistency or inconsistency, of certain linear equations which are invariant on fault elements. Dai and Souders [41] proposed a testability measure using time domain sensitivity equations. Slamani and Kaminska [52] used sensitivity equations and optimisation method for selecting test sets.

From the topology point of view, Huang et al. [44] introduced k-node-fault testability in 1983. In their studies, node-voltages and nodal equations are used. The beauty of their testability condition is that it depends only on the graph of the circuit instead of the component values. Lin et al. [53] studied the topological conditions for single-branch- fault. Maeda et al. [54]
presented necessary and sufficient analytical as well as graph theoretic conditions for fault detectability and distinguishability in non-linear systems and used these conditions to derive an algorithm for fault diagnosis. Ozawa et al. [55], and Starzyk and Dai [56] presented a decomposition approach for testing large analog non-linear networks. This was found to be superior to conventional methods using sensitivity approach. Recent studies based on the k-fault diagnosis method deal with the problem of component tolerances using artificial backward propagation neural network [57][58]. Other prominent works reported are for unambiguous fault diagnosis based on ambiguity test algorithms [59][60][61][62], selection of minimal set of test nodes [63][64], parametric fault modelling [65] and parallel analog functional test [66].

No matter what kind of testability measures are used, whether it is based on frequency domain, time domain or topology, the advantage is that the measure tells whether the CUT is testable or diagnosable. However, the computational complexity is a difficult problem to overcome. In manufacturing testing, this problem becomes more severe. SBT methods provide a compromise by shifting the computational burden to simulation before test.

1.2.2 Simulation-before-test methods

Martens and Dyck [67] used a frequency domain approach for single element faults. They considered a transfer function as a bilinear function of network elements. Morgan and Towill [68] included the higher order harmonics in the dictionary for the frequency domain response of the network. Varghese et al. [69] utilised the Euclidian norm to normalise the network response deviations. Lin and Elcherif [70] considered DC inputs to build the fault dictionary. Seshu and Waxman [71] employed a frequency domain approach to construct a fault dictionary of a linear frequency-dependent circuit.

Time-domain analysis approaches were also studied to construct the fault dictionary. Macleod [72] used pseudo-random sequences as inputs for analog fault diagnosis. For each faulty condition, the deviation in the impulse response of the network is computed using a periodic pseudo-random sequence as excitation. These deviations are quantised and are stored in the dictionary. Schreiber [73] proposed the test signal design method to construct the fault dictionary. In this, the loci of all single-element drift failure fault signatures are drawn in the augmented signal space to generate the fault dictionary. Wang and Schreiber [74] utilised a complementary signal approach for go/no-go testing of a partitioned network under test. Balivada et al. [75][76] have studied the effects of various stimuli