# PHYSICAL DESIGN ESSENTIALS

## An ASIC Design Implementation Perspective

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# Dedication

***To my father, Aziz, my wife, Maury, my son, Troy and his family, Rebecca, his wife and their daughters Madison and Darya***

# Contents

# Preface

The goal of this book is to provide the essential steps required in the physical design of Application Specific Integrated Circuits (ASIC). It is the intention that the book present self-contained material and enough detail so as to give the reader a basic idea of ASIC design implementation.

The first generation of modern electronics is thought to have begun in 1942 with the invention of electronic switches and miniature vacuum tubes. By 1946, a large-scale computing device based on these new inventions was developed. The computing device was known as Electronic Numerical Integration and Calculation (ENIAC). ENIAC could perform thousands of calculations per second and was used in many applications such as scientific research and weather predictions.

With the introduction of the first working transistor in 1948, the second generation of the electronic era began. This era was mainly characterized by the change from vacuum tubes to transistor technology. Vacuum tubes were gradually replaced in the design of switching circuits by discrete transistors.

By 1965, the third generation of electronics began with the development of the Integrated Circuit (IC). The IC started to replace discrete transistor circuits. In addition, semiconductor memories, such the Read Only Memory (ROM) and Random Access Memory (RAM), began to augment the system designs. This resulted in the substantial reduction of the physical size and cost of the systems. This generation propelled the rapid integration of circuit design forms (small, medium, and large) to very large devices that contained millions of transistors.

These tremendous achievements were made possible by the development of IC processing equipment, design tools, and software. In the past fifteen years, the world not only has been witness to the rapid reduction in the feature size of transistors (from 1000 to 45 nanometer), but also to the dramatic innovation of sophisticated physical design automation tools.

The complexities of today's ASIC physical designs require a mix of backgrounds in electrical engineering, computer science, and IC processes. Such diversified knowledge has created a new discipline in engineering – the physical design engineer. Today's physical design engineers are expected to be conversant with all aspects of ASIC design implementation stages that include device processes, library development, place-and-route algorithms, verification and testing.

This book is arranged in a format that follows the industry-common ASIC physical design flow. It begins with the general concept of an ASIC library, then covers floorplanning, placement, routing, verification, and finally, testing. Topics covered include:

- Basic standard cell design, transistor sizing, and layout styles
- Linear, nonlinear, and polynomial characterization
- Physical design constraints and floorplanning styles
- Algorithms used for placement
- Clock Tree Synthesis
- Algorithms used for global and detailed routing
- Parasitic extraction
- Functional, timing, and physical methods of verification
- Functional, scan, parametric, memory and parallel module test

Rather than go into lengthy technical depths, the emphasis has been placed on short, clear descriptions complemented by references to authoritative manuscripts for those desiring further information on each chapter. It is the goal of this book to capture the essence of physical design, and to introduce to the reader the challenging and diversified field of physical design engineering.

Khosrow Golshan
Engineering Division Director, Conexant Systems, Inc.
December 2006

# Foreword

In the year 2006, the semiconductor industry is well into its sixth decade of existence. Amazingly, the original Bell Lab invention of the transistor combined a decade later with the refining implementation of an integrated circuit continues to drive exponential economic gain in the form of both improved productivity and growth of new applications. Today, an integrated circuit can perform almost any electronic function on a piece of silicon less than a centimeter square.

From a PC, to a cell phone, to a television, to an internet router, the industry can conceive, design and deliver that function in an extraordinarily cost-effective and convenient form a–single silicon IC. The result looks so deceivingly simple it can be, and is, taken for granted by an entire population.

However, for the industry and design community who must continue to deliver to this value proposition, none of it can be taken for granted. Fully appreciating the science, technology and, dare I say, art that must be mastered to implement an IC that contains tens of millions of individual transistors is a must for those who want to drive semiconductor industry success through the coming decades.

*Physical Design Essentials – An ASIC Design Implementation Perspective* by Khosrow Golshan is a resource that can be used by all industry participants to help develop just that appreciation.

For the student who is looking to develop a skill and expertise to participate in the industry the book provides exactly what the title suggests a– perspective. I would encourage the student to read the book to gain an understanding of the overall process that drives the physical design community. The student is likely to be studying in depth one of the areas touched on by the book. Whether that be circuit design and analysis, or CAD tool development, the context provided by the book will undoubtedly provide insight that will enhance the learning process.

For the designer who is directly contributing in one or more of the areas of design covered in the book, the book will become a valued reference, complementing and updating the many references with which the designer is already familiar. Mr. Golshan, in fact, has cited many of these well-used references in the chapters of this book and so not only does the work provide an updated perspective within the context of modern design complexity, it also ties many of these works together in a self consistent and clearly articulated framework.

The book is likely to prove most valuable, however, to the design manager. The book, while providing insight on the individual design steps is organized in a way to provide a complete framework through which the design process can be executed.

For the design manager it is essentially a handbook to determine whether a sufficient process for IC design is in place in their organization. More than that, the design manager can use the book to keep an “inventory” of the various skill sets and competencies that their design organization must keep current.

Finally, the book can and should be appreciated by, like me, the business manager within a semiconductor organization. For the business manager, the physical design process may not be focused on as the value added step. From the business managers perspective, value is often perceived to be created in differentiated technology, market selection or product definition. Once these steps have been completed the business manager, like the public, often takes the physical implementation for granted.

I would encourage, however, the business manager to at least peruse Mr. Golshan’s book and become familiar and appreciate the significant process that now forms physical design. This process must be fully understood and

carefully executed within the semiconductor business organization or all that supposed value added work that preceded "chip layout and verification" could be for naught.

Matt Rhodes
CEO, Teranetics, Inc.

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Khosrow Golshan

Chapter 1

# LIBRARIES

*"Good order is the foundation of all things." Edmund Burke*

Various types of data sets or libraries are required for the physical design of an Application Specific Integrated Circuit (ASIC). Libraries are collections of the physical layout, abstract views, timing models, simulation or functional models, and transistor level circuit descriptions.

As such, libraries are considered one of the most critical parts of the ASIC physical design, and the accuracy of these libraries and their associated views and models has a great impact on the success of the final fabricated ASIC design.

Standard cell libraries and Input-Output pads are typically used in ASIC design. In addition, memories and custom libraries may be used. Memories, such as Random Access Memory (RAM) or Read Only Memory (ROM) and their appropriate layout, abstract, timing and simulation views, are usually obtained from memory compilers.

Custom libraries, which are also referred to as Intellectual Property (IP) libraries, are collections of manually crafted analog function layouts such as Phase Lock Loop (PLL), Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), and Voltage Regulator (VR).

Because standard cells and Input-Out pads are the most basic building blocks of ASIC physical design, a general overview of the physical specification and timing generation of standard cells and Input-Out pads is

the focus of this chapter. The techniques that are outlined for standard cells can be extended to memory and IP physical design as well.

## 1.1 Standard Cells

A standard cell is a specific design for each gate in the library. Special care needs to be taken during the physical design of such libraries in order to obtain optimal ASIC die size and performance. With the advancements in the fabrication process and the increasing complexity of logic designs, the overall area of ASIC designs is becoming more dominated by the routing area rather than by the total area of transistors used. Therefore, it is necessary that the routing area be minimized rather than minimizing the area consumed by standard cells. Since the majority of ASIC routing is performed automatically, it is important to design standard cell sizes so that they are well-suited to the place-and-route tools being used.

The basic step in the physical design of standard cells begins with horizontal and vertical wire track determination. Wire tracks are used to guide place-and-route tools to perform interconnection between standard cells. Manufacturing guidelines such as width and spacing of the first two conducting layers (e.g. metal one and metal two) are used to set proper wire track spacing. Commonly, there are three ways to compute wire track spacing using center-to-center spacing – line-to-line ($d1$), Via-to-line ($d2$), and Via-to-Via ($d3$):

$$d1 = 1/2w + s + 1/2w \tag{1.1.1}$$

$$d2 = 1/2w + s + Via_{overlap} + 1/2Via_{size} \tag{1.1.2}$$

$$d3 = 1/2Via_{size} + Via_{overlap} + s + Via_{overlap} + 1/2Via_{size} \tag{1.1.3}$$

The relationship between these equations is

$$d3 > d2 > d1 . \tag{1.1.4}$$

In comparison, line-to-line is the most aggressive for conducting layer compaction. However, line-to-line center spacing will not optimize the overall routing as Via-to-Via and Via-to-line are not considered. Via-to-Via center spacing meets all line-to-line and Via-to-line center requirements, but the overall routing will not be optimum due to large spacing between the conducting layers.

In practice, Via-to-line has shown to be the most optimum. Via-to-line meets all conducting layers spacing rules and exhibits the most compact overall routing. An example of each wire track style is shown in Figure 1-1.

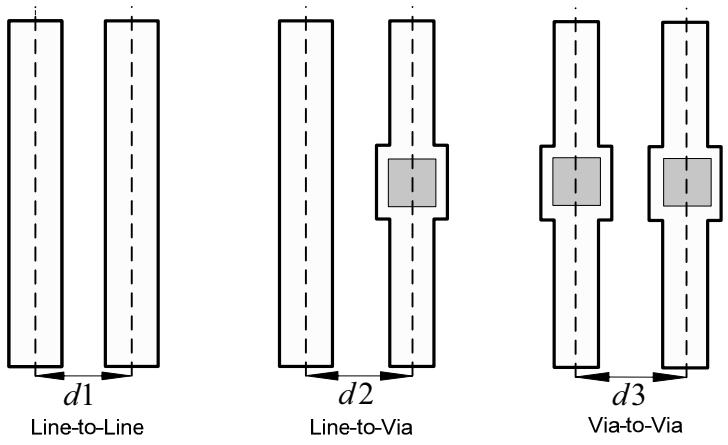


**Figure 1-1** Wire Track Center-to-Center Spacing

Most place-and-route tools require that the height and width of a standard cell be an integer multiple of the vertical and horizontal wire track. The height of the standard cell is the same throughout the library, but their widths vary according to their logical functions and drive strengths.

A typical standard cell for the Complementary Metal Oxide Semiconductor (CMOS) process is composed of a row of NMOS (N-type transistors) with

channel width $W_n$, and a row of PMOS (P-type transistors) with channel width $W_p$ separated by the distance of the P and N diffusion (or active) area.

The P and N diffusion area spacing, the channel width of PMOS and NMOS transistors, and the width of power (VDD) and ground (VSS) buses are the key parameters in determining the height of standard cells. Figure 1-2 shows a generalized standard cell height concept.

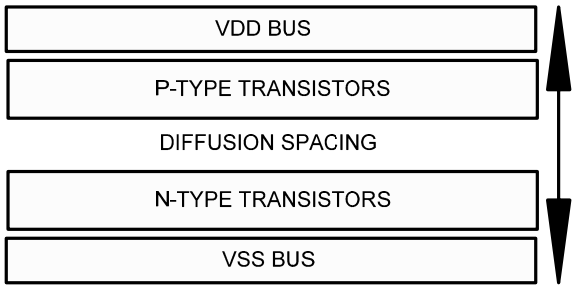


**Figure 1-2** Generalized Standard Cell Height

Once vertical and horizontal wire tracks, as well as the height of the standard cell is determined, this information is used to create a wire track template for use during standard cell layout.

Overlaying the wire track template on a standard cell layout during the physical design as a layout guideline insures that the actual physical layout of standard cells and their physical port locations will meet place-and-route tool routing requirements. Figure 1-3 shows a wire track mesh marked by Horizontal Wire Track and Vertical Wire Track.

As mentioned earlier, one of the key parameters in determining the standard cell height is the width of power and ground buses which traverse the top and bottom of the standard cells. If the power (VDD) and ground (VSS) bus layers are the same as the first horizontal routing layer, a limitation on standard cell heights is imposed. This is because the width of VDD and VSS buses has to be wide enough to provide proper current flow capability and this increase in the power and ground line width will affect the standard cell height.

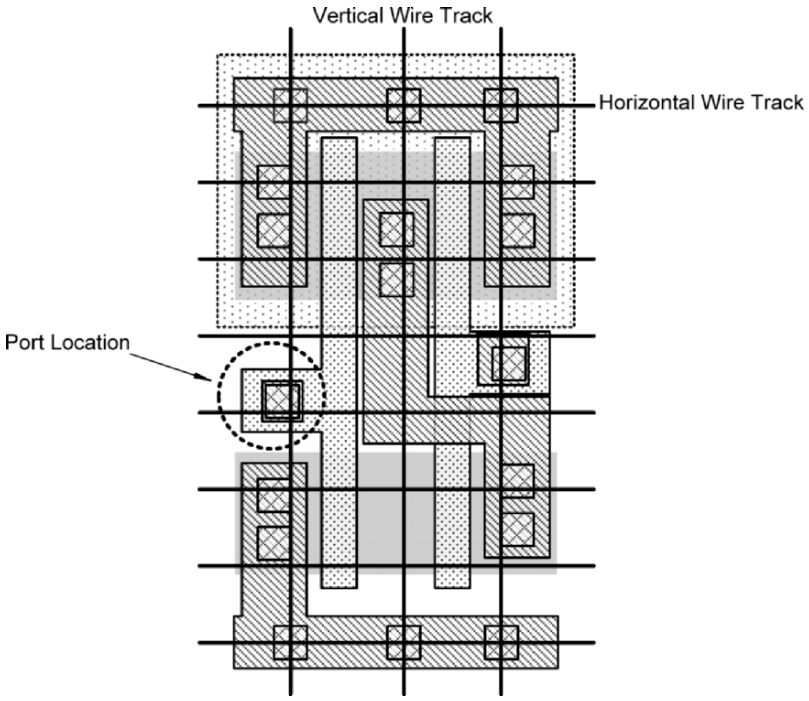


**Figure 1-3** Wire Track Mesh

For example, in an NWELL process, the power (VDD) bus must contact the NWELL and the ground (VSS) bus must contact the substrate. In addition, the VDD and VSS should be fully connected or strapped (i.e. using multiple contact cuts). The main advantage of fully strapped VDD and VSS buses to the NWELL and substrate is resistance reduction. This resistance reduction enhances standard cell immunity to internal latch-up phenomena. Because the power and ground minimum widths are dictated by the contact size and overlapping contact of the first conducting layer (e.g. *metal one*), the width of both VDD and VSS buses needs to be enlarged enough to avoid physical design rule violations.

With more metal layers available in today's silicon processes, using an alternate routing approach, such as first metal traverse vertically and second metal horizontally, would be advantageous in standard cell physical design. Using this method, the second layer can be used for power and ground

routing over internal standard cell transistors. This technique may provide much better results with respect to area, performance, and power consumption for multimillion gate ASIC designs that require significant amounts of routing resources for power to prevent voltage drop across the chip. To handle a variety of power requirements, the standard cell power and ground buses can vary in widths depending on power requirements without modifying the standard cell heights.

In standard cell layout, it is preferable to use the first conducting layer, such as metal one, as much as possible to make internal connections of NMOS and PMOS transistors within standard. If there is a need to use other conducting layers, such as metal two, use of such layers must be kept to a minimum. This greatly influences the ASIC top level routing. In addition, all internal node capacitance need to be kept at a minimum with the most capacitive nodes close to the VDD and VSS buses in order to reduce body effect impact. The body effect is a dynamic problem that changes the transistor (MOSFET) threshold voltage when the source to well (or body) bias changes.

Another key factor in standard cell physical layout is the location of input and output ports. It is desired to use the first routing (e.g. metal one) layer for standard cell ports, or pins, and place them where the horizontal and vertical wire tracks cross as shown in Figure 1-3. This allows the place-and-route tools to access the ports from both X and Y directions. This is known as port accessibility; it improves execution time during the routing step and produces better quality routing with respect to the overall physical design rule violations.

During standard cell library development, establishing geometrical regularity among the layout of all the standard cells of the same type has two advantages. First, it allows the use of compaction software in order to further reduce the area of standard cells while enabling migration of the standard cell library to another process node (e.g. migrating standard cell library from one design rules to another one) with ease. Secondly, and most importantly, establishing geometrical regularity leads to common electrical characteristics between the standard cells. This electrical uniformity will be useful when dealing with one of the most common limitations and challenges in physical cell design. In addition, it plays an important role in deciding the largest PMOS and NMOS transistor channel widths within the library.

Once channel width and ratio of the PMOS and the NMOS transistors is determined, the standard cell layout can be designed by using a single column of NMOS and PMOS transistors aligned at common connection distances by active area. It is desirable to layout all simple transistors as unbroken columns.

The polysilicon gates need to be ordered to allow maximum connection between them by sharing the source and drain area to form transistors. It is electrically advantageous to place the NMOS transistors as close as possible to the VSS bus and PMOS transistors to the VDD bus.

In connecting the source and drain of transistors to the VDD and VSS buses, single contact cut should be minimized. Minimizing single contact cut and using multiple source and drain contact cut connections will reduce source-drain resistance and enhance electrical performance of the standard cell.

For the logical gates that consist of transistors in series, such as AND logic, the smallest transistor should be placed close to the output, and the size of transistors needs to be increased as they approach the ground (VSS) or power (VDD) supplies. This will improve the overall performance [1], but it has an area penalty.

In the case of complex cells, such as flip-flop or Boolean functions, polysilicon connections can be used for non-critical signals. It is extremely important to avoid PWELL or NWELL routing. There are two main problems with PWELL or NWELL routing – the material is highly resistive, and often its parasitic such as resistance cannot be extracted. This influences the gate characterization accuracy in comparison to the actual silicon.

The current submicron CMOS process is very complex in nature. In addition, it is very difficult to visualize all the mask levels and manufacturing design rules that are used during actual fabrication of an ASIC design. However, in designing standard cell layouts for the CMOS process, a minimal set of design rules shown in Figure 1-4, are adequate. The reason for this minimal set is that most of today's standard cell are using up to *metal two* in their designs, however, using higher layer such a *metal three* can create a routing obstruction that could lead to local routing congestion during routing.

In the early days of standard cell development, the area of the standard cell was of more concern, thus the physical design objective was to design the standard cell to be as small as possible. This was mainly dominated by the fact the polysilicon feature (two micrometer line width) was larger than the metallization line width. Electrical parameters, such as power and noise, were not an important factor and they did not have a large impact on overall design performance.

Minimum width of a nwell
Minimum space between two nwell of the same potential
Minimum area of nwell

Minimum width of diffusion to define NMOS/PMOS width
Minimum width of diffusion for interconnect
Minimum space between diffusion regions

Minimum overlap of nwell over P+ region inside nwell
Minimum clearance from nwell to P+ region outside nwell
Minimum area of diffusion

Minimum width of a poly for channel length of MOS transistor
Minimum width of a poly for interconnect
Minimum clearance from diffusion to poly on field oxide
Minimum space between two poly on field oxide area
Minimum poly extend into field oxide (end-cap)
Minimum poly area

Contact size
Contact spacing
Minimum space of contact on diffusion to poly
Minimum space of contact on poly to diffusion

Maximum width of metal1
Minimum extension of metal1 over contact
Minimum metal1 space
Minimum metal1 area

**Figure 1-4** Minimum Design Rule Set

With today's advanced processes, where the polysilicon line width is becoming very narrow, the overall ASIC chip area is dominated by the level of metallization. Hence, performance is impacted by noise injection and power consumption. It is important to make sure that the channel width of PMOS and NMOS transistors is large enough to account for power dissipation, overall noise immunity, and their ratio is set properly to provide optimum performance. Therefore, one should note that the style of standard cell layout involves optimizing the transistors with respect to noise immunity, power dissipation, and performance, rather than optimizing the transistors to achieve a smaller area.

Another consideration in the physical design of standard cells is the size of the output stage transistors that determine the drive capability of the external capacitive loads. Each gate type needs to have multiple drive strengths. These drive strengths must be uniform across all gate types and need to increase monotonically with the output capacitance.

For process nodes with gate lengths of 130nm and below, classical mask generation for patterning the critical dimensions, such as polysilicon gate and first conducting layer (e.g. metal one), can no longer produce correct results. This is mainly because during wafer printing of very narrow width geometries, the incident light sources will interfere with each other and will cause incorrect exposure. Figure 1-5 shows the basic concept of such a wafer printing problem.

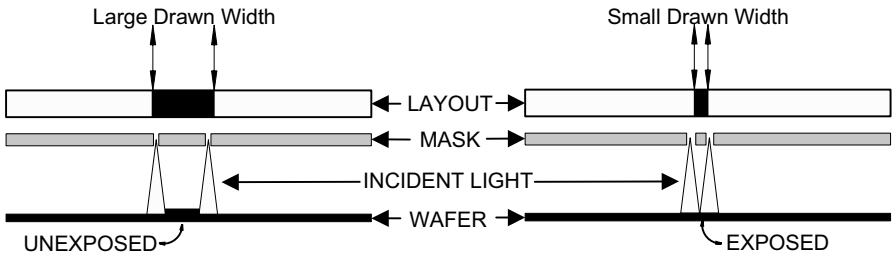


**Figure 1-5** Illustration of Problematic Wafer Printing

In order to solve deep submicron wafer printing problems, many of today's semiconductor foundries are utilizing a new way of generating masks called