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Philips, K., van Roermund, A.H.M.

CALIBRATION TECHNIQUES IN NYQUIST A/D CONVERTERS
van der Ploeg, H., Nauta, B.

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Fayed, A., Ismail, M.

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HIGH-SPEED PHOTODIODES IN STANDARD CMOS TECHNOLOGY
Radovanovic, Sasa, Annema, Anne-Johan, Nauta, Bram
Design of High Voltage xDSL Line Drivers in Standard CMOS

By

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KU Leuven, Belgium

and

MICHEIL STEYAERT
KU Leuven, Belgium
Today, the worldwide DSL market penetration has surpassed all other forms of broadband access technologies. However, still less than 5% of the world’s phone lines are connected to DSL networks. At over 173 million DSL subscribers, as of September 2006, the majority of the world remains thus “unconnected”. The opportunity of DSL is to reuse the billions of available twisted pairs of the classical plain old telephone service (POTS) to offer a triple play of high-speed Internet, voice over IP (VOIP) and multichannel television to your home.

The Discrete MultiTone (DMT) modulation was developed to provide bit-rates close to the Shannon limit for the lossy transmission medium. In this modulation technique, the used bandwidth is divided into several carriers, spaced at 4.3125 kHz. Each carrier is modulated by a quadrature amplitude modulation. A large disadvantage of this technique is the high Crest Factor (CF) of the signals in the time domain, requiring linear amplifiers for a broad range of input signal amplitudes. This results in line drivers with very low efficiencies.

It is known that the Self-Oscillating Power Amplifier (SOPA) is a highly efficient line driver for xDSL applications. However, in the nano-electronic era, the line driver remains more than ever the major bottleneck for lowering the cost and power of the xDSL modem. The low supply voltages coming from nanometer technologies increase the current density in the line driver for a constant output power. This results in a low efficiency and reliability problems.

To solve these low voltage issues, high voltage design techniques are discussed in this book using the principle of stacking standard nanometer devices. Two realisations are analysed to demonstrate the feasibility of this principle. A first high voltage driver is implemented in a standard 2.5 V 0.25 µm CMOS technology. Although the supply voltage of the high voltage driver is set at three times the nominal supply voltage, none of the transistors in the circuit is stressed by applying too large voltages, resulting in reliable operation and guaranteed minimum lifetime of operation described by the foundry.
An output swing of 6.46 V at a frequency of 10 MHz is measured over a 50 Ω load. With the second high voltage driver, the boundaries of the stacking principle are even further explored. The chip is implemented in a standard 1.2 V 130 nm CMOS technology. With five stacked transistors and a supply voltage of 5.5 V an output swing of 4.2 V at a frequency of 40 MHz is measured over a 4 Ω load with an efficiency of 79%.

To prove the usefulness of this stacking principle, a high voltage driver is integrated in the SOPA architecture, which leads to a fully integrated high voltage line driver. Again, two test chips were developed in a standard 1.2 V 130 nm CMOS technology to materialize this concept. The first, zeroth order, SOPA complies with the aDSL-Lite specification with its 1.1 MHz bandwidth and 42 dB Missing Tone Power Ratio (MTPR). The efficiency is 40%. The second, first order, SOPA faces the two challenges of line drivers in wireline communications: increasing the signal’s bandwidth while maintaining a high efficiency. The circuit complies with the aDSL2+ specifications. A MTPR of 58 dB is reached for a DMT signal with a CF of 15 dB. The efficiency for driving a 100 mW aDSL2+ signal is 42%.

Heverlee
August 2007

Bert Serneels
Michiel Steyaert
## List of Abbreviations and Symbols

### Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>aDSL</td>
<td>Asymmetric Digital Subscriber Loop</td>
</tr>
<tr>
<td>AFE</td>
<td>Analog Front-End</td>
</tr>
<tr>
<td>AM</td>
<td>Amplitude Modulation</td>
</tr>
<tr>
<td>AMI</td>
<td>Alternate-Mark Inversion</td>
</tr>
<tr>
<td>AWG</td>
<td>American Wire Gauge</td>
</tr>
<tr>
<td>BER</td>
<td>Bit-Error Rate</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer Aided Design</td>
</tr>
<tr>
<td>CF</td>
<td>Crest Factor</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal-Oxide-Semiconductor</td>
</tr>
<tr>
<td>CO</td>
<td>Central Office</td>
</tr>
<tr>
<td>CPE</td>
<td>Customer Premises Equipment</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>DFE</td>
<td>Digital Front-End</td>
</tr>
<tr>
<td>DIDF</td>
<td>Dual Input Describing Function</td>
</tr>
<tr>
<td>DMT</td>
<td>Discrete MultiTone modulation</td>
</tr>
<tr>
<td>DSL</td>
<td>Digital Subscriber Line</td>
</tr>
<tr>
<td>DSP</td>
<td>Digital Signal Processing</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>FEXT</td>
<td>Far-End Crosstalk</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
</tr>
<tr>
<td>G-Lite</td>
<td>less performing ADSL-Lite</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain Bandwidth</td>
</tr>
<tr>
<td>HCD</td>
<td>Hot Carrier Degradation</td>
</tr>
<tr>
<td>HD₂</td>
<td>Second-order Harmonic Distortion Term</td>
</tr>
<tr>
<td>HD₃</td>
<td>Third-order Harmonic Distortion Term</td>
</tr>
<tr>
<td>HDSL</td>
<td>High-speed Digital Subscriber Line</td>
</tr>
<tr>
<td>HDTV</td>
<td>High Definition Television</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>HPF</td>
<td>High-Pass Filtering</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuits</td>
</tr>
<tr>
<td>IM\textsubscript{2}</td>
<td>Second-order Intermodulation Distortion Product</td>
</tr>
<tr>
<td>IM\textsubscript{3}</td>
<td>Third-order Intermodulation Distortion Product</td>
</tr>
<tr>
<td>IP\textsubscript{3}</td>
<td>Third-order Intercept Point</td>
</tr>
<tr>
<td>ISDN</td>
<td>Integrated Service Digital Network</td>
</tr>
<tr>
<td>ISP</td>
<td>Internet Service Provider</td>
</tr>
<tr>
<td>ITU-T</td>
<td>International Telecommunications Union - Telecommunications standardization sector of ITU</td>
</tr>
<tr>
<td>ITRS</td>
<td>International Technology Roadmap for Semiconductors</td>
</tr>
<tr>
<td>LD</td>
<td>Line Driver</td>
</tr>
<tr>
<td>LDDMOS</td>
<td>Laterally Double Diffused MOS</td>
</tr>
<tr>
<td>LDMOS</td>
<td>Laterally Diffused MOS</td>
</tr>
<tr>
<td>LPF</td>
<td>Low-Pass Filtering</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-Insulator-Metal</td>
</tr>
<tr>
<td>MOSFET</td>
<td>MOS Field Effect Transistor</td>
</tr>
<tr>
<td>MTPR</td>
<td>Missing Tone Power Ratio</td>
</tr>
<tr>
<td>NEBS</td>
<td>Network Exploitation Board Specifications</td>
</tr>
<tr>
<td>NEXT</td>
<td>Near-End Crosstalk</td>
</tr>
<tr>
<td>NOS</td>
<td>Non-Overlapping Switching</td>
</tr>
<tr>
<td>ONU</td>
<td>Optical Network Unit</td>
</tr>
<tr>
<td>OSR</td>
<td>Over Switching Ratio</td>
</tr>
<tr>
<td>PAR</td>
<td>Peak-to-Average-Ratio</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PON</td>
<td>Passive Optical Network</td>
</tr>
<tr>
<td>POTS</td>
<td>Plain Old Telephone Service</td>
</tr>
<tr>
<td>PSD</td>
<td>Power Spectral Density</td>
</tr>
<tr>
<td>PSTN</td>
<td>Public Switched Telephone Network</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
</tr>
<tr>
<td>QAM</td>
<td>Quadrature Amplitude Modulation</td>
</tr>
<tr>
<td>RF</td>
<td>Radio-Frequency</td>
</tr>
<tr>
<td>rms</td>
<td>root mean square</td>
</tr>
<tr>
<td>Rx</td>
<td>Receive</td>
</tr>
<tr>
<td>SHDSL</td>
<td>Symmetric HDSL</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious Free Dynamic Range</td>
</tr>
<tr>
<td>SLIC</td>
<td>Subscriber Line Interface Circuit</td>
</tr>
<tr>
<td>SINAD</td>
<td>Signal-to-Noise and Distortion Ratio</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon On Insulator</td>
</tr>
<tr>
<td>SOPA</td>
<td>Self-Oscillating Power Amplifier</td>
</tr>
<tr>
<td>TDDB</td>
<td>Time-Dependent Dielectric Breakdown</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>TSIDF</td>
<td>Two Sinusoid Describing Function</td>
</tr>
<tr>
<td>Tx</td>
<td>Transmit</td>
</tr>
<tr>
<td>VDMOS</td>
<td>Vertical integrated Diffused MOS</td>
</tr>
</tbody>
</table>
vDSL Very high-speed Digital Subscriber Loop
VGA Variable Gain Amplifier
VLSI Very Large-Scale Integration
VOIP Voice-over IP
xDSL Digital Subscriber Loop

Symbols

\( _2F_1(a, b; c; z) \) The 2-1 hyper-geometric function in the variable \( z \) with factors \( (a, b) \) and \( (c) \) [-]
\( \alpha \) Coupling factor between two coupled SOPAs [-]
\( \alpha(\omega) \) Gain term of the complex propagation constant [-]
\( A \) Limit cycle amplitude [V]
\( (a)_n \) The Pochhammer symbol, a notation for \( \Gamma(x+n)/\Gamma(x) \) [-]
\( \beta(\omega) \) Phase term of the complex propagation constant [-]
\( C_{\text{gate}} \) Gate capacitance of a MOSFET [F]
\( C_{\text{int}} \) Integrator capacitance [F]
\( C_{\text{in}} \) Input capacitance [F]
\( C_{\text{j}} \) Junction capacitance of a diode [F]
\( C_{\text{ox}} \) Oxide capacitance of a MOSFET [F]
\( C_{\text{well}} \) Well-capacitance [F]
\( d \) Cable length [km]
\( dx \) Unit length [-]
\( e \) Euler’s number 2.72 [-]
\( f_{\text{fil}} \) Cut-off frequency of a loop filter [Hz]
\( f_{\text{int}} \) Unit-gain frequency of an integrator [Hz]
\( f_{\text{lc}} \) Limit cycle frequency [Hz]
\( \gamma(\omega) \) Complex propagation constant [-]
\( g_{\text{m}} \) Transconductance of a MOSFET [S]
\( I \) \( \sqrt{-1} \) [-]
\( I_{\text{q}} \) Quiescent current [A]
\( I_{\text{DS}} \) Drain-source current [A]
\( I_{\text{rms}} \) Rms current [A]
\( \Im(z) \) The imaginary part of the complex number \( z \) [-]
\( J_n(x) \) Besselfunction of the first kind and order \( n \) [-]
\( k \) Boltzmann constant \( 1.3807 \cdot 10^{-23} \) [J/K]
\( k_R \) Material-dependent factor for calculating the skin-effect [-]
\( L \) Length of a MOS transistor [\( \mu \)m]
\( L(s) \) Transfer function of a linear loop filter [-]
\( L_{\text{min}} \) Minimal gate length of a specified CMOS technology [\( \mu \)m]
\( \eta \) Total power efficiency of a power amplifier [-] or [%]
\( N \) Number of tones in a DMT signal [-]
List of Abbreviations and Symbols

$n$ Voltage multiplication factor [-]
Number of stacked transistors [-]

$N_A(A)$ The single input describing function of a non-linearity
with one sinusoidal input with amplitude $A$ [-]

$N_B(A, B)$ The dual input describing function for a non-linearity
with two sinusoidal inputs with amplitudes $A$ and $B$,

describing the gain of the signal with amplitude $B$ [-]

$O(\phi)$ The Landau symbol also called big-O, which denotes that
there exists a positive value $A$ so that if $f = O(\phi)$,

$$|f| < A\phi [-]$$

$P_{out}$ Output power [W] or [dBm]

$R_L$ Load resistance [$\Omega$]

$R_S$ Switch resistance [$\Omega$]

$R_{on}$ On-resistance of a MOSFET [$\Omega$]

$\Re(z)$ The real part of the complex number $z$ [-]

$\sigma_n^2$ Noise energy [dBm]

$s$ Laplace variable $s = \frac{1}{2\pi f}$ [1/s]

$\Gamma(x)$ Gamma function [-]

$t_{d0}$ Delay time of a unit inverter [s]

$\mu$ Mobility $[\text{cm}^2/\text{Vs}]$

$V_{BD}$ Junction breakdown voltage [V]

$V_T$ MOS threshold voltage [V]

$V_{DD}$ Nominal supply voltage [V]

$V_{DS}$ Drain-source voltage [V]

$V_{GB}$ Gate-bulk voltage [V]

$V_{GD}$ Gate-drain voltage [V]

$V_{GS}$ Gate-source voltage [V]

$\omega$ Pulsation [rad/s]

$W$ Width of a MOS transistor [$\mu$m]

$x$ Scaling factor of an inverter chain [-]

$y$ Transformer ratio [-]

$Z_0$ Characteristic line impedance [$\Omega$]
Contents

Preface ........................................................ V

List of Abbreviations and Symbols ............................. VII

1 Introduction ................................................... 1
  1.1 Motivation of the Work ................................. 3
  1.1.1 xDSL Technologies: The Market Opportunities .... 4
  1.1.2 xDSL Technologies: The Gap ....................... 4
  1.1.3 Power or High Voltage in Nanometer CMOS? ....... 5
  1.2 Organisation of the Book ............................... 7

2 Digital Subscriber Line: Signals, Specifications
and Driver Solutions ......................................... 11
  2.1 DSL in a Nutshell ....................................... 12
   2.1.1 History .......................................... 12
   2.1.2 How it Works ..................................... 13
   2.1.3 Continuing Developments in DSL ................. 14
  2.2 The Channel ............................................ 16
   2.2.1 Cable Technology ................................ 16
   2.2.2 Twisted Pair Cable Modeling ..................... 17
   2.2.3 Cable Impairments ............................... 20
  2.3 Modulation Techniques .................................. 21
   2.3.1 The Shannon Limit ................................ 21
   2.3.2 DMT Modulation ................................ 21
   2.3.3 DMT Specifications ............................. 24
  2.4 Solutions for xDSL Line Drivers ...................... 26
   2.4.1 Line Driver Requirements ......................... 26
   2.4.2 Class AB .......................................... 27
   2.4.3 Class G/H ........................................ 29
   2.4.4 Class D .......................................... 31
   2.4.5 Class K and Other Combined Structures .......... 33
  2.5 Conclusions ............................................. 34
# Contents

3 **The SOPA xDSL Line Driver** .............................................. 37
   3.1 The Describing Function Analysis Method .......................... 37
      3.1.1 Nonlinear Systems ............................................. 37
      3.1.2 The Describing Function Viewpoint ......................... 38
   3.2 Behavior Model of the SOPA ........................................ 40
      3.2.1 Reference Model ............................................... 40
      3.2.2 Limit Cycle Oscillation ..................................... 42
      3.2.3 The Coupled System .......................................... 43
      3.2.4 The Forced System .......................................... 46
      3.2.5 Higher Order SOPA Amplifiers ............................... 54
   3.3 High Voltage SOPA Amplifiers ..................................... 55
   3.4 Conclusions .......................................................... 59

4 **High Voltage Design Considerations** .................................. 61
   4.1 CMOS Scaling .................................................................. 62
      4.1.1 Introduction: Moore’s Law ................................. 62
      4.1.2 CMOS Scaling Laws .............................................. 62
      4.1.3 Influence of CMOS Scaling on Switching Amplifiers ... 64
      4.1.4 Influence of CMOS Scaling on SOPA Design .............. 67
      4.1.5 Reliability Issues .............................................. 70
      4.1.6 Customized Silicon Technologies ......................... 75
   4.2 Stacking Devices: The High Voltage CMOS Solution ............. 77
      4.2.1 Introduction ....................................................... 77
      4.2.2 Power Dissipation ............................................... 80
   4.3 Conclusions .......................................................... 90

5 **High Voltage Implementations in Standard CMOS** .................... 91
   5.1 A 7.5 V Output Driver in a 2.5 V 0.25 μm CMOS Technology . 91
      5.1.1 Introduction ....................................................... 91
      5.1.2 Building Block Design ....................................... 92
      5.1.3 Layout Aspects .................................................... 111
      5.1.4 Power Dissipation .............................................. 116
      5.1.5 Measurements .................................................... 116
      5.1.6 Discussion of the Results .................................... 119
   5.2 A 5.5 V Output Driver in a 1.2 V 130 nm CMOS Technology . 122
      5.2.1 Introduction ....................................................... 122
      5.2.2 Building Block Design ....................................... 123
      5.2.3 Layout Aspects .................................................... 141
      5.2.4 Power Dissipation .............................................. 143
      5.2.5 Measurements .................................................... 144
      5.2.6 Discussion of the Results .................................... 146
   5.3 Conclusions .......................................................... 148
<table>
<thead>
<tr>
<th>6. High Voltage Line Driver Realisations</th>
<th>149</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1 A Zeroth-Order SOPA in 130 nm CMOS</td>
<td>149</td>
</tr>
<tr>
<td>6.1.1 Introduction</td>
<td>149</td>
</tr>
<tr>
<td>6.1.2 Building Block Design</td>
<td>151</td>
</tr>
<tr>
<td>6.1.3 Layout Aspects</td>
<td>152</td>
</tr>
<tr>
<td>6.1.4 Measurements</td>
<td>156</td>
</tr>
<tr>
<td>6.1.5 Discussion of the Results</td>
<td>159</td>
</tr>
<tr>
<td>6.2 A First-Order SOPA in 130 nm CMOS</td>
<td>160</td>
</tr>
<tr>
<td>6.2.1 Introduction</td>
<td>160</td>
</tr>
<tr>
<td>6.2.2 Building Block Design</td>
<td>160</td>
</tr>
<tr>
<td>6.2.3 Layout Aspects</td>
<td>164</td>
</tr>
<tr>
<td>6.2.4 Measurements</td>
<td>166</td>
</tr>
<tr>
<td>6.2.5 Discussion of the Results</td>
<td>169</td>
</tr>
<tr>
<td>6.3 Conclusions</td>
<td>172</td>
</tr>
<tr>
<td>7. Conclusions</td>
<td>175</td>
</tr>
<tr>
<td>7.1 Main Contributions and Achievements</td>
<td>175</td>
</tr>
<tr>
<td>References</td>
<td>179</td>
</tr>
<tr>
<td>Index</td>
<td>183</td>
</tr>
</tbody>
</table>
Introduction

In 1874, while Alexander Graham Bell (who considered himself to be a teacher of the deaf, more than the inventor of the telephone) was working on the harmonic telegraph, the telephone and hearing aids for the deaf, he built a device called phonoautograph. The device was made with Frankensteinian ingenuity out of a dead man’s ear (It is not recorded just where the ear came from, volunteered or otherwise.). Speaking into the device caused the ear to operate . . . like an ear. The ear’s membrane vibrated according to the intensity of the voice, more for louder voices or sounds, less for quieter sounds or whispers. This in turn caused a lever attached to the ear to “write” a wave pattern on smoked glass; bigger waves for louder sounds and smaller for quieter sounds. This inspired Bell. He thought that, by using a membrane to convert sounds of varying intensity into electrical current of varying intensity (instead of just the working of the lever) and then reversing the process on the other end with another membrane, he could replicate speech over long distances. It took him two years to put this idea into practice, but it became the founding principle of telephony.

Once the variable current is generated, it has to have some way to travel to the receiving end, where it is converted back to sounds. From the beginning, copper wire has been the carrier of choice. But, how many wires are needed? The first phones did just use one wire, carrying both the transmitter’s and receiver’s current and grounding each end in the earth to complete the circuit. However, this created a lot of static interference, since everyone was using the earth to ground their phones. This was fixed when Bell invented a two-wire circuit in 1881. It meant that a phone conversation would require two wires creating a complete circuit, where grounding in the earth was not needed. The two-wire circuit is considered as the start of the billions of twisted pairs for the Plain Old Telephone Service (POTS) that are laying in the ground at this moment.

The history of data-transmission began thus with Alexander Graham Bell, a pioneer who developed the idea that data could be transmitted through
copper wire. Of course, he had no idea of the scope of his findings or where they would actually lead to. However, the principles had been established.

In the course of history, many people improved the telephone. The invention of the microphone by David Hughes, with further improvements by Thomas Edison who introduced the carbon granule transmitter, made the telephone into an instrument that was much more sensitive than Bell’s Aluminium alloy diaphragm. By the early 1960s, low-cost transistors and associated circuit components made the introduction of touch-tone into home telephones possible. Extensive human factors tests determined the position of the buttons to limit errors and increase dialing speed even further.

Also in the 1960s, the telephone system gradually began converting its internal connections to a packet-based, digital switching system, whereas the earlier phone systems were purely analog causing great inefficiency. It was very prone to breakdown and noise and did not lend itself well to long distance connections. Today, most voice switching in the world is digital with the exclusion of the final connection from the local Central Office (CO) to the Customer Premises Equipment (CPE). This final connection is an analog POTS line, also called The Last Mile.

From the 1950s on, people started experimenting sending digital data over the copper wires. However, while the theoretical capacity of copper to transmit data was long known, mathematician Claude Shannon presented in 1948 its theory of channel-information capacity, the practical use of telephone wires for high-speed data was first demonstrated in the late 1980s. Joseph Lechleider demonstrated, through mathematical analysis, the feasibility of sending broadband. The first efforts, to make use of this capacity, created Integrated Service Digital Network (ISDN). The ISDN vision was very ambitious: to construct a global network for data communications and telephony.

In 1986 the early concept definition of High-speed Digital Subscriber Line (HDSL) started. Digital Subscriber Line (DSL) technology was originally implemented as part of the ISDN specifications. Under the impulse of Joseph Lechleider, asymmetry, between up- and downstream data-rates, was introduced in the DSL spectrum, representing the $a$ in aDSL. He understood that many users would benefit from the higher data rates possible in one direction.

In the early years of DSL, the economic benefit was not present. However, the .com boom of the mid-1990s created a viable market for DSL. Nowadays, multiple standards for DSL are emerging, grouped under the term xDSL. The reason is the ever-increasing demand for more bandwidth. Latest developed standards, such as aDSL2+ and vDSL2, have the opportunity to offer a triple play of high-speed Internet, Voice-over IP (VOIP) and High Definition Television (HDTV). As such, DSL can preserve its market position between cable and Passive Optical Network (PON) in the field of last mile access solutions.

Figure 1.1 shows a timeline with some interesting aspects of wireline communications from the invention of the telephone to the latest DSL standards.
1.1 Motivation of the Work

Today, the worldwide DSL market penetration has surpassed all other forms of broadband last mile access technologies combined. The resulting xDSL standards and the prospects of the vDSL2 system have proven the expectations for millions of broadband users. The implementations of these techniques had, however, a big drawback from a power consumption point of view, certainly at the CO side. Its line drivers, the final building block between the modem and the telephone line, consume an enormous amount of power.

A typical CO modem architecture for xDSL is shown in Figure 1.2 [Sto06]. Coding and modulation is done in the digital interface by digital signal processing. The analog part of the Transmit (Tx) channel contains a Digital-to-Analog Converter (DAC), Low-Pass Filtering (LPF) and a Line Driver (LD). The function of the hybrid is to separate the strong transmitted signals from the weak received signals and thus prevent saturation of the Receive (Rx) path. In the Rx channel High-Pass Filtering (HPF) is used to reduce the out-of-band signals such as the echo from the transmit signal. A Variable Gain Amplifier (VGA) is used in order to ensure that the Rx signal optimally fits into the input of the Analog-to-Digital Converter (ADC). This converter is preceded by an anti-alias filter. With the advent of the nano-electronic era, the line driver remains more than ever the bottleneck for lowering cost and power of the Analog Front-End (AFE).

The presented research activities are aimed at improving this building block, to design aDSL/aDSL2+ compliant line drivers with a high voltage output buffer in a low voltage mainstream Complementary Metal-Oxide-Semiconductor (CMOS) technology and at the same time, maximize its efficiency. In this chapter the importance of this work will be motivated and an overview of the contents of this book is given to guide the reader through this work.

Fig. 1.1. Timeline of telephone wireline communications
1.1.1 xDSL Technologies: The Market Opportunities

DSL’s subscriber base went up to more than 173 million, while global broadband subscribers reached more than 263 million in the 12 months to 30 September 2006. Each week, 1.25 million people signed up to broadband according to the latest statistics prepared for the international DSL Forum by industry analyst Point Topic. Two-thirds of new subscribers are choosing DSL technology, that delivers broadband over telephone lines. [source: www.dslforum.org]

DSL is by far the most popular broadband access technology in the world at 65.6% market share, rising to 82% in the European Union, the world’s largest broadband region. Of the remaining broadband access technologies, cable and fiber-to-the-home deliver respectively 23% and 10% of the world’s broadband subscribers. Less than 1% of broadband is delivered by satellite, accounting for less than one million subscribers. However, there are still large opportunities for DSL since less than 5% of the phone lines are connected to DSL networks. The majority of the world remains thus “unconnected”. DSL reuses the billions of available twisted pairs of the classical POTS. Today vDSL2 with a bandwidth of 30 MHz can offer 100 Mbit symmetrical data rate and enables real triple play. In this point of view, DSL is complying to the need-for-speed on the web for the millions of broadband users.

1.1.2 xDSL Technologies: The Gap

The reuse of the billions of copper wires in the ground for last mile access is a good choice from a market point of view. However, the implementation of those xDSL systems has brought engineers and analog designers a lot of worries. The transmission line characteristics of the twisted pair telephone wires are far from good at higher frequencies. Therefore, specialized modulation techniques
1.1 Motivation of the Work

Table 1.1. Overview of the most important driver architectures in relation to the maximum number of lines per 500 cm$^2$ board

<table>
<thead>
<tr>
<th>Lines per 500 cm$^2$ board</th>
<th>24</th>
<th>48</th>
<th>72</th>
<th>96</th>
<th>120</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class AB 740 mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Class G 400 mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>∆Σ Class D 200 mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOPA 100 mW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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are necessary to reach high bandwidths in Asymmetric Digital Subscriber Loop (aDSL). aDSL signals have a noise-like look with several voltage peaks. This large Crest Factor (CF), meaning the ratio between the maximum voltage and the root mean square (rms) signal voltage, render traditional class AB power amplifiers to be low efficient line drivers.

The importance of high efficiency can be easily observed by taking a look at the Network Exploitation Board Specifications (NEBS) norms. The NEBS prescribe the maximal amount of power that can be dissipated on a 500 cm$^2$ modem board. If the efficiency of the line drivers is taken into account, the power dissipation will fix the maximum number of lines that can be served by a single board. The result of these calculations is depicted in Table 1.1 [Sev02]. The cost per served line thus increases with decreasing efficiencies of the line drivers. The modem-board density is, nowadays, not only limited by the number and size of the components, but also by thermal limitations.

If a complete modem-board is split in an AFE, Digital Front-End (DFE) and a line driver, one can say that, when scaling the technology to a next node, the power dissipation for the DFE and AFE decreases with roughly 50% and 30% respectively. However, the power savings in the line driver is only a few percent. Today, the line driver represents about 80% of the total power dissipation per served line. The goal is to design highly efficient line drivers such that the cost per line can be lowered. Table 1.1 shows also that traditional architectures do not suffice. Therefore, the presented research activities are based on a relatively novel, highly efficient architecture for xDSL line drivers: the Self-Oscillating Power Amplifier (SOPA) [Pie04].

1.1.3 Power or High Voltage in Nanometer CMOS?

An important research topic of this work is high voltage design in mainstream nanometer CMOS for designing analog power building blocks. The nanometer technologies provide an answer to the increasing integration density of Very Large Scale Integration (VLSI) circuits and the low power requirements of
complex signaling processing applications. For mass-production, the integration of the power amplifier within the digital part of the system could lead to a lower production cost and smaller products [Rey05].

A major issue when integrating power amplifiers in CMOS technologies is the fact that for nanometer technologies, the supply voltage drops to nearly 1 V or even below 1 V. This is done to limit the electric field across the transistor’s channel, such that the foundry reliability targets are met. However, the output power is coupled with the square of the maximum voltage swing by \( P = V^2/R_L \), and the output swing is of course limited by the supply voltage. Another problem is that the load impedance \( R_L \) is fixed by physical constraints, which are very difficult to change. For instance, the characteristic impedance of free space, also called the \( Z_0 \) of free space, is an expression of the relationship between the electric-field and magnetic-field intensities. The \( Z_0 \) of free space is, like the characteristic impedance in general, expressed in ohms. It is considered as a physical constant and its exact value is \( 120\pi \, \Omega \).

Therefore, the load impedance needs to be converted or transformed into a lower value for achieving a constant output power. This is typically done by an impedance matching network, resulting in extra power losses. On the one hand, these are losses in the impedance network itself. On the other hand, these are losses due to the large current densities in the amplifier driving a low ohmic resistance. After all, when driving high currents, small parasitic resistors can lower the overall efficiency drastically. Moreover, reliability becomes an issue, since electro-migration effects can occur at these current densities. For an xDSL system, the impedance transformation is performed by the line transformer, which is depicted in Figure 1.3.

New power amplifier architectures, such as the SOPA, addresses these issues up to some point, but when entering in the nano-electronic era more has to be done. A 1 V supply is too low for designing an xDSL CO modem. The transformer ratio of the impedance matching network becomes too large such that it becomes impossible to meet the noise specifications of an xDSL system. Moreover, the received signal in the modem will be attenuated with this ratio, resulting in Signal-to-Noise Ratio (SNR) specifications for the building blocks in the Rx path (Figure 1.2) that appeals to one’s imagination. The low voltage issues can be elevated by going to higher voltages. This can be done in three ways:

Fig. 1.3. Schematic of the line transformer as an impedance matching network
1. By using a separate high voltage output stage comprised of power transistors. This is a very costly solution, since this requires extra costly components on the line card.

2. By using a technology that is able to deal with higher voltages, like DMOS or BiCMOS technologies. These technologies can be integrated in a low cost CMOS process at, of course, a higher cost. After all, this integration requires extra process steps and mask sets. When scaling towards nanometer lengths, the price of these mask sets is increasing exponentially.

3. By using drain source engineering and circuit techniques in a standard CMOS technology. This technique ensures that the devices never encounter a voltage as high as the breakdown voltage over their gate capacitance, while the output swing is higher than this value.

These solutions are ordered from an easy implementation to a very difficult one, but also from a high cost to a low cost implementation. It is only the third and last solution that results in a fully integrated, low cost modem for xDSL applications. Therefore, an important part of the research in this book is dedicated to high voltage circuit design in a mainstream, low voltage nanometer CMOS technology.

These high voltage techniques can also be used for other (low power) applications when using (sub) 1 V CMOS technologies. After all, such low supply voltages put serious restrictions on the design of analog circuits, such as limited gain and SNR.

### 1.2 Organisation of the Book

The presented work aims for a high efficiency, high voltage line driver in a mainstream nanometer CMOS technology. It is a contribution to a fully integrated low cost, high efficiency AFE for xDSL CO modems.

Chapter 2 starts with an investigation of the required specifications for an xDSL line driver. Since these requirements are a direct consequence of the used channel, a short overview of the channel properties is given. From that, it will become clear why Discrete MultiTone modulation (DMT) is used as the modulation technique. The DMT signals pose severe requirements on the line drivers. A brief overview of the most important reported architectures is given. The conclusion of this overview is that a self-oscillating switching structure is necessary for a high efficient xDSL line driver.

The high voltage techniques developed in this work are applied on the output stage of the SOPA architecture for it is the most efficient line driver for xDSL applications. Therefore, a summary of the behavioral model of the SOPA is given in Chapter 3. The SOPA is characterized by the limit cycle oscillation. Techniques to calculate its amplitude and frequency are discussed. The limit cycle oscillation will act as a natural dither in the non-linear system. Formulas are derived to calculate the possible distortion and Missing Tone