Charge-based MOS Transistor Modeling

The EKV model for low-power and RF IC design

Christian C. Enz
Eric A. Vittoz
Charge-based MOS Transistor Modeling
To our families

Dominique, Adrien, Mathilde and Simon
and
Monique, Nathalie and Didier
Contents

Foreword xiii
Preface xv
List of Symbols xvii

1 Introduction 1
1.1 The Importance of Device Modeling for IC Design 1
1.2 A Short History of the EKV MOS Transistor Model 2
1.3 The Book Structure 5

Part I The Basic Long-Channel Intrinsic Charge-Based Model 7

2 Definitions 9
2.1 The N-channel Transistor Structure 9
2.2 Definition of Charges, Current, Potential, and Electric Fields 10
2.3 Transistor Symbol and P-channel Transistor 11

3 The Basic Charge Model 13
3.1 Poisson’s Equation and Gradual Channel Approximation 13
3.2 Surface Potential as a Function of Gate Voltage 17
3.3 Gate Capacitance 18
3.4 Charge Sheet Approximation 20
3.5 Density of Mobile Inverted Charge 21
  3.5.1 Mobile Charge as a Function of Gate Voltage and Surface Potential 21
  3.5.2 Mobile Charge as a Function of Channel Voltage and Surface Potential 23
3.6 Charge-Potential Linearization 23
  3.6.1 Linearization of $Q_i(\Psi_s)$ 23
  3.6.2 Linearized Bulk Depletion Charge $Q_b$ 26
  3.6.3 Strong Inversion Approximation 27
  3.6.4 Evaluation of the Slope Factor 29
  3.6.5 Compact Model Parameters 32
CONTENTS

4 Static Drain Current 33
  4.1 Drain Current Expression 33
  4.2 Forward and Reverse Current Components 35
  4.3 Modes of Operation 36
  4.4 Model of Drain Current Based on Charge Linearization 37
    4.4.1 Expression Valid for All Levels of Inversion 37
    4.4.2 Compact Model Parameters 39
    4.4.3 Inversion Coefficient 40
    4.4.4 Approximation of the Drain Current in Strong Inversion 41
    4.4.5 Approximation of the Drain Current in Weak Inversion 43
    4.4.6 Alternative Continuous Models 45
  4.5 Fundamental Property: Validity and Application 46
    4.5.1 Generalization of Drain Current Expression 46
    4.5.2 Domain of Validity 46
    4.5.3 Causes of Degradation 48
    4.5.4 Concept of Pseudo-Resistor 49
  4.6 Channel Length Modulation 50
    4.6.1 Effective Channel Length 50
    4.6.2 Weak Inversion 52
    4.6.3 Strong Inversion 52
    4.6.4 Geometrical Effects 53

5 The Small-Signal Model 55
  5.1 The Static Small-Signal Model 55
    5.1.1 Transconductances 55
    5.1.2 Residual Output Conductance in Saturation 60
    5.1.3 Equivalent Circuit 61
    5.1.4 The Normalized Transconductance to Drain Current Ratio 62
  5.2 A General NQS Small-Signal Model 65
  5.3 The QS Dynamic Small-Signal Model 72
    5.3.1 Intrinsic Capacitances 72
    5.3.2 Transcapacitances 74
    5.3.3 Complete QS Circuit 75
    5.3.4 Domains of Validity of the Different Models 77

6 The Noise Model 81
  6.1 Noise Calculation Methods 81
    6.1.1 General Expression 81
    6.1.2 Long-Channel Simplification 86
  6.2 Low-Frequency Channel Thermal Noise 87
    6.2.1 Drain Current Thermal Noise PSD 87
    6.2.2 Thermal Noise Excess Factor Definitions 89
    6.2.3 Circuit Examples 91
  6.3 Flicker Noise 96
    6.3.1 Carrier Number Fluctuations (Mc Worther Model) 96
    6.3.2 Mobility Fluctuations (Hooge Model) 101
    6.3.3 Additional Contributions Due to the Source and Drain Access Resistances 103
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.3.4</td>
<td>Total 1/f Noise at the Drain</td>
<td>104</td>
</tr>
<tr>
<td>6.3.5</td>
<td>Scaling Properties</td>
<td>105</td>
</tr>
<tr>
<td>6.4</td>
<td>Appendices</td>
<td>106</td>
</tr>
<tr>
<td></td>
<td>Appendix: The Nyquist and Bode Theorems</td>
<td>106</td>
</tr>
<tr>
<td></td>
<td>Appendix: General Noise Expression</td>
<td>108</td>
</tr>
<tr>
<td>7</td>
<td>Temperature Effects and Matching</td>
<td>111</td>
</tr>
<tr>
<td>7.1</td>
<td>Introduction</td>
<td>111</td>
</tr>
<tr>
<td>7.2</td>
<td>Temperature Effects</td>
<td>112</td>
</tr>
<tr>
<td>7.2.1</td>
<td>Variation of Basic Physical Parameters</td>
<td>112</td>
</tr>
<tr>
<td>7.2.2</td>
<td>Variation of the Voltage–Charge Characteristics</td>
<td>116</td>
</tr>
<tr>
<td>7.2.3</td>
<td>Variation of the Voltage–Current Characteristics</td>
<td>118</td>
</tr>
<tr>
<td>7.2.4</td>
<td>Variation of the Current–Charge Characteristics</td>
<td>120</td>
</tr>
<tr>
<td>7.3</td>
<td>Matching</td>
<td>120</td>
</tr>
<tr>
<td>7.3.1</td>
<td>Introduction</td>
<td>120</td>
</tr>
<tr>
<td>7.3.2</td>
<td>Deterministic Mismatch</td>
<td>121</td>
</tr>
<tr>
<td>7.3.3</td>
<td>Random Mismatch</td>
<td>125</td>
</tr>
<tr>
<td>8</td>
<td>Nonideal Effects Related to the Vertical Dimension</td>
<td>133</td>
</tr>
<tr>
<td>8.1</td>
<td>Introduction</td>
<td>133</td>
</tr>
<tr>
<td>8.2</td>
<td>Mobility Reduction Due to the Vertical Field</td>
<td>133</td>
</tr>
<tr>
<td>8.3</td>
<td>Nonuniform Vertical Doping</td>
<td>138</td>
</tr>
<tr>
<td>8.3.1</td>
<td>Introduction and General Case</td>
<td>138</td>
</tr>
<tr>
<td>8.3.2</td>
<td>Constant Gradient Doping Profile</td>
<td>139</td>
</tr>
<tr>
<td>8.3.3</td>
<td>Step Profile</td>
<td>141</td>
</tr>
<tr>
<td>8.3.4</td>
<td>Effect on the Basic Model</td>
<td>147</td>
</tr>
<tr>
<td>8.4</td>
<td>Polysilicon Depletion</td>
<td>148</td>
</tr>
<tr>
<td>8.4.1</td>
<td>Definition of the Effect</td>
<td>148</td>
</tr>
<tr>
<td>8.4.2</td>
<td>Effect on the Mobile Inverted Charge</td>
<td>149</td>
</tr>
<tr>
<td>8.4.3</td>
<td>Slope Factors and Pinch-Off Surface Potential</td>
<td>150</td>
</tr>
<tr>
<td>8.4.4</td>
<td>Voltage Slope Factor $n_v$</td>
<td>152</td>
</tr>
<tr>
<td>8.4.5</td>
<td>Charge Slope Factor $n_q$</td>
<td>153</td>
</tr>
<tr>
<td>8.4.6</td>
<td>Effect on $Q_i(V)$, Currents, and Transconductances</td>
<td>154</td>
</tr>
<tr>
<td>8.4.7</td>
<td>Strong Inversion Approximation</td>
<td>155</td>
</tr>
<tr>
<td>8.5</td>
<td>Band Gap Widening</td>
<td>156</td>
</tr>
<tr>
<td>8.5.1</td>
<td>Introduction</td>
<td>156</td>
</tr>
<tr>
<td>8.5.2</td>
<td>Extension of the General Charge–Voltage Expression</td>
<td>158</td>
</tr>
<tr>
<td>8.5.3</td>
<td>Extension of the General Current–Voltage Expression</td>
<td>160</td>
</tr>
<tr>
<td>8.6</td>
<td>Gate Leakage Current</td>
<td>161</td>
</tr>
<tr>
<td>9</td>
<td>Short-Channel Effects</td>
<td>167</td>
</tr>
<tr>
<td>9.1</td>
<td>Velocity Saturation</td>
<td>167</td>
</tr>
<tr>
<td>9.1.1</td>
<td>Velocity-Field Models</td>
<td>169</td>
</tr>
<tr>
<td>9.1.2</td>
<td>Effect of VS on the Drain Current</td>
<td>171</td>
</tr>
<tr>
<td>9.1.3</td>
<td>Effect of VS on the Transconductances</td>
<td>181</td>
</tr>
</tbody>
</table>
CONTENTS

9.2 Channel Length Modulation 186
9.3 Drain Induced Barrier Lowering 189
  9.3.1 Introduction 189
  9.3.2 Evaluation of the Surface Potential 189
  9.3.3 Effect on the Drain Current 194
  9.3.4 Effect on Small-Signal Parameters in Weak Inversion 196
9.4 Short-Channel Thermal Noise Model 197
  9.4.1 Thermal Noise Drain Conductance 198
  9.4.2 Effect of VS and Carrier Heating on Thermal Noise 205
  9.4.3 Effects of Vertical Field Mobility Reduction and Channel
       Length Modulation 209
  9.4.4 Summary 211

10 The Extrinsic Model 213
  10.1 Extrinsic Part of the Device 213
  10.2 Access Resistances 215
    10.2.1 Source and Drain Resistances 215
    10.2.2 The Gate Resistance 217
  10.3 Overlap Regions 220
    10.3.1 Overlap Capacitances 220
    10.3.2 Overlap Gate Leakage Current 223
  10.4 Source and Drain Junctions 223
    10.4.1 Source and Drain Diodes Large-Signal Model 223
    10.4.2 Source and Drain Junction Capacitances 224
    10.4.3 Source and Drain Junction Conductances 226
  10.5 Extrinsic Noise Sources 226

Part III The High-Frequency Model 229

11 Equivalent Circuit at RF 231
  11.1 RF MOS Transistor Structure and Layout 231
  11.2 What Changes at RF? 231
  11.3 Transistor Figures of Merit 232
    11.3.1 Transit Frequency 232
    11.3.2 Maximum Frequency of Oscillation \( f_{\text{max}} \) 236
    11.3.3 Minimum Noise Figure 238
    11.3.4 Moderate and Weak Inversion for RF Circuits 239
  11.4 Equivalent Circuit at RF 240
    11.4.1 Equivalent Circuit at RF 240
    11.4.2 Intradevice Substrate Coupling and Substrate Resistive
       Networks 242
    11.4.3 Practical Implementation Issues 247

12 The Small-Signal Model at RF 249
  12.1 The Equivalent Small-Signal Circuit at RF 249
  12.2 Y-Parameters Analysis 251
  12.3 The Large-Signal Model at RF 257
CONTENTS

13 The Noise Model at RF  261
    13.1 The HF Noise Parameters  261
        13.1.1 The Noisy Two-Port  261
        13.1.2 The Correlation Admittance  263
        13.1.3 The Noise Factor  265
        13.1.4 Minimum Noise Factor  266
    13.2 The High-Frequency Thermal Noise Model  267
        13.2.1 Generalized High-Frequency Noise Model  268
        13.2.2 The Two-Transistor Approach at High Frequency  269
        13.2.3 Generic PSDs Derivation  272
        13.2.4 First-Order Approximation  273
        13.2.5 Higher Order Effects  279
    13.3 HF Noise Parameters of a Common-Source Amplifier  282
        13.3.1 Simple Equivalent Circuit Including Induced Gate Noise and Drain Noise  282
        13.3.2 Equivalent Circuit Including Induced Gate Noise, Drain Noise, Gate and Substrate Resistances Noise  288

References  291

Index  299
Foreword

Modern electronic technology is largely based on MOS integrated circuits containing both analog and digital parts. In designing such circuits with high performance, a correct MOS transistor model is a must. The designer needs a model he or she can rely on, which correctly describes the numerous physical phenomena in MOS transistors, allowing the performance of a circuit composed of such devices to be predicted with accuracy during circuit simulation. In addition, for preliminary “hand” analysis and design, it is desirable to have a simple model that makes evident the inter-relations between the various parameters, and allows the designer to correctly identify the trade-offs involved. The EKV approach to MOS transistor modeling combines both of these attributes.

The EKV model is the result of a large body of work by Drs C. C. Enz, F. Krummenachcer, and E. A. Vittoz, and several of their students and colleagues. The work has its origins in the pioneering work at CEH (now CSEM), on micropower devices and circuits for watches in the late sixties. This has given the EKV model development a unique aspect: it originated with highly competent circuit designers, notably analog ones, and was developed by them, or at least with constant feedback from them, every step of the way. Thus, it not only describes the physics of the MOS transistor, but takes into account carefully what circuit designers need. The result is a model that is accurate and predictive, correctly treats the MOSFET as a four-terminal, nominally symmetric device, has smooth behavior without discontinuities in all regions of operation, and correctly predicts small-signal parameters. In addition, the basic part of the model consists of a simple set of equations that are intuitively appealing, which makes it possible for the circuit designer to have a feel for the model and its parameters, rather than treating the model simply as a black box in which no designer dares to tread. This helps make circuit design a systematic process, and less a cut-and-try approach.

Drs. Enz and Vittoz, well-known for their contributions to MOS devices and circuits, have done a great job putting together a streamlined presentation of the EKV model. The book covers every aspect of the model, from DC large-signal I-V equations, to charge modeling, nonquasi-static effects, small-signal modeling, noise, small-channel effects, and matching. I have followed the work of the authors and their colleagues for many years with appreciation, and I am delighted to see their results presented in this unified manner. This book will help spread the understanding and use of the EKV model, as the latter certainly deserves.

Prof. Y. Tsividis
Columbia University, New-York
The aggressive downscaling of CMOS technologies that has been going on for more than 25 years has led to an increase in the number of transistors per chip and hence extend the functionality while at the same time dramatically pushing the speed performance. Although these tremendous speed improvements have been mainly driven by the requirements of VLSI digital chips, they have also been exploited for analog and RF circuits. Today, ultra deep-submicron (UDSM) technologies have caught up and even surpassed the transit frequencies achieved by bipolar transistors. This has clearly opened the door to full CMOS highly integrated solutions for wireless applications. Of course, in addition to high transit frequency, good noise performance and low-power consumption are required as well. Since the noise figure also decreases as the transit frequency is increased, it has also clearly taken advantage of the downscaling of the transistor length. At the same time, the supply voltage has had to be decreased progressively in order to limit high electric fields within the device and hence avoid the related high-field effects. The threshold voltage could unfortunately not be scaled in the same proportion without strongly increasing the drain leakage current, which is now seriously affecting the static power consumption of digital chips. This has resulted in a decrease of the overdrive voltage which in turn has moved the operating points of analog transistors more and more from strong inversion to moderate inversion and even into weak inversion. From this perspective, it is important to have a model that accurately predicts the behavior of the MOS transistor in all regions of operation, from weak to strong inversion, through moderate inversion, in a consistent way. This was the primary motivation for developing what today is known as the EKV model.

The purpose of this book is to assemble and explain in a coherent manner all the know-how and all the publications related to the particular MOS transistor modeling approach embodied by the EKV model. This model borrows from the work of a long line of researchers, starting in the early times of semiconductor physics. It has its roots in the search of early designers of very low-power and low-voltage integrated circuits for a description of the transistor behavior fulfilling their specific needs. This book focuses on this particular line of research, with no intention to present all alternative ways of modeling the transistor. Being written by analog circuit designers, it is clearly design-oriented with the purpose of describing the transistor as the basic component of integrated circuits, rather than the result of a sequence of physical processing steps. It gives to emphasis highlighting the properties of the device that can be used by designers to build new robust circuits, or to understand existing circuits and assess their robustness. The book is organized in three hierarchically structured parts. It firstly describes
the basic behavior of the generic MOS transistor, then focuses on additional effects essentially
due to scaling down the device dimensions, and finally discusses the transistors to be used in
RF circuits.

Based on the charge in the channel, the EKV model describes in a continuous manner the
static, dynamic and noise characteristics of the transistor down to very low current levels. The
basic model requires a very limited set of parameters, all of them directly related to basic
independent physical parameters. Intended for analog designers, it conserves the intrinsic
source-drain symmetry of the transistor by using the substrate as the voltage reference and
by introducing the concept of forward and reverse components of the drain current. This
symmetrical approach makes it easier to understand the various modes of static operation
of the device, and to describe them by a single uncomplicated equation. The charge-based
approach lends itself naturally to a coherent description of the dynamic and noise behavior of
the transistor.

The authors want to acknowledge the numerous persons who contributed directly and
indirectly to this book. We are grateful to Dr François Krummenacher for his invaluable
contribution to the EKV model and for his many inputs and suggestions that greatly helped
us to write this book. We have benefited from the many discussions we had with Jean-Michel
Sallese and Ananda Roy who helped us to clarify many fine points along the process of writing
this book. We also would like to acknowledge the contribution of all the other members of the
EKV development team, who each brought their own contribution to the EKV model: Matthias
Bucher, Christophe Lallement, Alain-Serge Porret, Wladek Grabinski. Our gratitude also goes
to Henri Oguye and Stephan Cserveny who pioneered the work for a continuous model and
paved the way for the current EKV model.

Finally, we would like to give special thanks to our families – Dominique, Adrien, Mathilde
and Simon Enz, and Monique, Nathalie and Didier Vittoz – for their support and understanding
during this seemingly endless task.

Christian C. Enz, Eric A. Vittoz
St-Aubin-Sauges, Switzerland
Cernier, Switzerland
# List of Symbols

## Table 0.1 Symbols and their definitions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>(q)</td>
<td>Electron charge</td>
<td>(2.1)</td>
</tr>
<tr>
<td>(k)</td>
<td>Boltzmann’s constant</td>
<td>(2.1)</td>
</tr>
<tr>
<td>(T)</td>
<td>Absolute temperature in degree Kelvin</td>
<td>(2.1)</td>
</tr>
<tr>
<td>(T_n)</td>
<td>Noise temperature in degree Kelvin</td>
<td>(9.141)</td>
</tr>
<tr>
<td>(T_L)</td>
<td>Lattice temperature in degree Kelvin</td>
<td>(9.143)</td>
</tr>
<tr>
<td>(T_C)</td>
<td>Carrier temperature in degree Kelvin</td>
<td>(9.142)</td>
</tr>
<tr>
<td>(\epsilon_0)</td>
<td>Permittivity of free space</td>
<td>3.1</td>
</tr>
<tr>
<td>(\epsilon_{si})</td>
<td>Permittivity of silicon</td>
<td>3.2</td>
</tr>
<tr>
<td>(\epsilon_{ox})</td>
<td>Permittivity of SiO(_2)</td>
<td>3.2</td>
</tr>
<tr>
<td>(n_i)</td>
<td>Intrinsic carrier concentration</td>
<td>3.1</td>
</tr>
<tr>
<td>(\mu)</td>
<td>Mobility of current carriers</td>
<td>(4.1)</td>
</tr>
<tr>
<td>(\mu_0)</td>
<td>Low-field surface mobility</td>
<td>(8.1)</td>
</tr>
<tr>
<td>(\mu_z)</td>
<td>Mobility including the effect of the vertical field</td>
<td>(8.1)</td>
</tr>
<tr>
<td>(\mu_{eff})</td>
<td>Effective mobility including the effects of the vertical and longitudinal fields</td>
<td>(9.2)</td>
</tr>
</tbody>
</table>

**Physical parameters**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>(n_p)</td>
<td>Electron concentration (in P-type Si)</td>
<td>(3.1)</td>
</tr>
<tr>
<td>(p_p)</td>
<td>Hole concentration (in P-type Si)</td>
<td>(3.1)</td>
</tr>
<tr>
<td>(N_b)</td>
<td>Doping concentration of the substrate</td>
<td>3.1</td>
</tr>
<tr>
<td>(N_g)</td>
<td>Doping concentration of the polysilicon gate</td>
<td>8.4</td>
</tr>
<tr>
<td>(N_{diff})</td>
<td>Doping concentration of the source and drain diffusions</td>
<td>4.6.1</td>
</tr>
<tr>
<td>(\Gamma_b)</td>
<td>Substrate modulation factor</td>
<td>(3.30)</td>
</tr>
<tr>
<td>(\Gamma_g)</td>
<td>Depletion factor in the polysilicon gate</td>
<td>(8.54)</td>
</tr>
<tr>
<td>(v_{drift})</td>
<td>Drift velocity</td>
<td>9.1</td>
</tr>
<tr>
<td>(v_{sat})</td>
<td>Saturated drift velocity</td>
<td>9.1</td>
</tr>
</tbody>
</table>

**Process parameters**

continued on next page
**LIST OF SYMBOLS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W$</td>
<td>Channel width</td>
<td>Figure 2.1</td>
</tr>
<tr>
<td>$L$</td>
<td>Channel length</td>
<td>Figure 2.1</td>
</tr>
<tr>
<td>$L_{SD}$</td>
<td>Distance between the source and drain metallurgical junctions</td>
<td>Figure 4.12</td>
</tr>
<tr>
<td>$L_{	ext{eff}}$</td>
<td>Effective channel length</td>
<td>Figure 9.26</td>
</tr>
<tr>
<td>$L_{ov}$</td>
<td>Gate overlap length</td>
<td>Figure 10.10</td>
</tr>
<tr>
<td>$L_f$</td>
<td>Length of a single finger</td>
<td>Figure 11.1</td>
</tr>
<tr>
<td>$W_f$</td>
<td>Width of a single finger</td>
<td>Figure 11.1</td>
</tr>
<tr>
<td>$\Delta L_S$</td>
<td>Channel length reduction at the source</td>
<td>Figure 4.12</td>
</tr>
<tr>
<td>$\Delta L_D$</td>
<td>Channel length reduction at the drain</td>
<td>Figure 4.12</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>Oxide thickness</td>
<td>Figure 2.1</td>
</tr>
<tr>
<td>$x$</td>
<td>Distance from source along the channel</td>
<td>Figure 2.1</td>
</tr>
<tr>
<td>$y$</td>
<td>Distance across the channel</td>
<td>Figure 2.1</td>
</tr>
<tr>
<td>$z$</td>
<td>Distance in direction perpendicular to the surface into the bulk</td>
<td>Figure 2.1</td>
</tr>
</tbody>
</table>

**Voltages and potentials**

- $U_T$: Thermodynamic voltage
- $\Psi$: Electrostatic potential
- $\Psi_s$: Surface potential [$\Psi_s \triangleq \Psi(z = 0)$]
- $\Psi_{SD}$: Surface potential at the source
- $\Psi_{SD}$: Surface potential at the drain
- $\Psi_p$: Pinch-off surface potential
- $\Psi_0$: Approximation of $\Psi_s$ in strong inversion at equilibrium ($V = 0$)
- $\Phi_{ns}$: Difference between the work functions of the gate and the substrate
- $\Phi_F$: Fermi potential of silicon substrate
- $\Phi_{Fn}$: Quasi-Fermi potential of electrons
- $\Phi_B$: Potential barrier of source and drain junctions at equilibrium
- $V_{FB}$: Flat-band voltage
- $V_{TB}$: Threshold function
- $V_{TD}$: Equilibrium threshold voltage
- $V$: Channel voltage
- $V_G$: DC gate-to-bulk voltage
- $V_S$: DC source-to-bulk voltage
- $V_D$: DC drain-to-source voltage
- $\Delta V_G$: Incremental gate-to-bulk voltage
- $\Delta V_S$: Incremental source-to-bulk voltage
- $\Delta V_D$: Incremental drain-to-bulk voltage
- $V_P$: Pinch-off voltage
- $V_{sh}$: Channel voltage shift
- $V_{DS\,	ext{sat}}$: Drain-to-source saturation voltage
- $V_M$: Channel-length modulation voltage (Early voltage)
- $V_{G0}$: Extrapolated band gap voltage

*continued on next page*
### Electric fields

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_c$</td>
<td>Critical longitudinal electric field</td>
<td>(9.1)</td>
</tr>
<tr>
<td>$E_{ox}$</td>
<td>Electric field in the oxide</td>
<td>Figure 2.2</td>
</tr>
<tr>
<td>$E_x$</td>
<td>Electric field along the longitudinal direction</td>
<td>3.1</td>
</tr>
<tr>
<td>$E_y$</td>
<td>Electric field along the lateral direction</td>
<td>3.1</td>
</tr>
<tr>
<td>$E_z$</td>
<td>Electric field along the vertical direction</td>
<td>3.1</td>
</tr>
<tr>
<td>$E_{zs}$</td>
<td>Electric field along the vertical direction at the surface [$E_{zs} \triangleq E_z(z = 0)$]</td>
<td>3.1</td>
</tr>
</tbody>
</table>

### Currents

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D$</td>
<td>Static drain current flowing into the drain terminal</td>
<td>Figure 2.1</td>
</tr>
<tr>
<td>$I_S$</td>
<td>Static source current flowing into the source terminal</td>
<td>5.3</td>
</tr>
<tr>
<td>$I_B$</td>
<td>Static bulk current flowing into the bulk terminal</td>
<td></td>
</tr>
<tr>
<td>$I_G$</td>
<td>Static gate current flowing into the gate terminal</td>
<td>(8.107)</td>
</tr>
<tr>
<td>$I_{spec}$</td>
<td>Specific current</td>
<td>(4.14)</td>
</tr>
<tr>
<td>$I_F$</td>
<td>Static forward current</td>
<td>(4.9)</td>
</tr>
<tr>
<td>$I_R$</td>
<td>Static reverse current</td>
<td>(4.9)</td>
</tr>
<tr>
<td>$I_{DO}$</td>
<td>Off drain current</td>
<td>(4.38)</td>
</tr>
<tr>
<td>$\Delta I_D$</td>
<td>Incremental drain current</td>
<td>5.1.1</td>
</tr>
<tr>
<td>$\Delta I_S$</td>
<td>Incremental source current</td>
<td></td>
</tr>
<tr>
<td>$\Delta I_G$</td>
<td>Incremental gate current</td>
<td></td>
</tr>
<tr>
<td>$\Delta I_B$</td>
<td>Incremental bulk current</td>
<td></td>
</tr>
</tbody>
</table>

### Charges

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_i$</td>
<td>Inversion mobile charge density</td>
<td>Figure 2.2</td>
</tr>
<tr>
<td>$Q_{iS}$</td>
<td>Inversion mobile charge density at the source</td>
<td>Figure 2.2</td>
</tr>
<tr>
<td>$Q_{iD}$</td>
<td>Inversion mobile charge density at the drain</td>
<td>Figure 2.2</td>
</tr>
<tr>
<td>$Q_b$</td>
<td>Depletion charge density</td>
<td>Figure 2.2</td>
</tr>
<tr>
<td>$Q_g$</td>
<td>Gate charge density</td>
<td>Figure 2.2</td>
</tr>
<tr>
<td>$Q_{fc}$</td>
<td>Fixed charge density</td>
<td>Figure 2.2</td>
</tr>
<tr>
<td>$Q_{spec}$</td>
<td>Specific charge density</td>
<td>(3.42)</td>
</tr>
<tr>
<td>$Q_{si}$</td>
<td>Semiconductor total charge density</td>
<td>2.2</td>
</tr>
<tr>
<td>$Q_1$</td>
<td>Total channel charge</td>
<td>(6.16), (6.19)</td>
</tr>
</tbody>
</table>

### Resistances, conductances, and transconductances

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_S$</td>
<td>Source series resistance</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>$R_D$</td>
<td>Drain series resistance</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>$R_G$</td>
<td>Gate series resistance</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>$R_B$</td>
<td>Bulk series resistance</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>$R_{sde}$</td>
<td>Source and drain extension resistance</td>
<td>Figure 10.2(b)</td>
</tr>
</tbody>
</table>

continued from previous page

continued on next page
### List of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{con}}$</td>
<td>Source and drain contact resistance</td>
<td>Figure 10.2(b)</td>
</tr>
<tr>
<td>$R_{\text{sal}}$</td>
<td>Source and drain salicide resistance</td>
<td>Figure 10.2(b)</td>
</tr>
<tr>
<td>$R_{\text{via}}$</td>
<td>Source and drain via resistance</td>
<td>Figure 10.2(b)</td>
</tr>
<tr>
<td>$R_{\text{DSB}}$</td>
<td>Source-to-drain substrate resistance</td>
<td>Figure 11.9(c)</td>
</tr>
<tr>
<td>$R_{\text{BS}}$</td>
<td>Source-to-bulk substrate resistance</td>
<td>Figure 11.9(c)</td>
</tr>
<tr>
<td>$R_{\text{BD}}$</td>
<td>Drain-to-bulk substrate resistance</td>
<td>Figure 11.9(c)</td>
</tr>
<tr>
<td>$G_{\text{ch}}$</td>
<td>Channel conductance</td>
<td>(9.116)</td>
</tr>
<tr>
<td>$G_{\text{ds}}$</td>
<td>Residual output conductance in saturation</td>
<td>(5.22)</td>
</tr>
<tr>
<td>$G_{\text{spec}}$</td>
<td>Specific conductance</td>
<td>(5.6)</td>
</tr>
<tr>
<td>$G_{m}$</td>
<td>Gate transconductance</td>
<td>(5.2c)</td>
</tr>
<tr>
<td>$G_{\text{ms}}$</td>
<td>Source transconductance</td>
<td>(5.2a)</td>
</tr>
<tr>
<td>$G_{\text{md}}$</td>
<td>Drain transconductance</td>
<td>(5.2b)</td>
</tr>
<tr>
<td>$G_{mb}$</td>
<td>Bulk transconductance</td>
<td>13.3.2</td>
</tr>
</tbody>
</table>

### Capacitances and Transcapacitances

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{\text{ox}}$</td>
<td>Oxide capacitance per unit area</td>
<td>3.2</td>
</tr>
<tr>
<td>$C_{\text{OX}}$</td>
<td>Total oxide capacitance</td>
<td>5.2</td>
</tr>
<tr>
<td>$C_{\text{si}}$</td>
<td>Silicon capacitance per unit area</td>
<td>(3.23)</td>
</tr>
<tr>
<td>$C_{g}$</td>
<td>Gate capacitance per unit area</td>
<td>(3.25)</td>
</tr>
<tr>
<td>$C_{d}$</td>
<td>Depletion capacitance per unit area</td>
<td>3.3</td>
</tr>
<tr>
<td>$C_{\text{OX}}$</td>
<td>Total oxide capacitance</td>
<td>(5.38)</td>
</tr>
<tr>
<td>$C_{\text{GSi}}$</td>
<td>Intrinsic gate-to-source capacitance</td>
<td>Figure 5.14</td>
</tr>
<tr>
<td>$C_{\text{GDi}}$</td>
<td>Intrinsic gate-to-drain capacitance</td>
<td>Figure 5.14</td>
</tr>
<tr>
<td>$C_{\text{GBi}}$</td>
<td>Intrinsic gate-to-bulk capacitance</td>
<td>Figure 5.14</td>
</tr>
<tr>
<td>$C_{\text{BSi}}$</td>
<td>Intrinsic bulk-to-source capacitance</td>
<td>Figure 5.14</td>
</tr>
<tr>
<td>$C_{\text{BDi}}$</td>
<td>Intrinsic bulk-to-drain capacitance</td>
<td>Figure 5.14</td>
</tr>
<tr>
<td>$C_{\text{GGi}}$</td>
<td>Total intrinsic gate capacitance</td>
<td>(11.4)</td>
</tr>
<tr>
<td>$C_{m}$</td>
<td>Intrinsic gate transcapacitance</td>
<td>(5.58)</td>
</tr>
<tr>
<td>$C_{\text{ms}}$</td>
<td>Intrinsic source transcapacitance</td>
<td>(5.56)</td>
</tr>
<tr>
<td>$C_{\text{md}}$</td>
<td>Intrinsic drain transcapacitance</td>
<td>(5.57)</td>
</tr>
<tr>
<td>$C_{\text{GSo}}$</td>
<td>Gate-to-source overlap capacitance</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>$C_{\text{GDo}}$</td>
<td>Gate-to-drain overlap capacitance</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>$C_{\text{GBo}}$</td>
<td>Gate-to-bulk overlap capacitance</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>$C_{\text{GGo}}$</td>
<td>Total gate overlap capacitance</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>$C_{\text{BSj}}$</td>
<td>Source-to-bulk junction capacitance</td>
<td>10.4</td>
</tr>
<tr>
<td>$C_{\text{BDj}}$</td>
<td>Drain-to-bulk junction capacitance</td>
<td>10.4</td>
</tr>
<tr>
<td>$C_{\text{GS}}$</td>
<td>Total gate-to-source capacitance</td>
<td>(12.1)</td>
</tr>
<tr>
<td>$C_{\text{GD}}$</td>
<td>Total gate-to-drain capacitance</td>
<td>(12.1)</td>
</tr>
<tr>
<td>$C_{\text{GB}}$</td>
<td>Total gate-to-bulk capacitance</td>
<td>(12.1)</td>
</tr>
<tr>
<td>$C_{\text{BS}}$</td>
<td>Total bulk-to-source capacitance</td>
<td>(12.1)</td>
</tr>
<tr>
<td>$C_{\text{BD}}$</td>
<td>Total bulk-to-drain capacitance</td>
<td>(12.1)</td>
</tr>
<tr>
<td>$C_{G}$</td>
<td>Total gate capacitance</td>
<td>(12.6)</td>
</tr>
<tr>
<td>$C_{g}$</td>
<td>Local gate capacitance per unit area</td>
<td>3.3</td>
</tr>
</tbody>
</table>

continued on next page
## LIST OF SYMBOLS

```

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Admittances and transadmittances</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Y_{GSi}$</td>
<td>Intrinsic gate-to-source admittance</td>
<td>Figure 5.9</td>
</tr>
<tr>
<td>$Y_{GDi}$</td>
<td>Intrinsic gate-to-drain admittance</td>
<td>Figure 5.9</td>
</tr>
<tr>
<td>$Y_{GBi}$</td>
<td>Intrinsic gate-to-bulk admittance</td>
<td>Figure 5.9</td>
</tr>
<tr>
<td>$Y_{BSi}$</td>
<td>Intrinsic bulk-to-source admittance</td>
<td>Figure 5.9</td>
</tr>
<tr>
<td>$Y_{BDi}$</td>
<td>Intrinsic bulk-to-drain admittance</td>
<td>Figure 5.9</td>
</tr>
<tr>
<td>$Y_m$</td>
<td>Intrinsic gate transadmittance</td>
<td>(5.36)</td>
</tr>
<tr>
<td>$Y_{ms}$</td>
<td>Intrinsic source transadmittance</td>
<td>(5.36)</td>
</tr>
<tr>
<td>$Y_{md}$</td>
<td>Intrinsic drain transadmittance</td>
<td>(5.36)</td>
</tr>
<tr>
<td>$Y_{sub}$</td>
<td>Substrate admittance</td>
<td>Figure 12.4</td>
</tr>
<tr>
<td></td>
<td><strong>Frequency and time constants</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\omega_t$</td>
<td>Transit frequency</td>
<td>(11.4)</td>
</tr>
<tr>
<td>$\tau_{qs}$</td>
<td>Intrinsic channel time constant</td>
<td>(5.32)</td>
</tr>
<tr>
<td>$\omega_{qs}$</td>
<td>Intrinsic channel transit frequency</td>
<td>(5.32)</td>
</tr>
<tr>
<td> </td>
<td>    (also limit between quasi-static and non-quasi static operation)</td>
<td></td>
</tr>
<tr>
<td>$\omega_{\text{max}}$</td>
<td>Extrapolated maximum frequency of oscillation</td>
<td>(11.18)</td>
</tr>
<tr>
<td>$\omega_{\text{spec}}$</td>
<td>Specific (or critical) frequency</td>
<td>(5.33)</td>
</tr>
<tr>
<td>$\tau_{\text{spec}}$</td>
<td>Specific time constant</td>
<td>(5.33)</td>
</tr>
<tr>
<td></td>
<td><strong>Noise</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$S_{\Delta I^2_{D}}$</td>
<td>Thermal noise power spectral density at the drain</td>
<td>(6.4), (6.14)</td>
</tr>
<tr>
<td>$S_{\Delta I^2_{S}}$</td>
<td>Thermal noise power spectral density at the source</td>
<td>(13.42)</td>
</tr>
<tr>
<td>$S_{\Delta I^2_{G}}$</td>
<td>Thermal noise power spectral density at the gate</td>
<td>(13.42)</td>
</tr>
<tr>
<td> </td>
<td>    (induced gate noise power spectral density)</td>
<td></td>
</tr>
<tr>
<td>$S_{\Delta I^2_{B}}$</td>
<td>Thermal noise power spectral density at the bulk</td>
<td>(13.42)</td>
</tr>
<tr>
<td>$S_{\Delta I_{GD} \Delta I^*_{AD}}$</td>
<td>Thermal noise gate-drain cross-power spectral density</td>
<td>(13.42)</td>
</tr>
<tr>
<td>$G_{nD}$</td>
<td>Drain thermal noise conductance</td>
<td>(6.15)</td>
</tr>
<tr>
<td>$G_{nG}$</td>
<td>Gate thermal noise conductance</td>
<td>(13.49)</td>
</tr>
<tr>
<td> </td>
<td>    (induced gate noise thermal conductance)</td>
<td></td>
</tr>
<tr>
<td>$\delta_{nD}$</td>
<td>Thermal noise parameter at the drain</td>
<td>(6.26)</td>
</tr>
<tr>
<td>$\delta_{nG}$</td>
<td>Thermal noise parameter at the gate</td>
<td>(13.49)</td>
</tr>
<tr>
<td>$\gamma_{nD}$</td>
<td>Thermal noise excess factor at the drain</td>
<td>(6.30)</td>
</tr>
<tr>
<td>$\gamma_{nG}$</td>
<td>Thermal noise excess factor at the gate</td>
<td>(13.49)</td>
</tr>
<tr>
<td>$\rho_{GD}$</td>
<td>Gate-drain thermal noise correlation factor</td>
<td>(13.71)</td>
</tr>
<tr>
<td>$S_v$</td>
<td>Input-referred thermal noise voltage power spectral density</td>
<td>(13.13)</td>
</tr>
<tr>
<td>$S_i$</td>
<td>Input-referred thermal noise current power spectral density</td>
<td>(13.13)</td>
</tr>
<tr>
<td>$R_v$</td>
<td>Input-referred thermal noise voltage resistance</td>
<td>(13.13)</td>
</tr>
<tr>
<td>$G_i$</td>
<td>Input-referred thermal noise current conductance</td>
<td>(13.13)</td>
</tr>
<tr>
<td>$G_{iu}$</td>
<td>Uncorrelated part of $G_i$</td>
<td>(13.14)</td>
</tr>
</tbody>
</table>

*continued on next page*
# LIST OF SYMBOLS

**continued from previous page**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>( G_{ic} )</td>
<td>Correlated part of ( G_i )</td>
<td>(13.14)</td>
</tr>
<tr>
<td>( Y_c )</td>
<td>Noise correlation admittance</td>
<td>(13.8)</td>
</tr>
<tr>
<td>( G_c )</td>
<td>Noise correlation conductance</td>
<td>(13.16)</td>
</tr>
<tr>
<td>( B_c )</td>
<td>Noise correlation susceptance</td>
<td>(13.16)</td>
</tr>
<tr>
<td>( F )</td>
<td>Noise factor</td>
<td>(13.17), (13.21), (13.26)</td>
</tr>
<tr>
<td>( NF )</td>
<td>Noise figure</td>
<td>(13.17)</td>
</tr>
<tr>
<td>( F_{min} )</td>
<td>Minimum noise factor</td>
<td>(13.25)</td>
</tr>
<tr>
<td>( NF_{min} )</td>
<td>Minimum noise figure</td>
<td>(13.25)</td>
</tr>
<tr>
<td>( Y_{opt} )</td>
<td>Optimum source admittance for ( F = F_{min} )</td>
<td>(13.24)</td>
</tr>
<tr>
<td>( G_{opt} )</td>
<td>Optimum source conductance</td>
<td>(13.24)</td>
</tr>
<tr>
<td>( B_{opt} )</td>
<td>Optimum source susceptance</td>
<td>(13.24)</td>
</tr>
<tr>
<td>Other</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( \rho )</td>
<td>Charge concentration</td>
<td>(3.1)</td>
</tr>
<tr>
<td>( L_D )</td>
<td>Extrinsic Debye length</td>
<td>(3.15)</td>
</tr>
<tr>
<td>( L_{c0} )</td>
<td>Characteristic length for DIBL</td>
<td>(9.100)</td>
</tr>
<tr>
<td>( t_d )</td>
<td>Thickness of the depletion layer</td>
<td>(3.26)</td>
</tr>
<tr>
<td>( n )</td>
<td>Slope factor</td>
<td>(3.34)</td>
</tr>
<tr>
<td>( n_w )</td>
<td>Slope factor evaluated at pinch-off</td>
<td>(3.68)</td>
</tr>
<tr>
<td>( n_0 )</td>
<td>Slope factor evaluated at ( V = 0 )</td>
<td>(3.73)</td>
</tr>
<tr>
<td>( n_q )</td>
<td>Charge slope factor</td>
<td>(8.60)</td>
</tr>
<tr>
<td>( n_v )</td>
<td>Voltage slope factor</td>
<td>(8.60)</td>
</tr>
<tr>
<td>( \beta )</td>
<td>Transconductance factor or transfer parameter</td>
<td>(4.7)</td>
</tr>
<tr>
<td>( D_S )</td>
<td>Source-to-bulk diode</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>( D_D )</td>
<td>Drain-to-bulk diode</td>
<td>Figure 10.1</td>
</tr>
<tr>
<td>( A_{v_{max}} )</td>
<td>Maximum voltage gain in common gate</td>
<td>(5.24), (9.115)</td>
</tr>
<tr>
<td>( \Delta P )</td>
<td>Mismatch of parameter ( P )</td>
<td>(7.52)</td>
</tr>
<tr>
<td>( A_P )</td>
<td>Area proportionality constant of parameter ( P )</td>
<td>(7.52)</td>
</tr>
<tr>
<td>( \theta )</td>
<td>Parameter of field-dependent mobility</td>
<td>(8.5)</td>
</tr>
<tr>
<td>( z_c )</td>
<td>Characteristic depth</td>
<td>Figure 8.7</td>
</tr>
<tr>
<td>( v_{drift} )</td>
<td>Drift velocity of carriers</td>
<td>Figure 9.1</td>
</tr>
<tr>
<td>( v_{sat} )</td>
<td>Saturation value of ( v_{drift} )</td>
<td>Figure 9.1</td>
</tr>
<tr>
<td>( \lambda_c )</td>
<td>Velocity saturation parameter</td>
<td>(9.19)</td>
</tr>
</tbody>
</table>

<p>| Table 0.2 | Normalization factor definition | |</p>
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L )</td>
<td>Transistor length for normalizing distance along the ( x )-axis</td>
<td>2.1</td>
</tr>
<tr>
<td>( U_T ) ( \triangleq ) ( kT ) ( q )</td>
<td>Thermodynamic voltage for normalizing voltages and potentials</td>
<td>2.1</td>
</tr>
<tr>
<td>( I_{spec} ) ( \triangleq ) ( 2n\beta U_T^2 )</td>
<td>Specific current for normalizing currents</td>
<td>(4.14)</td>
</tr>
<tr>
<td>( Q_{spec} ) ( \triangleq ) ( -2nC_{ox}U_T )</td>
<td>Specific charge density for normalizing charge densities</td>
<td>3.6.1</td>
</tr>
<tr>
<td>( C_{ox} ) ( \triangleq ) ( WL_{Cox} )</td>
<td>Total oxide capacitance for normalizing capacitances</td>
<td>5.2</td>
</tr>
<tr>
<td>( G_{spec} ) ( \triangleq ) ( \frac{I_{spec}}{U_T^2} )</td>
<td>Specific admittance for normalizing admittances</td>
<td>(5.6)</td>
</tr>
<tr>
<td>( \omega_{spec} ) ( \triangleq ) ( \frac{2n\mu dU_T}{L^2} )</td>
<td>Specific angular frequency for normalizing angular frequency</td>
<td>5.2</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Reference</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>-----------</td>
</tr>
<tr>
<td>$\xi \triangleq x/L$</td>
<td>Normalized position along the $x$-axis</td>
<td>(4.21)</td>
</tr>
<tr>
<td>$\zeta_c$</td>
<td>Normalized characteristic depth</td>
<td>(8.24)</td>
</tr>
<tr>
<td>$\nu$</td>
<td>Doping ratio</td>
<td>(8.32)</td>
</tr>
<tr>
<td>$\lambda_0 \triangleq L/L_c$</td>
<td>Channel length normalized to characteristic length</td>
<td>(9.100)</td>
</tr>
<tr>
<td>$v_x \triangleq V_X/U_T$</td>
<td>Normalized voltage</td>
<td>(3.43)</td>
</tr>
<tr>
<td>$\gamma_j \triangleq (\Gamma_j/U_T)^2$</td>
<td>Normalized modulation factor</td>
<td>(3.43)</td>
</tr>
<tr>
<td>$\phi_f \triangleq \Phi_f/U_T$</td>
<td>Normalized Fermi potential of silicon substrate</td>
<td>3.1</td>
</tr>
<tr>
<td>$\psi_p \triangleq \Psi_p/U_T$</td>
<td>Normalized pinch-off surface potential</td>
<td>(3.37)</td>
</tr>
<tr>
<td>$\psi_0 \triangleq \Psi_0/U_T$</td>
<td>Normalized approximation of $\Psi_s$ in strong inversion</td>
<td>(3.66)</td>
</tr>
<tr>
<td>$i_x \triangleq I_X/I_{spec}$</td>
<td>Normalized drain current</td>
<td>(4.15)</td>
</tr>
<tr>
<td>$I_C$</td>
<td>Inversion coefficient or factor</td>
<td>(4.26)</td>
</tr>
<tr>
<td>$g_x \triangleq G_x/G_{spec}$</td>
<td>Normalized conductance or transconductance</td>
<td></td>
</tr>
<tr>
<td>$q_x \triangleq Q_X/Q_{spec}$</td>
<td>Normalized charge density</td>
<td>(3.41)</td>
</tr>
<tr>
<td>$q_s \triangleq Q_{is}/Q_{spec}$</td>
<td>Normalized inversion charge density at the source</td>
<td>(5.7a)</td>
</tr>
<tr>
<td>$q_d \triangleq Q_{id}/Q_{spec}$</td>
<td>Normalized inversion charge density at the drain</td>
<td>(5.7b)</td>
</tr>
<tr>
<td>$q_X \triangleq Q_X/Q_{spec}$</td>
<td>Normalized total charge</td>
<td></td>
</tr>
<tr>
<td>$\Omega \triangleq \omega/\omega_{spec}$</td>
<td>Normalized frequency</td>
<td>13.2.2</td>
</tr>
<tr>
<td>$\Omega_{qs} \triangleq \omega_{qs}/\omega_{spec}$</td>
<td>Normalized QS frequency</td>
<td>(5.32)</td>
</tr>
<tr>
<td>$c_j \triangleq C_j/C_{ox}$</td>
<td>Normalized capacitance per unit area</td>
<td>(5.50)</td>
</tr>
<tr>
<td>$c_j^* \triangleq C_j/C_{ox}$</td>
<td>Normalized total capacitance</td>
<td>(5.50)</td>
</tr>
</tbody>
</table>
1 Introduction

This chapter explains the basic motivations for developing MOS transistor models that can be used for the design of complementary MOS (CMOS) integrated circuits. It then gives a short history of the EKV MOS transistor model starting from the early development, motivated by the design of micropower circuits for watch applications, to the most recent developments. Finally, the structure of the book is highlighted in order to help the reader organizing his reading.

1.1 THE IMPORTANCE OF DEVICE MODELING FOR IC DESIGN

Modern large-scale integrated circuits are essentially composed of MOS transistors and their interconnections. Therefore, the design of such circuits requires some kind of a model for the transistors.

For noncritical digital circuits, this model may in principle be very simple. Indeed, modeling each transistor as an on–off switch would be sufficient to design purely logic circuits. However, as soon as there are critical races among transitions, the model must be extended to describe the dynamic behavior of the device, in order to obtain the rise and fall time of these transitions. This dynamic behavior is also needed when the frequency of operation approaches its maximum limit. With the reduction of supply voltage, more details must be introduced, such as the residual current of blocked transistors, the importance of which is increased.

Analog circuits contain usually a smaller number of transistors, but they are even more dependent on the exact behavior of each transistor. The design of high-performance analog circuits therefore requires a very detailed model of the transistor. This model must include a precise description of the voltage–current relationships, including the effect of the source that is often not grounded, and of the dynamic behavior of the device. Its behavior with respect to noise and to temperature variations must also be accounted for.

A transistor model intended for circuit design should serve two essential purposes:

It should first provide a good understanding of the various properties of the device to facilitate the synthesis of optimum circuit architectures. Indeed, in order to build robust circuits, the
physical properties of the transistor must be exploited in a way that is minimally dependent on temperature and process variations. For this purpose, the model should be explicit. It should “speak to the mind,” using no complicated or chained equations. Clarity should supersede precision and can be enhanced by means of graphical representations. This important aspect of a model is often underestimated and overlooked. It will be emphasized in this book, in particular in Part I, which essentially describes what can be called the core of the model.

Second, the model should be adapted to numerical simulations on a computer, embedded in a circuit simulator. For this purpose, precision supersedes clarity, and second-order effects must be accounted for. This can be obtained by predistorting variables, by chaining equations and/or by providing additional layers around a core model. The model does not need to be fully explicit, but it should be compact: it should use sufficiently simple expressions with minimum need for numerical iterations, in order to limit the computation time.

A transistor model should include a minimum number of process-dependent device parameters. This is to facilitate the very heavy task of extracting and following-up the value of these parameters, with their statistical distribution and temperature dependency.

Now, the correlation between these parameters (with process and temperature variations) must be known, in order to avoid designing circuits for irrelevant worst cases. For this reason, the device parameters should be explicitly based on independent and measurable process parameters. This is essential to be able to ascertain their amount of correlations while avoiding the almost impossible task of measuring all these correlations. It also makes the model predictive, allowing to foresee the characteristics of the transistor and hence the performance of the resulting circuits even before measuring the device.

The EKV model described in this book is believed to meet all the above expectations. It serves the two main purposes in a coherent manner. Its core requires just a few parameters to describe all the basic properties of the long-channel intrinsic device in an explicit manner. Layers are added to this core to account for short-channel and secondary effects.

1.2 A SHORT HISTORY OF THE EKV MOS TRANSISTOR MODEL

The model presented in this book results from a series of direct and indirect contributions along several decades. Its origins can be traced back to the early developments of electronic watches at CEH (French acronym for Watchmakers Electronic Center) in Switzerland [2].

The total power consumption had to be extremely low, less than 1μW, to ensure a few years of life to the single button-size cell battery. After the very first versions based on bipolar transistors [3], the CMOS technology was soon identified as the best approach to implement the digital electronic circuitry needed in a watch using a crystal resonator as the time reference. Supply voltage had to be very low, compatible with the 1.3 V delivered by the cell, so the development of low-threshold CMOS was a major challenge in the late 1960’s [4].

The digital circuitry was essentially an asynchronous chain of divide-by-two stages. The main design problem was to minimize the number of node transitions in order to minimize the dynamic power. Another one was the elimination of logic hazards to improve the robustness against large local variations of the small gate voltage overhead, and this led to the first single clock circuits [5–7]. For these digital circuits, MOS transistors could be considered just as switches and hence no special model was required.
The problem was very different for the few analog subcircuits. Most important was the circuitry needed to sustain the oscillation of the quartz crystal resonator (the quartz oscillator). Each transistor had to be biased at a drain current much below 1 μA. Early measurements carried out in 1967 showed that the transistor behaved in a very strange manner at these very low current levels. Indeed, the well-known square-law transfer characteristics were replaced by an exponential over more than 5 order of magnitude of the drain current, very similar to bipolar transistors. This is how weak inversion popped out to the attention of micropower circuit designers in the late 1960s.

At that time, no transistor model was available for weak inversion, but they started coming out in subsequent years, mainly to account for what appears in digital circuits as a leakage current of blocked transistors. In 1972, M. B. Barron published a model for the grounded source device showing the exponential dependencies on drain voltage and on surface potential, with a rather complex expression relating the surface potential to the gate voltage [8]. The same year, R. M. Swanson and J. D. Meindl [9] showed that this relation could be accounted for by means of an almost constant factor, which became the slope factor \( n \) of our model. The following year, R. R. Troutman and S. N. Chakravarti [10] treated the case of nonzero source voltage. Then T. Mashuhara et al. [11] showed that the current depends on a difference of exponential functions of source and drain voltages. In the mean time, micropower analog circuit blocks were developed at CEH. They were first published in 1976 [12, 13], together with a model applicable for weak inversion circuit design, which was based on the previously mentioned work. This model already included two important features of the EKV model: reference to the \((\text{local})\ substrate\) (and not to the source) for all voltages and full source–drain symmetry. The related small-signal model including noise was also presented [14].

A symmetrical model of the MOS transistor in strong inversion was first published by P. Jespers in 1977 [15, 16]. Based on an idea of O. Memelink, this graphical model uses the approximately linear relationship between the local mobile charge density and the local “non-equilibrium” voltage in the channel. This charge-based approach has been adopted and generalized to all levels of current in the EKV model.

Another ingredient of EKV is the representation of the drain current as the difference between a \( \text{forward} \) and a \( \text{reverse} \) component. This idea was first introduced in 1979 by J.-D. Châtelain [17], by similarity with the Ebers–Moll model of bipolar transistors [18]. However, his definition of these two components was different from that adopted later, and was not applicable to weak inversion.

Even in micropower analog circuits, not all transistors should be biased in weak inversion. There was therefore a need for a good continuous model from weak to strong inversion. Such a model was developed at CEH by H. Oguey and S. Cserveny, and was first published in French in 1982 [19]. The only publication in English was at a Summer Course given in 1983 [20].

This model embodied most of the basic features that were retained later. It introduced a function of the gate voltage called control voltage, later renamed \( \text{pinch-off voltage} V_p \). A single function of this control voltage and of either the source voltage or the drain voltage defined two components of the drain current (which became the forward and reverse components). This function was continuous from weak to strong inversion, using a mathematical interpolation to best fit moderate inversion.

In the mid-1980s, the model of Oguey and Cserveny was simplified by the second author for his undergraduate teaching at EPFL (Swiss federal Institute of Technology, Lausanne, Switzerland), and most further developments were carried out there. They started with the Ph.D. Thesis of the first author [21], in collaboration with F. Krummenacher. The model was
formulated more explicitly. Noise and dynamic behavior were introduced by exploiting the fundamental source–drain symmetry. The status of the model was presented at various Summer Courses [22–24] and a full paper was finally published in 1995 [25]. This publication gave its name to the model, but many important extensions were added later.

Probably the most important extension was the replacement of the current and transconductance interpolation functions between weak and strong inversion presented in [25] by a more physical based one, derived from an explicit linearization of the inversion charge versus the surface potential. The incremental linear relationship between inversion charge and surface potential was first considered by M. Bagheri and C. Turchetti [26], but the linearization of the inversion charge versus surface potential was originally proposed in 1987 by M. Maher and C. Mead [27, 28]. Several years later, different groups looked at this problem. B. Iñiguez and E. G. Moreno [29, 30] derived an approximate explicit relation between inversion charges and surface potential which included a fitting parameter. While their first linearization was done at the source [29], they later obtained a substrate referenced model based on the original EKV MOSFET model approach [25], which also included some short-channel effects. A similar approach was also proposed by Cunha et al. [31–34] who obtained an interpolated expression of the charges versus the potentials that used the basic EKV model definitions\textsuperscript{1} [25] and was closely inspired from our approach. We also adopted the inversion charge linearization approach, since it offers physical expressions for both the transconductance-to-current ratio and the current that are valid from weak to strong inversion [35–38]. This gave rise to the \textit{charge-based EKV model} which is discussed in this book. The inversion charge linearization principle was rediscovered once more in 2001 by H. K. Gummel and K. Singhal [39, 40]. Finally, a formal detailed analysis of the inversion charge linearization process and a rigorous derivation of the EKV model was finally published by J.-M. Sallese \textit{et al.} in [41].

Note that this approach actually provides voltages versus currents expressions that cannot be explicitly inverted. It can nevertheless be easily inverted by using a straightforward Newton-Raphson technique or by an appropriate approximation. Both these techniques have been used in the final model implementation.

The basic long-channel charge-based EKV model was further developed by the EKV team to include the following additional effects:

\textbf{Nonuniform doping:} Nonuniform doping in the vertical direction was proposed by C. Lallement \textit{et al.} in [42, 43].

\textbf{Non-quasi-static model:} A small-signal charge-based non-quasi-static model was presented by J.-M. Sallese and A.-S. Porret in [38, 44].

\textbf{Polysilicon depletion and quantum effects:} Polysilicon depletion and quantum effects were also added [45–47].

\textbf{RF modeling:} The EKV model was extended by the first author to also cover high-frequency operation for the design of RF CMOS integrated circuits [48–52].

\textbf{Thermal noise:} An accurate thermal noise model accounting for short-channel effects was developed by A. S. Roy and C. C. Enz [53–55].

\textsuperscript{1} Unfortunately, Cunha \textit{et al.} did not use the same definition of the specific current we have been using. Their specific current is actually four times smaller.