Nanometer Frequency Synthesis
Beyond the Phase-Locked Loop

Liming Xiu

IEEE Series on Microelectronic Systems
R. Jacob Baker, Series Editor

Circuit Design
Flying-Adder Frequency Analysis Architecture™
Number Theory
Fourier Analysis
Time-Average-Frequency Concept

A NEW FRONTIER IN ELECTRONIC SYSTEM DESIGN

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NANOMETER FREQUENCY SYNTHESIS BEYOND THE PHASE-LOCKED LOOP
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NANOMETER FREQUENCY SYNTHESIS BEYOND THE PHASE-LOCKED LOOP

LIMING XIU

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PREFACE

I have no special talents. I am only passionately curious.

—Albert Einstein

In the great Einstein’s view, passion, desire—and above all curiosity—are the very ignition switches to spark discovery and creation. More than two decades ago, when I was studying physics in Tsinghua University (Beijing, China), this confession seemed counterfactual. After 20 years of involvement in scientific and engineering work, it is gradually starting to make sense to me. Nowadays, there are 7 billion people living on this planet. If all the people who ever lived on Earth were included, this enormous number would be exponentially larger. Among this gigantic population there are countless gifted people who are born with talent. However, history shows that only a tiny handful of people have made paramount contributions to the understanding of the world we all live in. The force that separates these all-time greats from the exceptional group of the talented is the passion to ask what and why, sincerely and unyieldingly.

FREQUENCY IS CHANGED

I am neither the great nor the gifted. But this force of curiosity does have its hold over me. In my career as a very-large-scale integration (VLSI) circuit design professional, I have had the fortune to work in many different areas (please see my other book: *VLSI Circuit Design Methodology Demystified: A Conceptual Taxonomy*, 2007). This unique experience provides me with the opportunity to observe everything from a broader viewpoint, the ability to see things in the bigger picture. In the meantime, it engages my curiosity. It often
drives me to challenge the conventional way of doing things. One particular example is the clock signal used in the VLSI circuit. As both a circuit level phase-locked loop (PLL) designer and a system-on-a-chip integration level PLL user, I have seen the story from both sides. I distinctly remember one afternoon in the summer of 2003, after spending a long time explaining the flying-adder architecture (invented in the late 1990s) to one of my colleagues, a question suddenly occurred to me: What is frequency? Why must all the cycles have equal lengths in time? In common sense, this question looks foolish and dangerous for anyone to ask. Curiosity about this issue has intrigued me for several years (secretly, for fear of being treated as an illiterate). In 2008, after a long period of serious investigation from both theoretical and experimental perspectives, I had built up enough nerve to formally introduce the concept of “time-average-frequency.” It removes the constraint that all clock cycles must have the same length-in-time. This seemingly ridiculous or insignificant step is a bold move philosophically. Its aim is the two long-lasting problems in this field: arbitrary frequency generation and fast response in frequency switching. It will have profound influence in VLSI circuit design since clock signal is used in every chip. Along the running history of our progressive understanding of this world, it is shown that all the great advancements originate at the concept level. The greatest example is provided by Einstein. By changing our view of the two fundamental concepts of time and space, he brought us one giant step closer to the ultimate understanding of the universe. This has forever changed the way we live. In this book, the most important message that I want to share with reader is: the concept of clock frequency is changed.

Your time is limited, so don’t waste it living someone else’s life. Don’t be trapped by dogma—which is living with the results of other people’s thinking. Don’t let the noise of others’ opinions drown out your own inner voice. And most important, have the courage to follow your heart and intuition.

—Steve Jobs

The spirit behind this excerpt from Steve Jobs’s famous speech (Stanford University, 2005) is not unfamiliar. Similar wisdom has been expressed in the past by great philosophers and pioneers. But Mr. Jobs’s testimony is more touching and real to us as individuals because he lived in our time. He noticeably changed the face of technology and the modern way of life, and he preached his passion in a way that was pleasantly contagious. During the pursuit of time-average-frequency, I sometimes felt frustrated because this new thinking contradicts conventional wisdom. On several occasions, a painful price had to be paid to uphold what I believe. Today, whenever Jobs’s remark is replayed, I feel a bit of warmth and encouragement. Looking at his journey, it is confirmed again that all the greats have their own obstacles. The key to success is not superior intellect or powerful financial muscle. Instead, it is the intrinsic drive to believe, to achieve, and to change. This book is my case of this testimony.
SIMPLE AND ELEGANT

Coupled with curiosity, the other important part of my mindset is the tenacious
desire to pursue simplicity and elegance in almost everything. I admire
beautiful things in life: beautiful music, beautiful art, beautiful literature, beau-
tiful sportsmanship, a beautiful soul—the list goes on and on. During the
creation of the flying-adder circuit, simplicity drove me to search unrelentingly
for the simplest structure that required the minimum number of transistors
possible. Elegance compelled me to ensure that there is a sophisticated and
yet beautiful mechanism behind the simple circuit. I am a passionate believer
of the “Principle of Least Action” (Pierre-Louis Maupertuis, 1774). I apply it
to my circuit design whenever I can. I hope that I can convey this attitude to
readers throughout this book.

TIME, NUMBER, AND THE BEAUTY OF MATHEMATICS

The key focus of this book—frequency—is closely related to the thing that we
called time. Time is a major subject of religion, philosophy, and science. Among
great thinkers, there are two distinct standpoints on time. One view is that time
is part of the fundamental structure of the universe, a dimension in which
events occur in sequence. The opposing view is that time does not refer to any
kind of physical container that events and objects move through. Instead, time
is part of a fundamental intellectual structure (made of space, number, and
time) within which humans sequence and compare events. In this second view,
time is a virtual subject, neither an event nor a thing, and thus is not itself
measurable.

Another mysterious product from human brain is the number. The world
is virtually made of numbers. Numbers were invented to fulfill the need
to organize our life quantitatively, beyond just qualitatively. It is generally
believed that this is one of the major reasons why humans and all other species
have followed different evolutionary paths (language is among the others). In
our daily life, time and number are connected though an entity called the
atomic clock: the definition of second. In VLSI circuit design, time and number
are related by a special signal called clock. In this engineering practice, how-
ever, the relationship between time (frequency) and number has not reached
the harmonization achieved in our daily life. In this book, one of the goals is
to see if something can be done to improve the situation (digital-to-frequency
converter, the counterpart of digital-to-analog Converter). In this effort, two
important mathematical tools are used: Number Theory and Fourier Analysis.
During this process of reasoning and learning from several “beautiful minds,”
I am amazed at the power and the striking beauty of mathematics. I am deeply
touched by the mysterious harmony rooted in our number system. In this
book, I want to share this joy with reader.
PLAY TIME AS WE PLAY LEVEL

The entire VLSI circuit design business is built on the fact that we use level (voltage or current level) to represent information. In analog processing, level is organized in multiple elevations. In the digital domain, it is in binary fashion. As process technology advances, some momentous changes emerge: the transistor is switching faster and faster, and the supply voltage is reduced lower and lower. Consequently, time (or rate-of-switching) becomes an attractive option to represent information. This will unquestionably influence the way that we design circuits. In this book, a million-dollar question is asked: “Can we play time as we play level?”

This book is organized in the following way:

Chapter 1 discusses how the clock signal is used in all electronic applications. The aim of this chapter is to understand our targeting problem in depth. Chapter 2 briefly reviews the existing clock generation techniques. This chapter focuses on the explanation of how this problem is conventionally dealt with. Chapter 3 looks at the root of the clock problem. It investigates the very concept of frequency and introduces the breakthrough viewpoint that leads us on an entirely new path. Chapter 4 presents the supporting technology, flying-adder architecture, which implements this new concept into circuitry. This is the hardware implementation of this novel approach introduced in chapter three. Based on the time-average-frequency concept and the flying-adder circuit, Chapter 5 coins a new device: the digital-to-frequency converter. Chapter 6 shows some examples of using this innovative technology to build cheaper, faster, and better systems. It illustrates the strength of this new technology. Chapter 7 is the visionary discussion of using “time” for signal processing. It brings forth new directions for future chip design. Its goal is to inspire the next generation researcher and engineer with new opportunities.

This book was inspired by Stay Hungry, Stay Foolish, which I second from the bottom of my heart. This mindset is the invisible hand that has created our magnificent civilization out of the void. It will serve as the lighthouse to guide us in the journey of seeking the ultimate paradise. It is my wish that this book can play a role in achieving the goal of designing “cheaper, faster, and better” electronic products that will ultimately make for a more enjoyable life.

I would like to thank my dear wife, Zhihong You, for supporting me in the completion of this book. Without her selfless effort, this book would never have been published. She has always stood beside me through both “thick and thin.” As a fellow professional who works in similar area and was trained in the same schools, her gifted mental might is highly respected by me. Fortunately, it appears that her exceptional competence has been passed to our lovely daughters Katherine and Helen. I also want to thank Katherine Xiu for helping me in English proofreading and in creating the index.

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CHAPTER 1

CLOCK SIGNAL IN ELECTRONIC SYSTEMS

1.1 THE SIGNIFICANCE OF CLOCK SIGNAL

1.1.1 Clock Signal

In modern electronic-driven society, our everyday lives are supported by various kinds of electronic devices. At home, TV, computer, audio system, game machine, and digital camera are indispensable for our entertainment and relaxation. Away from home, mobile phones keep us connected with the world all the time. On the road, automobiles and airplanes with countless built-in electronic devices make them safe to be driven/flown and comfortable to ride in. At work, we spend most of our time dealing with the computer, fax machine, copier, printer, projector, etc. Without these electronic devices, people’s lives would be totally different; human society would regress many years in standard of living. Electronic devices have already penetrated into all aspects of our lives.

When in operation, almost all electronic devices rely on a very important signal: the clock. This is simply due to the fact that electronic devices are made of very-large-scale-integration (VLSI) chips, which are primarily designed on the synchronous principle. For any chip, simple or complex, its designed functionality is achieved by millions of events that occur inside it. These events do not happen randomly but in a predetermined, orderly sequence. The clock signal is the conductor of the orchestra to produce harmony. For successful
operation in a large chip, many clock signals (as many as hundreds) could be required simultaneously. Usually, phase-locked loop (PLL) is used on-chip to generate these crucial clock signals. If a VLSI chip could be treated as a person and the on-chip processor were regarded as the brain, then the clock pulse is the heartbeat, the clock signal is the blood, and the clock distribution network (clock tree) is the vessel. This analogy is graphically demonstrated in Fig. 1.1.

In the field of VLSI circuit design, the clock signal is an electrical pulse train of square waveform as shown in Fig. 1.2. It has two distinguishable voltage levels: high and low. The basic unit in this pulse train comprises one occurrence of high level voltage and one occurrence of low level voltage. The transitions between the low-to-high and high-to-low are termed the clock edges. They are called “rising edge” and “falling edge,” respectively. The length-in-time used by this basic unit is defined as the clock period; its inversion is the frequency that is often used by people to gauge the working speed of an electronic device.

One of the most important characteristics of the clock signal is that the basic unit, often called the cycle, has to be able to repeat itself indefinitely.

Fig. 1.1. The importance of clock pulses: they are the heartbeats.

Fig. 1.2. Clock signal is an electrical pulse train.
In other words, in this pulse train, every cycle has to be exactly the same. This is because that clock signal is the driver of the chip. The billions of operations (can also be viewed as events) inside a VLSI chip are all coordinated by clock signal. Structurally, the circuit inside the chip is designed in such way that these operations are triggered by either the rising edge or the falling edge, or both, of the clock signal. Therefore, it is essential that the occurrences of these edges in time are precisely predictable. The easiest way of achieving this goal is to make every cycle the same. A clock signal with this predictability in its waveform has enabled an important VLSI circuit design method: synchronous design. The synchronous design methodology is a milestone technology that allows the VLSI chip design industry to make great strides.

The physical medium inside the electronic circuit is electrical voltage or current. The electronic circuit is naturally suitable for handling the magnitude of this medium. (In all VLSI chips, information is represented through the magnitude of this medium.) By manipulating the magnitude, VLSI chips can process information and produce result for us to use. Manipulating the medium’s magnitude for representing information is natural for an electronic circuit, since magnitude is directly proportional to the number of electronics flowing inside electronic devices. On the other hand, an electronic circuit is not naturally born for managing the other important variable: time. Instead, electronic systems use voltage transition to represent timing information. Therefore, it is not an easy task to generate the period of the basic unit (clock cycle) any way you want. It usually requires external help of a timing reference source, such as a mechanical crystal oscillator. Then, a special circuitry of PLL is used to produce other time scales based on this precise reference. This field of work is called frequency synthesis, and it is one of the most actively researched and engineered areas in VLSI circuit design.

1.1.2 The Aim of This Book

Due to the difficulty of using electronic circuits to manipulate the time scale, the capability of PLLs is limited. In many cases, it is extremely difficult and costly for the clock circuit design engineer to produce the clock frequencies that the system engineer prefers. Most of the time, the system engineer has to use whatever frequencies the PLL circuit designer is able to offer. Moreover, when a PLL is used as the clock source, it is difficult to switch from one frequency to another in a short time (a short time in comparison to the clock period). Consequently, these problems have limited our options for designing better and cheaper electronic products.

Throughout the history of frequency synthesis development, there are three distinguished approaches: direct analog synthesis, direct digital frequency synthesis (DDFS), and PLL-based indirect frequency synthesis. Among these, the PLL-based method is the most popular one for on-chip clock generation. There are several styles in the PLL-based approach:
integer-N PLL, fractional-N PLL, sigma-delta fractional-N PLL, and all digital PLL (ADPLL). All the aforesaid techniques are built around one basic consensus: constructing the clock waveform with equal lengths in time for all the cycles. In other words, the basic unit of the clock waveform is repeatable; all the units have to be exactly the same. This feature is ideal for the clock that is being used as the driver signal for chip operation because the location in time of every edge is precisely predictable. Unfortunately, this is also the single most influencing factor that makes the task of clock generation (frequency synthesis) difficult.

History shows that major science and technology advancements often start with adventurous thinking. Breakthroughs usually happen when traditional thinking is detoured. Moreover, most of the time, crucial advancement is initialized at the conceptual level. After a long period of time sticking with the belief that “all cycles shall have same length-in-time,” it is worth focusing our attention back to the two fundamental issues:

1. **In the field of electronic circuit design, what does frequency mean?**
2. **In circuit design practice, how is the clock signal used?**

The process of searching the answers for these two questions has induced the formal introduction of the time-average-frequency concept (Xiu 2008a). This rigorously formed concept lays down the foundation for a new frequency synthesis technique: flying-adder direct period synthesis architecture. Together, time-average-frequency and flying-adder architecture are the two cornerstones of a new circuit component: digital-to-frequency converter (Xiu 2008b). These breakthrough innovations, as illustrated in Fig. 1.3, are the focus of this book.

**Fig. 1.3.** Time-average-frequency, flying-adder synthesizer, and digital-to-frequency converter are the focus of this book.
1.2 THE CHARACTERISTICS OF CLOCK SIGNAL

The clock signal used in electronic system has two functional characteristics: frequency and phase. It also has one quality-related characteristic: jitter (phase noise). A clock period is defined as the time used by one clock cycle. The frequency, which is the mathematical inverse of the period, is used to describe the number of clock cycles (clock pulses) that exist in the time frame of 1 second. In modern synchronous design practice, all the events that happen inside a chip are triggered by either the rising edge or the falling edge, or both, of the clock pulses. Therefore, frequency determines the number of operations carried out within 1 second. It is the gauge of chip speed. For example, a CPU running at 2 GHz has 2 billion clock pulses within 1 second. Consequently, there will be 2 billion coordinated operations that occur within 1 second. Frequency is the most important characteristic of the clock signal. When more than two clock signals exist in a system and interact with each other (through the data they drive), in addition to their frequencies, the relative positions of their functional edges are of interest to system designer as well. This relative position is represented through a parameter called the clock phase. The precision associated with the position of the clock’s functional edge is qualified by another parameter of jitter.

1.2.1 Jitter and Phase Noise

1.2.1.1 “Jitter” is Used to Describe the Clock Edge Uncertainty The term “jitter” is used to describe the nonidealness of the clock edges’ positions in time. Ideally, all clock edges shall occur in precisely determinable positions when both the frequency and the initial position are given. Their positions should be mathematically traceable. However, in real practice, the implementation of clock generation circuit (e.g., a PLL) inevitably has some imperfections. This results in some degree of uncertainty in the position of the clock edges, as illustrated in Fig. 1.4. People use the term “jitter” to quantitatively describe the degree of this uncertainty.

1.2.1.2 Timing Error is Caused by Voltage Noise An electrical circuit is naturally suitable for representing information by using magnitude (voltage or current). Timing information is not inherently attached to the electrical circuit. In circuit practice, timing information is converted from voltage or current. Clock signals with edge uncertainty are shown in Fig. 1.4.
current transient events. As shown in Fig. 1.5, the “time” in an electronic circuit is represented by the moment at which the voltage crosses a predefined threshold. In a synchronous system, jitter is the deviation of clock edges from their ideal positions. It is a form of noise, since any voltage noise that corrupts the waveform will be converted proportionately into a timing error, as also shown in Fig. 1.5. This edge fluctuation usually is a random process and must be characterized in terms of its statistics (mean value, standard deviation, confidence level, etc). There are many terminologies used in the literature to describe this clock edge uncertainty: period jitter, absolute jitter, cycle-to-cycle jitter, long-term jitter, accumulated jitter, random jitter, deterministic jitter, root mean square (rms) jitter, peak-to-peak jitter, periodic jitter, total jitter, etc. The fact that so many terms are used for one phenomenon is simply due to the reason that clock edge uncertainty is both an important and complex subject in academic research and engineering practice.

### 1.2.1.3 Look at Clock-Edge-Uncertainty in Time Domain: Period Jitter, Cycle-to-Cycle Jitter, and Time Interval Error

The three most commonly used jitter terms in engineering practice are period jitter, cycle-to-cycle jitter and time interval error (TIE). As depicted in Fig. 1.6, period jitter (P1, P2, P3, etc.) is the simple measurement of the period of each clock cycle.
Cycle-to-cycle jitter measures the degree of the clock period’s changes between any two adjacent cycles. By these definitions, it can be understood that no knowledge of an ideal clock signal is needed when calculating the period jitter or the cycle-to-cycle jitter. On the other hand, the TIE is defined as the measurement of how far each clock edge varies from its ideal position. Therefore, for this measurement, the ideal clock edge position must be known or estimated.

The relationships among the previously defined three jitter terms can be understood from their definitions. Figure 1.7 can help further illustrate the points where a clock signal’s cycle length (period) alternates between two values: $P_{\text{mean}} \pm x$. As implied in their definitions and shown in Fig. 1.7, period jitter is the direct measurement of a clock cycle’s length. It has great significance for digital operation since setup constraint is constructed under the influence of this period jitter. Meanwhile, cycle-to-cycle jitter is the first-order-difference operation to period jitter. It shows the instantaneous dynamic of the clock signal, which is very important to the PLL designer if this clock signal is used as the input of a PLL. The TIE can be regarded as the integrating operation over the period jitter (after each period is first subtracted from the ideal clock period). The TIE is significant because it shows the cumulative effect of the period jitter. It is the long-term characteristic of the clock signal. In summary, period jitter is important to digital design where only the jitter’s static characteristic is of interest. Both cycle-to-cycle jitter and the TIE are important to applications where the jitter’s dynamic characteristic is also critical in determining system performance, such as in clock data recovery (CDR), frequency conversion, and when used as reference.

It is worth mentioning that the term “jitter accumulation” has two completely different meanings when used in different situations. One is related to
the long-term jitter, where period jitter accumulates over many clock cycles (TIE). The other refers to the scenario that a clock signal propagates through multiple circuit stages (such as in a clock tree) and the noise generated at each stage is “added” to the clock signal. In this case, the term “accumulated jitter” is used to represent all the noises that the clock signal picks up along its propagation paths.

1.2.1.4 Distinguish the Jitter: Random or Deterministic? The period jitter, cycle-to-cycle jitter, and the TIE are used to quantitatively describe the clock edge uncertainty. However, these terms do not provide any insight to the causes of the jitter. To better describe the jitter, two additional terms are often used to distinguish the causes of the jitter: “random jitter” and “deterministic jitter.” Further, the sum of random jitter and deterministic jitter is termed “total jitter.” Random jitter is the timing noise that cannot be predicted. It does not have any discernable pattern. The primary source of the random jitter in electrical circuits is the thermal noise, also called Johnson noise or shot noise. It is the electronic noise generated by the thermal agitation of the electron inside the electrical conductor at equilibrium. It always happens regardless of the voltage applied on the circuits/devices. The random jitter bears the characteristic of Gaussian distribution (or normal distribution), which is shown in Fig. 1.8. As shown, this kind of stochastic process can be characterized by two values: the mean \( \mu \) and the standard deviation \( \sigma \). Mathematically, the root mean square (rms) is a statistical measure of the magnitude of a varying quantity: \( x_{\text{rms}}^2 = \mu^2 + \sigma^2 \). Electrical engineers often use the term “root mean square” as a synonym for standard deviation when referring to the square root of the mean squared deviation of a signal from a given baseline (AC-only rms of a signal). Therefore, standard deviation \( \sigma \) of a period jitter distribution (or cycle-to-cycle, TIE) is also called rms jitter. For a Gaussian distribution, one \( \sigma \) away from the mean (baseline) accounts

![Fig. 1.8. Gaussian (normal) distribution. (Courtesy of Petter Strandmark.)](image)

* For a long-term, very slow timing variation, the clock edge’s position uncertainty is often called frequency wander instead of jitter.
for about 68% of the total; three $\sigma$ away account for 99.7%. It is important to recognize that random jitter is unbounded due to the nature of the Gaussian distribution.

Deterministic jitter is the clock edge timing uncertainty that is repeatable and predictable. The root cause of deterministic jitter is usually associated with some traceable sources or events. The magnitude of the deterministic jitter is bounded. Deterministic jitter can further be categorized into periodic jitter, data-dependent jitter, and duty-cycle dependent jitter. Jitter that repeats itself in a cyclic fashion is called periodic jitter, also called sinusoidal jitter. It is typically caused by external traceable noise sources, such as a switching power supply or a local radio frequency (RF) carrier that coupled into the system.

In wired datalink communication, the jitter that correlates with the bit sequence is termed “data-dependent jitter.” It is usually caused by the frequency response of the transportation media (such as cable). Different data sequences result in different electrical waveforms due to the frequency response of the cable or device. These different waveforms introduce timing differences (and hence jitter) when the threshold is crossed. Duty-cycle-dependent jitter is used to differentiate the timing difference caused by either the rising or the falling edge of the waveform. It can be introduced for two reasons: (1) the slew rates of the rising and falling edge are different and (2) the decision threshold for a waveform is either higher or lower than it should be. Data-dependent jitter and duty-cycle-dependent jitter are mostly used in CDR applications to characterize the timing information embedded in the data stream (Tektronix).

### 1.2.1.5 Look at the Clock-Edge-Uncertainty in Frequency Domain: Phase Noise and Spurs

In addition to being studied in the time domain, the timing irregularity of a clock signal can also be investigated from the frequency domain. Phase noise is the frequency domain representation of the rapid short-term fluctuation in the phase of an electrical wave. For a pure sinusoid wave, the signal can be described by the following equation:

$$v(t) = A \cos(2\pi ft)$$  \hspace{1cm} (1.1)

Phase noise is added to this signal by adding a stochastic process represented by $\phi(t)$ in the phase part as shown in Eq. 1.2. This fluctuation in phase (hence phase noise) will cause uncertainty at the exact moment at which this waveform crosses a predefined voltage threshold (jitter). The term “phase noise” is typically used by radio frequency engineers, and the term “jitter” is mainly used by digital engineers, all for the convenience of serving on what they are doing. The two terms are related; they describe the same physical phenomenon from different angles.

$$v(t) = A \cos(2\pi ft + \phi(t))$$  \hspace{1cm} (1.2)
Phase noise is often expressed as the ratio of sideband power in a 1-Hz bandwidth to the signal power, in units of dBc/Hz, at a given offset from the carrier frequency (Poore 2001). It is often measured by using spectrum analyzer. Figure 1.9 is an example of phase noise measurement plot of a 2-GHz clock signal. The x-axis is the frequency offset from the carrier. The y-axis represents the noise strength at that offset frequency. Phase noise can also be expressed as a value integrated over a certain range of the offset frequency. This integrated phase noise can be converted into time domain rms jitter. In this figure, the integrated rms jitter from 20 KHz to 200 MHz is 1.76 ps.

In engineering practice, a histogram is often used to graphically characterize the time jitter. Figure 1.10 is the period jitter histogram of a 2.75-GHz clock signal (refer to Fig. 1.8). The number of samples in this histogram is 1.9 million. The standard deviation $\sigma$ is 2.85 ps, and the peak-to-peak range is 25.6 ps. As expected, this distribution bears approximately a Gaussian-like shape.

The shortcoming of the jitter histogram is that it does not show the temporal order in which the measurements occur. Therefore, it lacks the capability of identifying any repeating patterns that might indicate some deterministic modulation sources. A plot of jitter versus time (jitter–trend plot) can make such patterns visible. This feature can help us identify the sources of the
disturbances. The extension of this jitter-vs-time measurement is to apply fast Fourier transform (FFT) to it. The result, displayed in the frequency domain, is the jitter spectrum. The benefit of jitter spectral analysis is that any periodic components (periodic jitter) embedded in the noise can potentially be distinguished. Hence, the triggering source could be identified. Figure 1.11 shows one such jitter spectrum plot. Clearly, there is a 15-KHz fundamental

* Borrowed from Tektronix.
frequency in the noises. The second (30 KHz), and third (45 KHz) harmonics can also be seen easily. This suggests that a 15-KHz nearby signal could be coupled into the clock signal.

Another very important method used by circuit designers for studying clock signal quality is to directly perform FFT on a clock signal waveform. Figure 1.12 is an example of the FFT result performed on a 1.92-GHz clock. Clearly, the clock energy is concentrated at 1.92 GHz as designed. The spurious tone at the 12-MHz offset is an indication that there is a signal of 12 MHz modulating the 1.92-GHz clock. Indeed, in this case, the 12 MHz is the reference clock for the PLL. Clearly, it leaks to the output through the PLL.

1.2.1.6 Sources of Jitter From a solid-state physics point of view, all the voltage noises that occur inside a circuit can be traced back to thermal noise and 1/f flicker noise. From a system perspective, there are two types of systems that bear unique jitter characteristics. The first type is the autonomous system, which can oscillate on its own. The jitter associated with those systems accumulates. There is no inherent force that counteracts the wander tendency of its oscillating frequency. It has the characteristics of frequency modulation (FM jitter). In a typical PLL system, the input oscillator and the VCO (voltage control oscillator) are autonomous components. The other type is the driven system, which can only be activated by outside signals. Its edge uncertainty has a reference point. It syncs with the driving signal, and hence the jitter does not accumulate. This kind of behavior bears the phase modulation characteristic (PM jitter). The dividers and phase detector inside a PLL belong to this category.
When an electronic system is investigated as a whole, components that can contribute to total jitter though jitter accumulation are as follows:

- all transistors used in the circuit
- all passive components (resistor, capacitor, and inductor) used in the circuit
- random thermal and mechanical noise from crystal
- parasitic components from signal interconnections (within the integrated circuit [IC])
- trace, cable, and connector used in the printed circuit board (PCB) level.

### 1.2.1.7 Summary

Table 1.1 lists all the methods for studying clock quality. They are different ways of looking at the same thing: clock edge uncertainty. Digital designers prefer to use the term “jitter” while RF designers typically use the term “phase noise.” They are related and can be converted to/from each other. When clock edge uncertainty is caused by stochastic processes, its distribution in the time domain histogram is Gaussian-like. In the frequency domain, it raises the noise floor. When clock edge uncertainty is sourced from periodic events, spur (spurious tones) appear in its frequency spectrum. In the time domain, its histogram will deviate from Gaussian distribution because of those periodic events.

### 1.2.2 Clock Phase

When a clock signal is used to drive an analog-to-digital converter (ADC), another clock characteristic called clock phase is important. An example is shown in Fig. 1.13. In this system, an analog signal and a clock signal are transmitted from transmitter to receiver through different cables. Thus, they experience different delays. Moreover, the analog signal is originated from a digital-to-analog converter (DAC). There is an area of overshoot and ringing within each data boundary. Clearly, on the receiving side, the exact moment at which the ADC takes the sample has great impact on the value converted. It is desirable that some tuning capability is available inside the receiving side’s clock circuitry so that the position of the clock edge that will trigger the ADC can be adjusted. Within such a system, the exact sampling moment is called the clock phase, as illustrated in Fig. 1.14. In this scenario, phase is proportional to time. Different phases correspond to different time delays from a reference point. In many such systems, there could be 4, 8, 16, or 32 phases available within one clock cycle to help achieve the optimal result.

Clock phase is also important in digital communication when data are moved between blocks, modules, and chips. In such applications, information is exchanged between different domains, and each domain has its own clock. The relative position of the clock edges, which is represented using the clock phase of one of the involved clocks, plays a crucial role in the success of the data transfer. Examples include double data rate (DDR) memory interface,
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