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Yan Li
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3D Microelectronic Packaging

From Fundamentals to Applications

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Editors
Yan Li
Intel Corporation
Chandler, AZ, USA

Deepak Goyal
Intel Corporation
Chandler, AZ, USA

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Contents

Contributors

Liangbiao Chen Department of Mechanical Engineering, Lamar University, Beaumont, TX, USA

Paul Conway The Wolfson School of Mechanical, Electrical and Manufacturing Engineering, Loughborough University, Loughborough, Leicestershire, UK

Indranath Dutta School of Mechanical and Materials Engineering, Washington State University, Pullman, WA, USA

Xuejun Fan Department of Mechanical Engineering, Lamar University, Beaumont, TX, USA

Amlan Ganguly Computer Engineering Department, Rochester Institute of Technology, Rochester, NY, USA

Deepak Goyal Intel Corporation, Chandler, AZ, USA

Ran He The University of Tokyo, Tokyo, Japan

Zhiheng Huang School of Materials Science and Engineering, Sun Yat-sen University, Guangzhou, China

Tengfei Jiang Department of Material Science and Engineering, University of Central Florida, Orlando, FL, USA

Satish G. Kandlikar Mechanical Engineering Department, Rochester Institute of Technology, Rochester, NY, USA

Praveen Kumar Department of Materials Engineering, Indian Institute of Science, Bangalore, India

Sangil Lee, Ph.D. Invensas Corporation, San Jose, CA, USA

Menglu Li Department of Materials Science and Engineering, University of California, Los Angeles (UCLA), Los Angeles, CA, USA

Yan Li Intel Corporation, Chandler, AZ, USA

Kwang-Lung Lin Department of Materials Science and Engineering, National Cheng Kung University, Tainan, Taiwan, R.O.C.

Pilin Liu Intel Corporation, Chandler, AZ, USA

Yingxia Liu Department of Materials Science and Engineering, University of California, Los Angeles (UCLA), Los Angeles, CA, USA

Ravi Mahajan High Density Interconnect Pathfinding, Assembly Technology, Intel Corporation, Chandler, AZ, USA

Antonio La Manna IMEC Consortium, Leuven, Belgium

Erasenthiran Poonjolai Intel Corporation, Chandler, AZ, USA

Bob Sankman High Density Interconnect Pathfinding, Assembly Technology, Intel Corporation, Chandler, AZ, USA

Hualiang Shi Intel Corporation, Chandler, AZ, USA

Songhua Shi Medtronic, Tempe, AZ, USA

Tadatomo Suga The University of Tokyo, Tokyo, Japan

Peter Tortorici Medtronic, Tempe, AZ, USA

K. N. Tu Department of Materials Science and Engineering, University of California, Los Angeles (UCLA), Los Angeles, CA, USA

George Vakanas Intel Corporation, Chandler, AZ, USA

Paul Vianco Sandia National Laboratories, Albuquerque, NM, USA

Yaodong Wang Department of Materials Science and Engineering, University of California, Los Angeles (UCLA), Los Angeles, CA, USA

Luhua Xu Intel Corporation, Chandler, AZ, USA

About the Authors

Deepak Goyal graduated (Ph.D.) from State University of New York, Stony Brook, and joined Intel as a Failure Analysis Engineer. He is currently the Technical Leader of the Assembly and Test Technology Development (ATTD) Failure Analysis Labs at Intel, supporting the materials and failure analysis of all assembly technology development at Intel and developing the next generation of analytical tools and techniques. He is an expert in the failure analysis of packages and has taught Professional Development courses on Package FA/FI and failure mechanisms at the ECTC from 2003 to present. He has won two Intel Achievement Awards and around 25 Division Recognition Awards at Intel. He has around 50 publications and has been awarded three patents and has ten patents filed. He was the chair of the Package and Interconnect Failure Analysis Forum sponsored by the International Sematech. He is a senior member of the IEEE. He has coauthored a chapter titled "Applications of terahertz technology in the semiconductor industry" in the *Handbook of Terahertz Technology for Imaging, Sensing and Communications*, 2013. He has also coauthored and edited two chapters for a book titled *Characterization and Metrology for Nanoelectronics and Nanostructures*, which will be published in November 2016.

Yan Li is currently a senior staff packaging engineer in the Assembly Test and Technology Development Failure Analysis Lab of Intel Corporation located in Chandler, Arizona. She joined Intel in 2006, and her work focuses on the quality and reliability of electronic packages, fundamental understanding of failure modes and failure mechanisms of electronic packages, and developing new tools and techniques for fault isolation and failure analysis of electronic packages. Yan received her Ph.D. in materials science and engineering from Northwestern University in 2006 on studies related to the synthesis and characterization of boron-based nanowires and nanotubes. She is actively involved in professional associations, such as Minerals, Metals and Materials Society (TMS), American Society for Metals (ASM) International, and Electronic Device Failure Analysis Society (EDFAS), serving as conference organizers and session chairs for more than 5 years.

Chapter 1
Introduction to 3D Microelectronic Packaging

Yan Li and Deepak Goyal

1.1 Introduction

Microelectronic packaging is the bridge between the Integrated Circuit (IC) and the electronic system, which incorporates all technologies used between them [1]. Advanced 3D microelectronic packaging technology is the industry trend to meet portable electronics demand of ultra-thin, ultra-light, high performance with low power consumption. It also opens up a new dimension for the semiconductor industry to maintain Moore's law with a much lower cost [1–3].

A wide variety of real products assembled by the advanced 3D packaging technology have been unveiled in the recent years. For example, the Apple A7 inside the iPhone 5S, introduced in September 2013, is a 3D package with Package on Package (POP) configuration [4]. As displayed in Fig. 1.1, the wire bond Elpida (now Micron) memory (low power double data rate type-3 (LPDDR3) mobile random access memory (RAM)) package is stacked on top of the Apple A7 flip-chip package to achieve better performance with smaller form factor. In early 2014, SK Hynix announced its high bandwidth memory (HBM) products having higher bandwidth, less power consumption, and substantially small form factor, achieved by stacking up to eight DRAM dice interconnected through Through Silicon Vias (TSV) and micro-bumps [5]. In July of 2015, AMD introduced the AMD Radeon™ Fury graphics cards, the first Graphic Processing Unit (GPU) to implement HBM by TSVs and micro-bumps [6]. Figure 1.2 shows a top-down and schematic cross-sectional view of the advanced 3D package. The big GPU die is integrated into the Si interposer along with four HBM memory stacks by micro-bumps and TSVs to ensure faster and shorter connection between chips [6]. These real products bring

Y. Li (✉) • D. Goyal
Intel Corporation, Chandler, AZ, USA
e-mail: yan.a.li@intel.com

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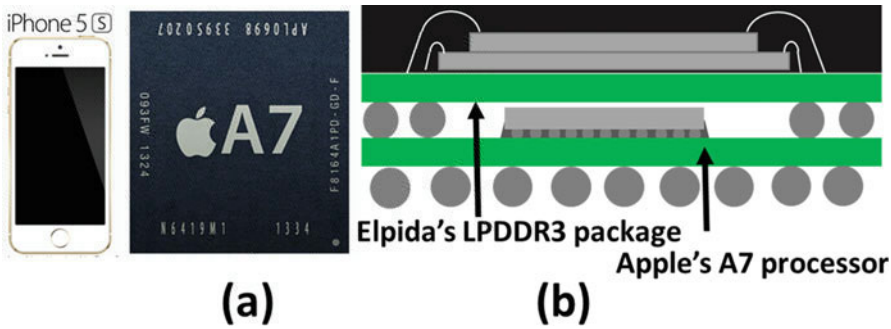

Fig. 1.1 POP inside iPhone 5s. (**a**) Top view of the Apple A7 package, (**b**) schematic of the cross-sectional view (not in scale), (adapted from Ref. [4])

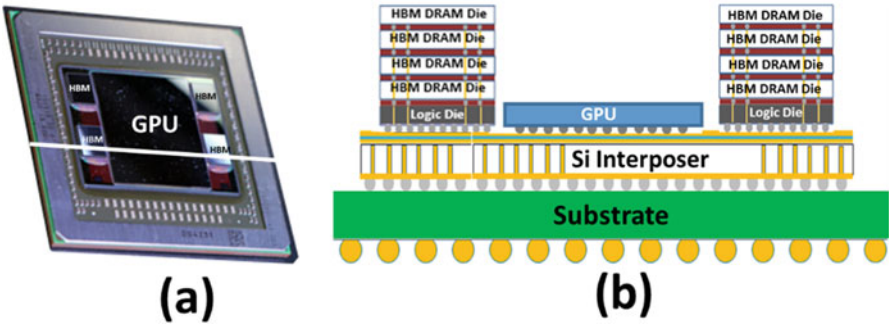

Fig. 1.2 Top view (**a**) and schematic cross-sectional view (not in scale), (**b**) of the AMD Radeon™ Fury. The big GPU die is integrated into the Si interposer along with four HBM memory stacks by micro-bumps and TSVs (adapted from Ref. [6])

the 3D packaging techniques from paper to reality and indicate the extensive applications of 3D packaging technology to microelectronics.

3D packaging technology involves multiple disciplines, for example, materials science, mechanical engineering, physics, chemistry, and electrical engineering. A technical book, which could provide a comprehensive scope of 3D microelectronic packaging technology is desirable for graduate students and professionals in both academic and industry area. Current available books on 3D integration typically focus on processing of wafers, especially TSV fabrication, and do not cover other key elements in 3D packaging. This book is proposed to fill in the gap. It presents a thorough extent of 3D packaging, covering the fundamentals of interconnects, bonding process, advanced packaging materials, thermal management, thermal mechanical modeling, architecture design, quality and reliability, and failure analysis of 3D packages, which are critical for the success of advanced 3D packaging.

This chapter provides detailed illustration of motivations as well as various architectures of 3D packaging. Challenges in 3D packaging, including fabrication,

assembly, cost, design, modeling, thermal management, material, substrate, quality, reliability, and failure analysis, are reviewed with brief introduction to the chapters addressing these challenges.

1.2 Why 3D Packaging

1.2.1 Moore's Law

Since Intel introduced the world's first single-chip microprocessor, the Intel 4004, in 1971, an exponential growth of ICs has been observed following Moore's law in terms of transistor number per chip [7]. As illustrated in Fig. 1.3, the number of transistors per Si chip doubles approximately every 18 months, resulting in a straight line on a log scale [7, 8]. In 1990, the bipolar transistor technology switched to CMOS in order to reduce thermal power, circuit size, and manufacturing costs, at the same time increase the operating speed and energy efficiency [3]. In the early 2000s, multi-core processors were developed to address the challenging thermal power issue in conventional single-core processors [3]. Since multi-core processors require enormous cache capacity and memory bandwidth to achieve the designed performance, 3D packaging becomes one of the viable solutions to provide the required cache and bandwidth with a relatively low cost [3].

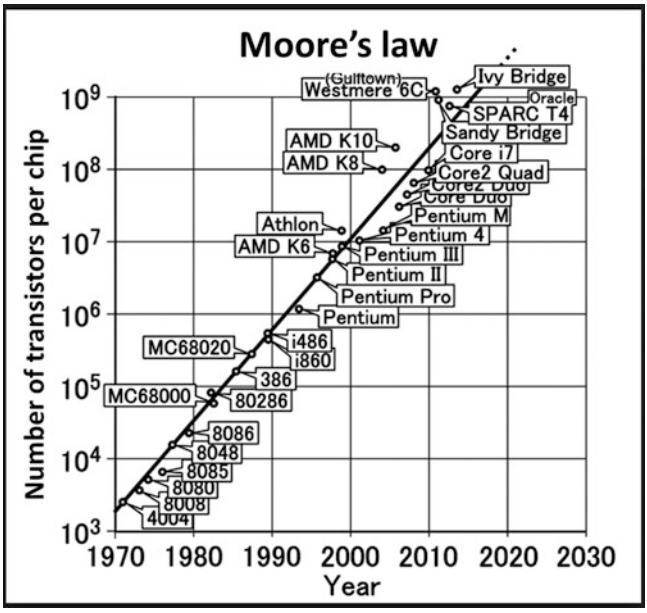

Fig. 1.3 Moore's law predicts the exponential growth of ICs since 1970s (adapted from Ref. [8])

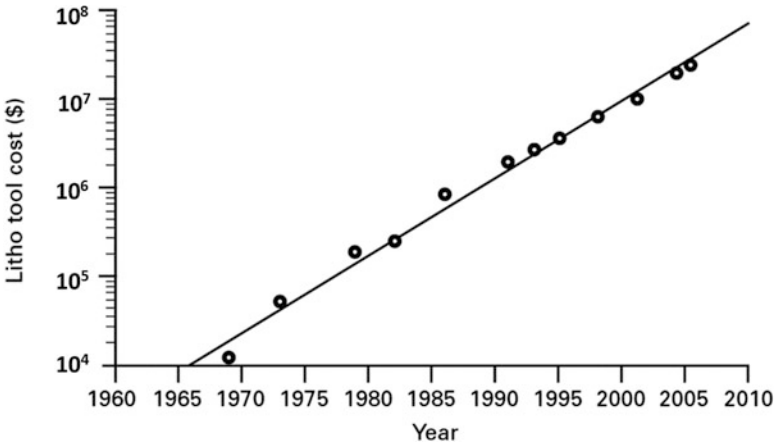

Fig. 1.4 The exponential growth of lithography equipment cost since 1970s (adapted from Ref. [8])

The conventional method to maintain Moore's law is to decrease the dimensions of components by lithography, which is becoming more and more sophisticated and expensive [8]. Figure 1.4 illustrates the exponential growth of lithography equipment cost since 1970s, which presents an economic challenge as the capital cost rises faster than semiconductor industry revenue [8]. 3D integration technology, which has been recognized as an enabling technology for future low cost ICs, provides the third dimension to extend Moore's law to ever higher density, more functionality, better performance with lower cost [3].

1.2.2 Small Form Factor Requires 3D Packaging

Market demands of small form factor microelectronics head to 3D packages, which are ultra-light, ultra-thin, and with small chip footprint. Si chips in 3D packages are typically 50–100 μm thick, about 90 % thinner compared with those in conventional packages. Substrate core thickness of 3D packaging is about 0–100 μm, more than 90 % thinner than that of traditional packaging. High density interconnects in 3D packaging are on the order of 5–20 μm in diameter, more than 90 % smaller than those in 2D packaging. Thus, tremendous reduction in size and weight could be achieved by replacing conventional packaging with 3D technology [2].

Small form factor requires small chip footprint, which is defined as the printed circuit board area occupied by the Si chip, as illustrated in Fig. 1.5 [2]. By stacking multiple dice on top of each other using 3D packaging techniques, the chip footprint could be reduced dramatically. Figure 1.5 schematically demonstrates the difference between conventional 2D packages and 3D packages

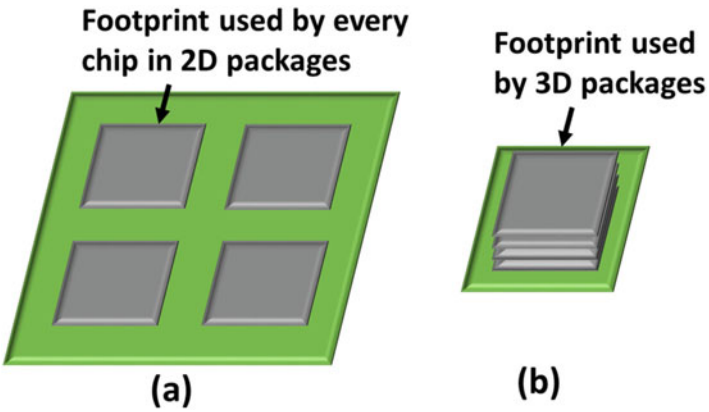

Fig. 1.5 (**a**) Schematic illustration of the footprint difference between conventional 2D packages (**a**) and 3D packages (**b**) (adapted from Ref. [2])

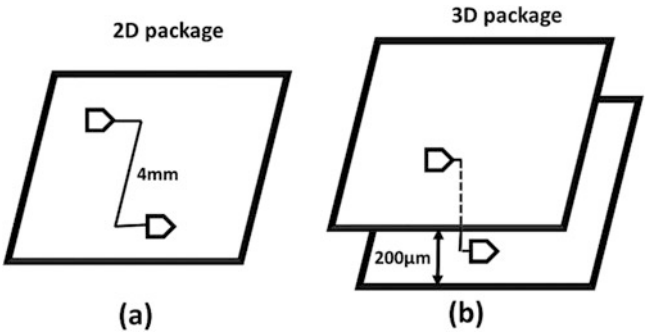

Fig. 1.6 Schematic comparison between the wiring length in 2D packages (**a**) and 3D packages (**b**) (adapted from Ref. [2])

1.2.3 Improved System Performance with Reduced Power

Interconnect length in 3D packages can be significantly reduced compared with conventional 2D packaging [2]. Figure 1.6a shows a typical interconnect length of 4 mm in a 2D package. The interconnect length could be reduced to 200 μm in a 3D package as demonstrated in Fig. 1.6b. Additionally, 3D packaging can also greatly improve the interconnect usability and accessibility [2]. Figure 1.7 shows a comparison between 2D and 3D packaging in terms of the accessibility and usability of interconnection. In contrast to eight neighbors to the center element in the case of 2D packaging technology, the utilization of a 3D packaging configuration provides access to 116 neighbors within an equal interconnect length to a center element in the stack.

The significant decrease in interconnect length as well as dramatic improvement in interconnect usability and accessibility result in much less delay in 3D devices, which is primarily limited by the time taken for the signal to travel along the

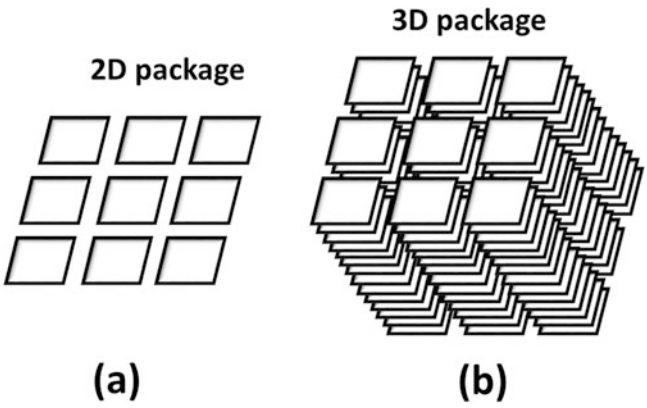

Fig. 1.7 Schematic comparison between 2D packages (**a**) and 3D packages (**b**) in terms of the interconnect accessibility and usability (adapted from Ref. [2])

interconnects [2]. Low latency and wide buses in 3D microelectronic systems lead to significant improvement to the system bandwidth [2]. Noise in well-designed 3D microelectronic systems, including reflection noise, crosstalk noise, simultaneous switching noise, and electromagnetic interference, can be reduced as a result of the reduction of interconnection length [2]. Additionally, as the parasitic capacitance in microelectronic packages is proportional to the interconnection length, the total power consumption in 3D packages is also reduced because of the reduced parasitic capacitance [2]. The power saving achieved by 3D technology enables 3D devices to perform at a faster rate or transition per second (frequency) with less power consumption. The overall system performance is greatly improved by applying 3D packaging technology [2].

1.3 3D Microelectronic Packaging Architectures

The various 3D packaging architectures could be divided into the following three categories: die-to-die 3D integration, package-to-package 3D integration, and heterogeneous 3D integration combining both package and die stacking [3, 9, 10]. Chapter 2 discusses different 3D packaging architectures in detail along with assembly and test flows.

1.3.1 Die-to-Die 3D Integration

Die-to-die 3D integration is enabled by through silicon via (TSV) interconnections and thinned die-to-die bonding [3]. As illustrated in Fig. 1.8, two memory dice are stacked on top of a logic die with TSVs and micro-bumps. First Level Interconnect

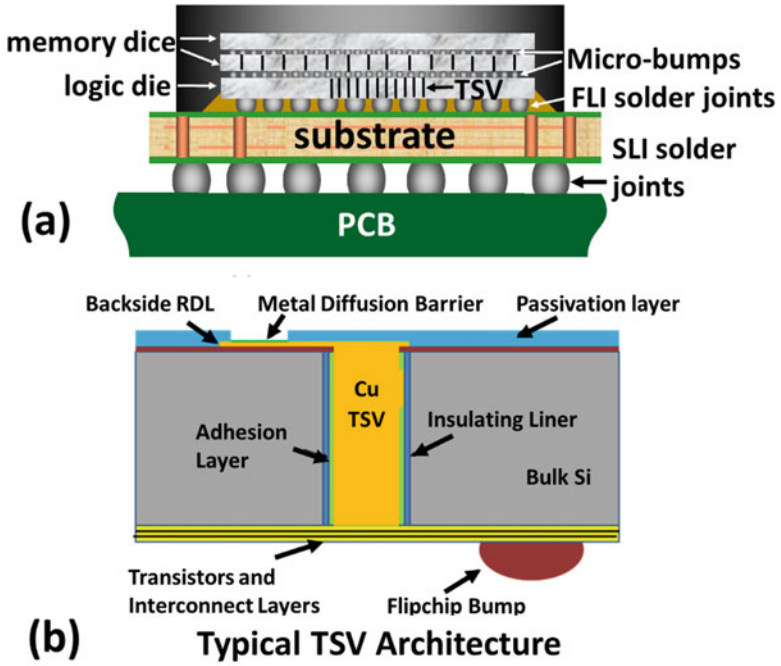

Fig. 1.8 Schematic illustration of die-to-die 3D integration enabled by TSV and thinned die-to-die bonding (adapted from Ref. [10])

(FLI) solder joints connects the logic die with the substrate, while Second Level Interconnect (SLI) solder joints provides the connection between this 3D package to the Printed Circuit Board (PCB) [10]. The TSVs are formed by laser drilling or deep reactive ion etching, followed by liner deposition and copper fill. There are three typical manufacturing processes for TSVs, Via First, Via Middle, and Via Last [11–13]. The detailed process flow of each process as well as the Pros and Cons of each process are discussed in Chaps. 2 and 3.

Die-to-die bonding is implemented by either Thermal Compression Bonding (TCB) process for solder micro-bumps or other alternative bonding process, for example, Cu-Cu bonding. Conventional solder mass reflow process in 2D packages, which includes flux dispensing, die attaching, and solder reflow in ovens, is not able to assemble advanced 3D packages having much thinner dice and organic packages, along with much smaller and denser interconnects. As the extent of warpage from both dice and substrates at the reflow temperature overcomes solder surface tension, leading to die misalignment, and results in die tilting, solder joint non-contact opens, and solder bump bridging [14]. TCB bonding process is developed to replace the conventional solder mass reflow process for solder-based micro-bump assembly in 3D packages. As illustrated schematically in Fig. 1.9, the substrate with pre-applied flux is kept flat on hot pedestal under vacuum to eliminate the substrate warpage. The die is picked up by the bond head, secured and kept flat with vacuum

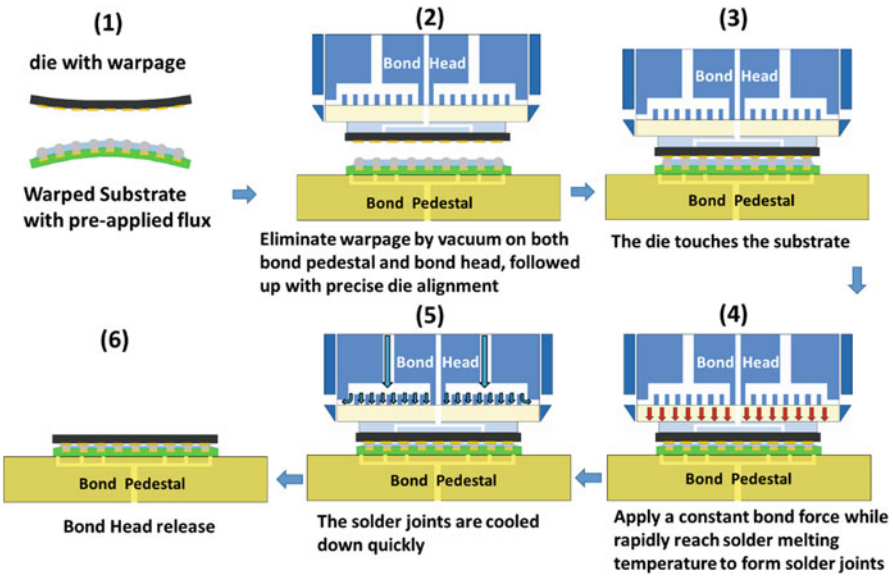

Fig. 1.9 Schematic illustration of a typical thermal compression bonding process (adapted from Ref. [14])

to remove any incoming die warpage. After the die is precisely aligned to the substrate, the bond head with die touches the substrate. A constant bond force is then applied on the die through the bond head, while the die is heated up rapidly beyond the solder melting temperature, with a ramping rate higher than 100 °C/s. As soon as the solder joints melt, the die is moved further down to ensure all the solder joints are at the same height. The die is held in this position long enough so that the solder joint forms between the die and the substrate. While the solder is still in the molten state, the bond head with die could retract upwards to control the solder joint height. Subsequently, the solder joints are cooled abruptly below the solidus temperature, with a cooling rate of more than 50 °C/s, followed up with die release from the bond head [14]. Unlike the traditional solder mass reflow process, with up to 10 min of process time for units in batches, the TCB bonding process assemble units one by one with about a couple of seconds per unit [14]. Additionally, thermal ramping rates during both the heating and cooling cycles are much higher than the conventional method. These higher rates result in solder grain size and orientation differences that can affect mechanical properties as detailed in Chap. 7.

Solder-based micro-bumps are more compliant, thus could compensate bump height variations, lack of co-planarity, and misalignment issues during high volume manufacture. However, the TCB process peak temperature needs to be higher than the melting point of solder material, typically in the range of 250–300 °C, which brings more assembly and reliability challenges. Additionally, solder bridging risk gets much higher as bump pitch shrinks from more than 100 μm to less than 40 μm. Alternative bonding process, like direct Cu to Cu bonding, which could address interconnects with

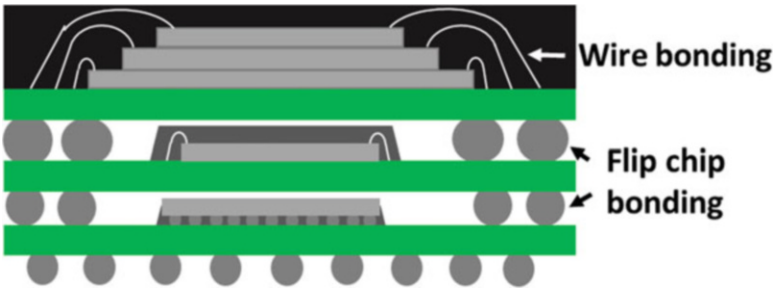

Fig. 1.10 Schematic illustration of package-to-package 3D integration (adapted from Ref. [3])

less than 5 μm bump pitch, and assemble at relatively lower temperature is very promising. Various types of alternative bonding process is reviewed in Chap. 6 as well as Pros and Cons comparing with solder-based TCB process.

1.3.2 Package-to-Package 3D Integration

System in Package (SIP) and Package on Package (POP) are typical configurations of package-to-package 3D integration, which is enabled by stacking packages through wire bonding or flip-chip bonding [3]. Comparing to die-to-die stacking, package-to-package stacking technique has a shorter development cycle, thus help bring products to market faster with a low price. As displayed in Fig. 1.10, a wire bonding package is stacked on top of the other wire bonding package by flip-chip bonding. The two packages are then stacked on a flip-chip package to form a POP. The conventional solder mass reflow process could still be used in package-to-package stacking if the package warpages are within control, and the interconnect size and density is comparable with traditional 2D packages. However, market demands require packages to be ultra-thin, which limit the number of packages that could be stacked together. Additionally, solder joints and package materials in SIP and POP need to go through multiple cycles of reflow, bringing process and reliability challenges, like solder joint open, delamination between multiple layers in packages, and moisture control between each reflow process. Chapter 13 discusses in detail the processing and reliability of stacked packaging technique, as well as the Pros and Cons comparing with die stacking.

1.3.3 Heterogeneous 3D Integration

Depending on product needs, complex 3D packages can have the combination of both die stacking and package stacking [10]. As shown in Fig. 1.11, a 3D Dynamic Random Access Memory (DRAM) package formed by stacking four memory dice

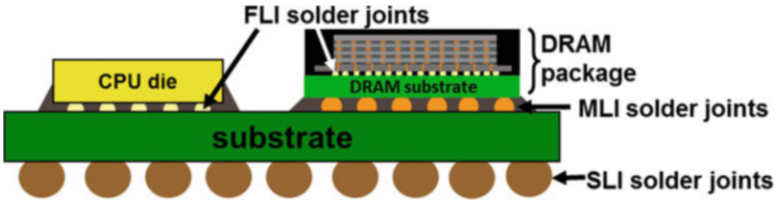

Fig. 1.11 Schematic illustration of 3D packaging architectures having the combination of both die stacking and package stacking (adapted from Ref. [10])

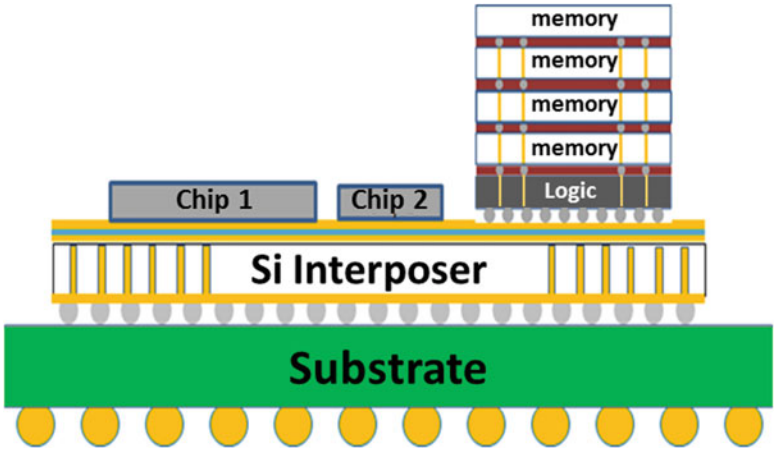

Fig. 1.12 Schematic illustration of Silicon interposer technology providing connection between chips and stacked dice through TSVs (adapted from Ref. [10])

on top of the logic die through TSVs and micro-bumps is integrated along with a flip CPU chip by package stacking. FLIs between the CPU chip and the 3D package, MLIs between the DRAM package and the 3D package, as well as interconnects in the substrate provide connection between the CPU chip and the DRAM package [10]. Smaller and denser interconnects between chips and packages are highly desired for better performance, higher bandwidth, and lower power consumption. Figure 1.12 demonstrates the Silicon interposer technology, which could provide better connection between chips and stacked dice through TSVs [10, 15]. Embedded Multi-Die Interconnect Bridge (EMIB) technology is an alternative approach to provide localized high density interconnects between dice without TSVs [16]. As illustrated in Fig. 1.13, the link between dice is provided by fine Cu interconnects in Si bridges embedded in the organic substrate and confined denser FLIs between Si bridges and chips. Comparing with Si interposer technology, EMIB technology is able to provide similar performance with a much lower cost, thus opens up new opportunities for heterogeneous 3D packaging [16].

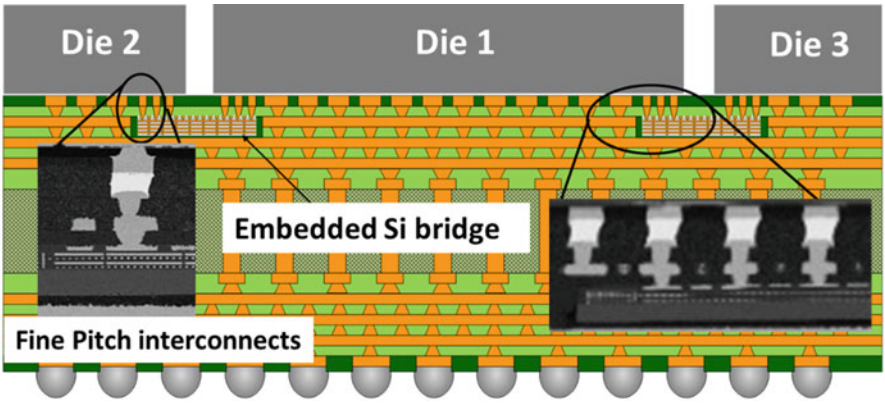

Fig. 1.13 Schematic illustration of Embedded Multi-Die Interconnect Bridge (EMIB) technology providing localized high density interconnects between chips without TSVs (adapted from Ref. [16])

1.4 3D Microelectronic Packaging Challenges

1.4.1 Assembly Process, Yield, Test, and Cost Challenges

3D packaging involves more challenging assembly steps than conventional packaging, such as TSV wafer fabrication and die singulation process (reviewed in Chap. 5), TCB of micro-bumps (discussed in Chap. 7), and multiple solder reflow process for POP (refer to Chap. 13). The complicated process results in yield, test, and cost challenges [2], which could be addressed by redundancy or fault-tolerant designs, throughput time (TPT) improvement of assembly process, and minimize process steps based on product quality and reliability requirement [2], [3].

1.4.2 Thermal Management, Package Design, and Modeling Challenges

The 3D integration of heat generation components in close vicinity increases the heat flux density as well as complexity of coolant routing, thus leads to big challenges to the thermal management of 3D packaging [2, 3]. Chapter 10 presents the fundamentals of heat transfer along with advanced guidelines helpful to address the issue.

Due to the increased system complexity, designing 3D packages could be very challenging, but could be addressed by designing and developing design software [2]. In addition to increased system complexity, 3D packaging involves multilevels of solder joints, underfill, and molding compounds. Thermal stress due to the

mismatch in coefficients of thermal expansion (CTE) and hygroscopic stress caused by excessive moisture absorption are often combined together, which complicates the stress modeling in 3D packaging [17, 18]. For interconnects with a couple of micrometer in diameter, like TSVs, it is found that microstructure, anisotropy of material properties, recrystallization, and time-dependent phase morphological evolution need to be considered during stress modeling [19]. Chapters 4 and 10 provide through discussions on the modeling of thermal mechanical and moisture stresses in 3D packaging.

1.4.3 Material and Substrate Challenges

3D packages typically have smaller interconnect size, tighter bump pitch, and reduced chip gap, which brings challenges to underfill, chip attachment, and deflux process. Additionally, the TCB process widely used in the chip attachment of 3D packages is very different from the conventional mass reflow process, as the whole bonding cycle completes in a few seconds rather than over 10 min [14]. Major modification of traditional underfill and flux material is essential to prevent underfill process, flux residue, and interconnect integrity-induced yield loss, such as underfill voids, delamination because of flux residue, solder bump bridging, or non-wets. Chapter 7 reviews the material challenges and provides guidelines for epoxy and flux material selection.

To enable the highly integrated 3D packaging, both substrate and PCB need to fulfill the much higher signal and power density requirements. Smaller substrate vias, through holes (TH), and traces, along with much tighter pitches are desired. Furthermore embedded components, including both Si chip and packages, integrating into substrates or PCB is one of the approaches to achieve the product miniaturization with higher performance and lower power consumption goal. These results in significant challenges in substrate warpage control and flawless fabrication process to enable much finer interconnect size and pitch. Chapter 11 reviews the substrate material and fabrication technology evolution, along with general recommendations in selecting and applying appropriate material and process technologies for 3D packaging.

1.4.4 Quality, Reliability, and Failure Analysis Challenges

Complex 3D packages have multiscale interconnects ranging from a few to 1000 micrometers. For instance, TSVs and micro-bumps are about a couple of micron in diameters, while the SLI connecting packages to the PCB could be up to 1000 μm in diameter. During 3D integration, interconnects need to go through multiple solder reflow process, defects generated during fabrication and assembly, CTE mismatch between different materials, and microstructure evolution in

interconnects could lead to new quality and reliability issues. Additionally, the extended application of 3D packaging in products requiring much higher reliability, for instance, Advanced Driver Assistance Systems (ADAS), avionics, and high-end servers brings extra challenges to the quality and reliability of 3D packages. Chapters 3 and 4 review the quality and reliability of TSVs. Chapter 9 reviews the electro migration concerns in interconnects of 3D packages. Focusing on the reliability of multilevel solder joints in stacked packages, Chap. 13 explains the different reliability requirements between consumer electronics and high-reliability electronics. It also provides detailed discussions of use conditions, the roles of encapsulants and underfills, reliability tests and modeling to address complex reliability concerns in 3D packages. Chapter 14 provides an overview of quality and reliability of 3D packaging and demonstrates with case studies, along with field performance prediction.

Failure analysis is critical for the technology development of 3D packaging, as in-depth root cause analysis of failures provides solution paths for resolving quality and reliability issues. Due to the complexity of 3D packages, Fault Isolation (FI) and Failure analysis (FA) become very challenging. First of all, multiple failures could exist in one unit post-reliability tests, flawless failure analysis on each failure requires nondestructive high-resolution techniques, including fault isolation, imaging, and material analysis. Additionally, each electrical failure in a 3D package could come from various dice, assembly layers or interconnects, high-resolution fault isolation techniques, which could provide 3D information of defects are highly desired. After the identification of defects, physical failure analysis needs to be performed for the root cause study. However interconnects in 3D packages, like TSVs, have small diameters (2–10 μm) and long lengths (40–200 μm), artifact free cross-sectional techniques with short throughput time is critical for characterizing small defects in a relatively large cross-sectional plane. Chapter 15 reviews advanced high-resolution nondestructive FI and FA techniques, such as Electro Optic Terahertz Pulse Reflectometry (EOTPR), 3D X-ray Computed Tomography (CT), Lock-in Thermography (LIT), and acoustic microscopy. The applications of novel physical sample preparation techniques and various material analysis methods in 3D packaging failure analysis are also discussed. It also provides guidelines for building up efficient 3D packaging FI-FA flow and performing in-depth root cause studies, along with case study demonstration.

1.4.5 Summary

3D packaging has provided a new dimension for semiconductor industry to maintain Moore's law with much lower cost and has been adopted as an effective approach to provide portable microelectronics with better performance, smaller power consumption, and less cost. There has been numerous novel technological innovations invented for the development of advanced 3D packaging in the recent years. However, due to the much smaller and denser interconnects, complicated

assembly process, unique TSV and micro-bump TCB process, and the extended application in high-reliability products, there are tremendous challenges in highly integrated 3D packaging.

Chapters in this book are written by experts from both academia and semiconductor industry. Chapter 2 provides an insightful overview of 3D packaging architecture and assembly process design. Chapters 3, 4, and 5 focus on the fundamentals of TSV processing, reliability, and mechanical properties. Chapters 6 and 7 discuss the fundamentals of thermal compression bonding of micro-bumps, process materials, direct Cu to Cu bonding, and other alternative interconnects in 3D packaging. Chapters 8 and 9 provide fundamentals of solder alloys and electro migration in interconnects of 3D packages. Chapter 10 presents a thorough review of thermal management in 3D packaging. Chapter 11 displays in great details the fundamentals of substrate materials and manufacture process. Chapter 12 covers the thermal mechanical and moisture modeling in 3D packaging. Chapters 13, 14, and 15 illustrate a comprehensive overview of quality, reliability, fault isolation, and failure analysis of advanced 3D packages. Readers could obtain all-around knowledge about 3D packaging, including the fundamentals, developing areas, technique gaps, and guidelines for future research and development.

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Chapter 2
3D Packaging Architectures and Assembly Process Design

Ravi Mahajan and Bob Sankman

Acronyms

2D	Two dimensional
3D	Three dimensional
BEOL	Back end of line
BI	Burn-In
CMP	Chemical mechanical polishing
D2D	Die-to-die
D2W	Die-to-wafer
ECD	Electro-chemical deposition
ECG	Deleted in chapter
EMIB	Embedded multi-die interconnect bridge
FEOL	Front end of line
IP	Intellectual property
KGD	Known good die
KOZ	Keep out zone
MCM	Multi chip module
MCP	Multi chip package
MEOL	Middle end of line
MPM	Multi package module
PECVD	Plasma enhanced chemical vapor deposition
PVD	Plasma vapor deposition
Rx	Receiver
SBS	Side by side

R. Mahajan (✉) • B. Sankman
High Density Interconnect Pathfinding, Assembly Technology, Intel Corporation, MS CH5-157, 5000 West Chandler Blvd., Chandler, AZ 85226, USA
e-mail: ravi.v.mahajan@intel.com; bob.sankman@intel.com

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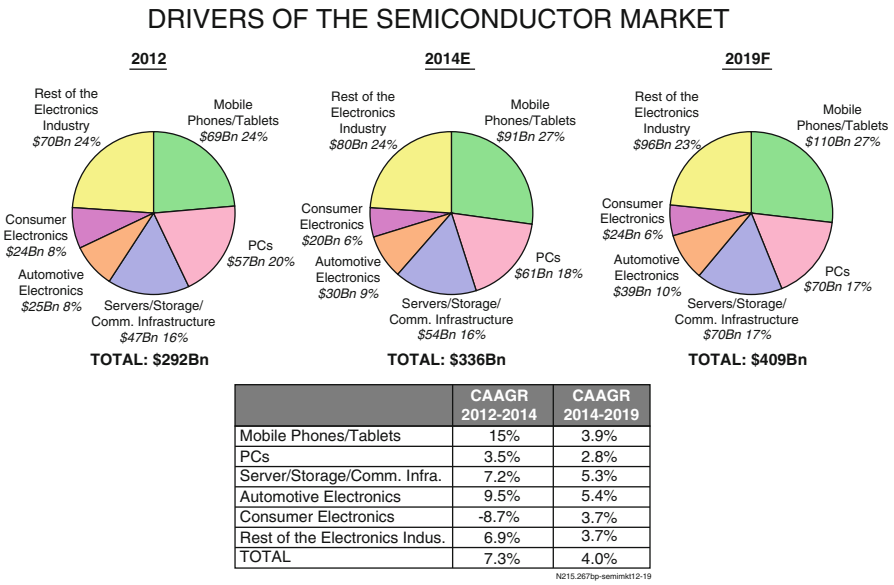
SIP	System in package
SOC	System on chip
TDP	Thermal design power
TIM	Thermal interface material
TSV	Through silicon via
Tx	Transmitter
W2W	Wafer-to-wafer

2.1 Introduction

Increasing transistor density enabled by Moore's Law [1, 2] has led to increasingly powerful and pervasive computer systems that enable multiple personal and business applications (see Fig. 2.1 for an estimate of the overall size and growth trends of the semiconductor market). The trend in increased compute capabilities has been fueled by increased wired and wireless connectivity [3] which has led to powerful interconnected computer networks. These computers and associated networks utilize a myriad of computing and communication functions that are implemented within digital circuits (e.g., Microprocessors, Field Programmable Gate Arrays), memory circuits (e.g., SRAM, DRAM), and analog circuits (e.g., power supplies, clocks, RF front end modules, amplifiers, SERDES, USB, PCIe, DDR). Different computing and communication functions can be integrated on a monolithic silicon chip (typically referred to as System On Chip or SOC integration) or on a package (typically referred to as System In Package or SIP integration[1]). Integration on chip has the advantages of improved signal transmission fidelity due to reduced interconnect lengths, lower system power due to efficient on-chip connections between IP blocks, and overall reduced silicon resulting from Moore's Law scaling. Thus, on-chip integration is usually preferred when:

(a) The integrated functions can easily be implemented on the same silicon fabrication process. For example, digital logic and SRAM can be built using compatible silicon processes. Conversely, high performance digital logic and DRAM are rarely fabricated on similar silicon manufacturing processes, and hence are not commonly included in the same chip.

[1] As a general definition, SIP refers to the on-package integration of multiple heterogeneous and/or homogenous ICs each of which may be in the form of unpackaged die, individually packaged die, or packaged modules. iNEMI (International Electronics Manufacturing Initiative) defines SIP as: *System in Package is characterized by any combination of more than one active electronic component of different functionality plus optionally passives and other devices like MEMS or optical components assembled preferred into a single standard package that provides multiple functions associated with a system or subsystem.* SIP is considered to be subset of the broader concept of System On Package (SOP) [4] where an entire computer system is built on a package.



	CAAGR 2012-2014	CAAGR 2014-2019
Mobile Phones/Tablets	15%	3.9%
PCs	3.5%	2.8%
Server/Storage/Comm. Infra.	7.2%	5.3%
Automotive Electronics	9.5%	5.4%
Consumer Electronics	-8.7%	3.7%
Rest of the Electronics Indus.	6.9%	3.7%
TOTAL	7.3%	4.0%

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Fig. 2.1 Overall size and growth trends of the semiconductor market (Source: Prismark Partners LLC)

(b) The IP[2] blocks desired for the SOC are available in the same silicon fabrication process and the resulting chip meets the cost target required to make the product economically viable.

SIP is preferred for the integration of heterogeneous functions [5] (i.e., functions manufactured using disparate semiconductor technologies) and to help bring products to market quicker when technical and/or business reasons prevent timely SOC integration. As seen in Table 2.1 and Fig. 2.2, there continues to be significant interest in SIP configurations. SIP architectures can be broadly classed in three categories:

(a) Planar configurations where two or more die or packages are placed side by side and connected to each other through lateral interconnects in a multilayer substrate.
(b) Stacked configurations where two or more die, or packages, are stacked one on top of the others and connected through a combination of both lateral and vertical interconnects. The value of implementing stacking in a product

[2] An IP (Intellectual Property) block is reusable circuit block that performs a certain specialized functions and serves as a building block for constructing the SOC.

Table 2.1 Volume forecast of different SIP configurations (Source: Prismark Partners LLC)

SiP/MCP forecast			
Product/package type volume (Bn units)	2014	2019 F	Leading suppliers/players
Stacked die in package and memory card	8.3	10.5	Samsung, Micron, SKHynix, Toshiba, SanDisk PTI, ASE, SPIL, Amkor, STATS ChipPAC
Stacked package on package: bottom package only	0.95	1.2	Samsung, Apple, Qualcomm, MediaTek Amkor, STATS ChipPAC, ASE, SPIL
PA centric RF module	4.5	5.9	Qorvo, Skyworks, Anadigics, Avago, Amkor, ASE, Inari, HEG, JCET. Unisem, ShunSin
Connectivity module (bluetooth/WLAN)	0.6	0.9	Murata, Taiyo Yuden, Samsung, ACSIP, ALPS, USI
Graphics/CPU or ASIC MCP	0.2	0.2	Intel, AMD, Nvidia, Xilinx, Altera
Leadframe module (power SiP)	3.2	4.7	NXP, STMicro, TI, Freescale, Toshiba, Infineon/IR, Renesas, ON Semi
MEMS and controller	5 4	8.2	ST, Analog, Bosch, Freescale, Knowles, InvenSense, Denso
Camera module	3.7	5.3	LG Innotek, SEMCO, Hon Hai, Lite-on, Toshiba, Sunny Optical, Sharp, Cowell
Fingerprint sensor	0.35	1.5	Apple, Synaptics, Fingerprint Cards, Cypress/ IDEX, Silead, Goodix, NEXT Biometrics, Qualcomm
Total	*27.2*	*38.4*	

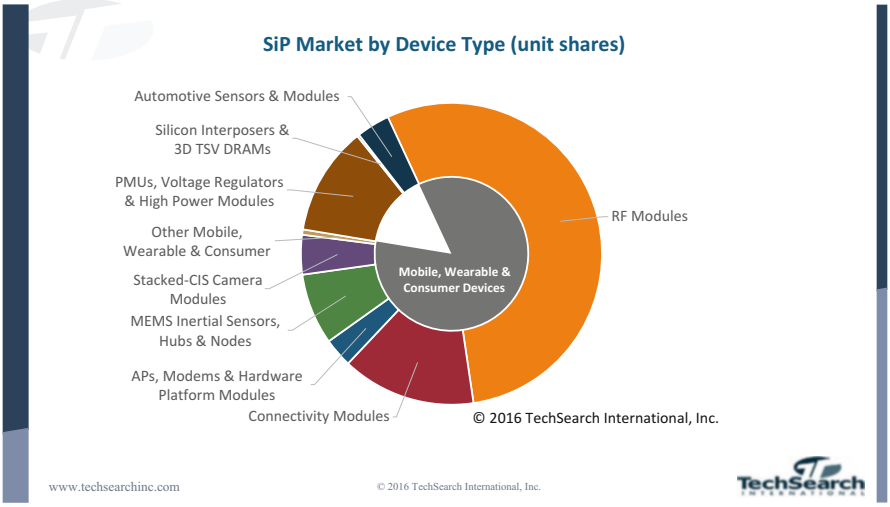

Fig. 2.2 2015 SIP Market by device type (Source: TechSearch International)

design, and thus leveraging the vertical dimension in a package, has been discussed in detail in [6].

(c) Hybrid configurations that combine both the planar and stacked configurations.

There are a number of innovative ways to construct SIP architectures using planar and stacked structures. Some of the more well-known SIP architectures are shown in Fig. 2.3. Figure 2.3 illustrates how different architectures have evolved to meet specific needs for different markets. Figure 2.3 is not intended to be a complete list of all the possible architectures. It is clear from the configurations shown in Fig. 2.3a–f that a number of SIP combinations are possible, offering feature, size, configuration, and cost flexibility.

One class of SIP configurations that has driven the most significant technology changes is through silicon vias (TSV)-based SIP. This chapter focuses on 3D stacks that are enabled by TSV technology. TSV-based SIPs have been the subject of considerable research for more than two decades and numerous papers have explored applications, architecture and design opportunities, as well as process, material, and equipment complexities [11–14]. Since it is difficult to comprehensively discuss all these aspects in a general overview, this chapter will attempt to provide a broad perspective of the architectural and process opportunities and complexities. The process of TSV formation has been previously discussed in depth in Chap. 3 and will not be repeated here, except for a brief reference in Sect. 2.3.

The most commonly used interconnect between stacked die for currently available products with TSVs is solder based (Fig. 2.4a, b) with interconnect pitches as low as 40 μm. Solder-based interconnects have an advantage of being compliant and hence they are more tolerant to misalignment and lack of coplanarity between bonded surfaces during assembly[3]. However as the joints become increasingly small, with decreasing interconnect pitches projected below 40 μm for future 3D stacks, the available solder volume will be reduced and a greater proportion of the solder joint will become intermetallic compounds [15], thus decreasing its compliance. Additionally, with shrinking interconnect pitch, there is an increasing risk of solder bridging during the assembly process since the joints are closer to each other. Various research groups have suggested the need for alternate interconnects; the most common among these are Cu-Cu bonding [17–21], a subject covered in detail in Chap. 6. In 2016, there are two types of widely available products with TSVs. These are DRAM memory stacks [7, 22, 23] and image sensors [24–26].

[3] In most applications, Thermo-Compression Bonding (TCB) is used to create the fine pitch interconnect typically needed between two stacked die because of its superior alignment capability over reflow based flip-chip bonding [16].