MICRO AND NANOMANUFACTURING

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Preface

When Nobel Laureate Richard Feynman presented his vision on miniaturization at the California Institute of Technology in 1959, he promoted a scientific curiosity in what is now known as "nanotechnology". His revolutionary vision was captured in a paper published in the February 1960 issue of Caltech's journal, "*Engineering and Science*". In this paper, Feynman speaks about controlling and manipulating atoms and constructing products atom-by-atom, and molecule-by-molecule. Feynman described the scaling down of lathes and drilling machines, and talks about drilling holes, turning, molding, stamping parts, and so forth. Even in 1959, Feynman described the need for micro- and nanomanufacturing as the basis for creating a microscopic world that would benefit mankind. Since the 1960s, Feynman's vision has created the basis for the foundation of the semiconductor industry and within the last decade, has rapidly contributed to the development of micro electro- mechanical systems (MEMS). At the same institution, President Bill Clinton talked about the exciting promise of nanotechnology in January 2000, and later announced an ambitious national nanotechnology initiative (NNI) that was enacted in 2001 with a budget of $497 million to promote nanoscale research that would benefit society. Nanotechnology encompasses technology performed at the nanoscale that has real-world applications. Nanofabrication includes methods that manipulate atoms and molecules to produce single artifacts to produce sub micron-sized components and systems. Nanomanufacturing is a challenge presented to us to produce single-nanoscale artifacts in a mass production fashion that obviously produces the accompanying economies of scale. Nanotechnology will have a profound effect on our society that will lead to breakthrough discoveries in materials and manufacturing, electronics, medicine, healthcare, the environment, sustainability, energy, biotechnology, information technology, national security, and prevention of the spread of global terrorism. Nanotechnology will lead the next industrial revolution.

The purpose of this book is to present information and knowledge on the emerging field of micro- and nanomanufacturing. The book is written in the spirit of scientific endeavor outlined by Richard Feynman, who stated that one of the greatest challenges to scientists in the field of miniaturization is the manufacture of tiny objects using techniques such as turning, molding, stamping, and drilling. The book presents information on subjects such as fabrication, molding, lithography, machining, milling, water drop machining, self assembly, manipulation, cutting, to name but a few.

The book should serve as a text for undergraduate and graduate courses in micro- and nanomanufacturing in subject areas such as mechanical engineering, materials science, physics, chemistry, and electrical and electronic engineering. The structure of the book is based on matter provided by many colleagues and the author wishes to thank Professor Waqar Ahmed, University of Ulster, U.K., Htet Sein, Manchester Metropolitan University, Grant Robinson, Purdue University, Luke Hyde, Purdue University, David Tolfree, Daresbury Laboratory, U.K., Emeritus Professor Milton Shaw, Arizona State University, Professor V. C. Venkatesh, Malaysia University of Technology, Sam McSpadden, Oak Ridge National Laboratory, Professor Kai Cheng, Brunel University, U.K., and Dr. Xun Luo, Cranfield University, U.K., for helping construct a source of knowledge and information on micro- and nanomanufacturing and for granting the author permission to use such matter.

The author expects that the textbook will stimulate further interest in this field of nanotechnology and hopes that there still is, "plenty of room at the bottom".

Mark J. Jackson
Purdue University

1. Principles of Micro- and Nanofabrication

1.1 Introduction

Innovations in the area of micro and nanofabrication have created opportunities to manufacture structures at the nanometer and millimeter scales. These opportunities can be used to fabricate electronic, optical, magnetic, and chemical/biological devices ranging from sensors to computation and control systems. In this chapter, we introduce the dominant micro and nanofabrication techniques that are currently used to fabricate structures in the nanometer scale up to the millimeter scale. The first part of this chapter focuses on microfabrication of MEMS and semiconductor devices as an example of microfabrication. Next, the chapter focuses on nanofabrication techniques including several top-down and bottom-up techniques. Again, we use semiconductor devices as an example that shows the promising techniques that can be used to manufacture nanofabricated structures.

Most micro and nanofabrication techniques were developed by the semiconductor industry. The semiconductor industry has grown rapidly in the past 30 years, which is driven by the microelectronics revolution. The desire to place many transistors on to a silicon wafer has demanded innovative ways to fabricate electronic circuits and to fit more and more electronic devices into a smaller workable area. Early transistors were made from germanium but are now predominantly silicon, with the remainder made from gallium arsenide. While gallium arsenide has high electron mobility compared to silicon, it has low hole mobility, a poor thermal oxide, less stability during thermal processing, and much higher defect density than silicon. Silicon is the material of choice for most electronic application but gallium arsenide is useful for circuits that operate at high speeds with low-to-moderate levels of integration. This type of material is used for analog circuits operating at speeds in excess of 10^9 Hz. The performance of integrated circuits can be increased by placing transistors closer together and by depositing transistors in a precise way. The minimum feature size has reduced at an astonishing rate over the past thirty years. Figure 1.1 shows the reduction in the feature sizes as a function of the number of transistors per chip using conventional lithographic techniques. Figure 1.2 shows a single strand of human hair and an array of transistors on a single piece of silicon to reveal the relative size of transistors that can be accommodated on a piece of silicon.

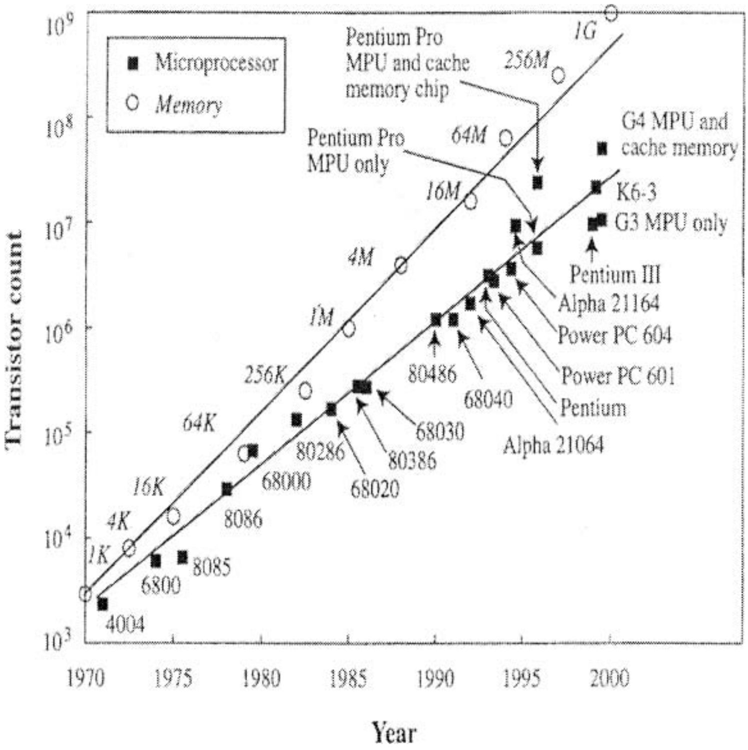


Fig. 1.1. Transistor count per chip as a function of time [1]

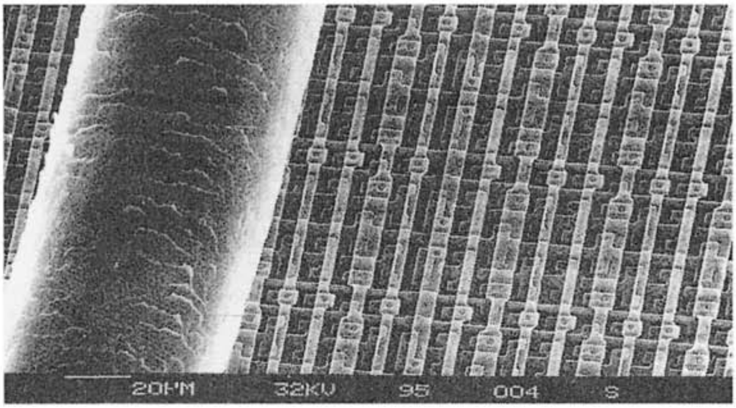


Fig. 1.2. Scanning electron micrograph of an integrated circuit chip in the mid-1980s. The human hair to the left of the image provides an indication of the relative size of the transistor wires [1]

Microfabrication begins when a set of photomasks are provided to the integrated circuit fabricator. The photomasks are physical representations of the design of the circuits to be manufactured in accordance with the rules of layout. A silicon wafer provides the basis of the integrated circuit. Wafers are processed using a grinding process that produces a flat surface that is still conductive at this stage. The wafer is insulated by growing a thermal oxide layer so that leakage of current between transistors is prevented. A conducting layer is deposited that will be used for producing transistors. Several techniques have been developed for depositing insulating and conducting layers such as sputtering, physical vapor deposition using a magnetron, chemical vapor deposition (CVD), and epitaxial growth of layers using techniques such as metal oxide CVD, molecular beam epitaxy, and chemical beam epitaxy. The conducting layer is divided up into individual resistors. Individual resistors are deposited to the wafer using photolithographic techniques. Further processing is required that forms the integrated circuit and uses techniques such as pattern transfer, etching, deposition, and growth. These same techniques have also been used to create a plethora of microscale products in silicon-based materials for applications other than integrated circuits.

1.1.1 Microfabrication of MEMS and Semiconductor Devices

Traditionally, integrated circuits have been manufactured using microfabrication techniques that have been classified as machining processes. Figure 1.3 shows the standard route followed to produce an integrated circuit. The same flowchart can be used for producing any microscale product produced using silicon-based materials. The chart shows the basic functions that are composed of initially cleaning the substrate, applying a thin film using many deposition techniques, applying lithographic techniques to apply mask material, etching to form the required shape of the microscale features, removal of the mask material using chemical or plasma etching, then finally characterizing the nature of the created structure. The final microstructures are then separated from the initial subtrate material and released for quality control.

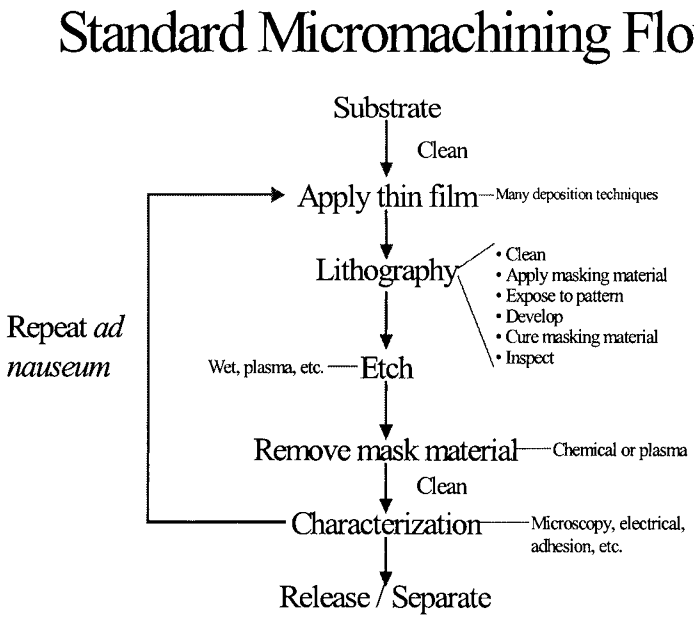


Fig. 1.3. Standard micromachining flow chart showing various processing steps

The basics of microfabrication are shown in Figs. 1.4 – 1.6 and show that fabrication at the microscale is made up of three basic regimes, i.e., addition, multiplication, and subtraction. The addition phase involves adding a thin film coating to the substrate material. This can take the form of electroplating or spray coating a liquid film to the substrate and allowing it to dry, or a thin film can be created by oxidation or doping in an atmospheric chamber. Other methods include fusion bonding a solid to the substrate, or using low- and high-pressure vacuum techniques to bond a thin coating to the substrate. The process of feature multiplication also takes many forms and is a process step necessary to create microscale features, particularly channeled features that are used in micro and nanofluidic devices.

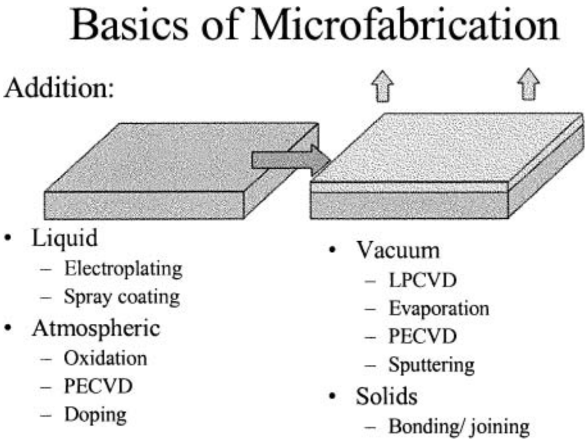
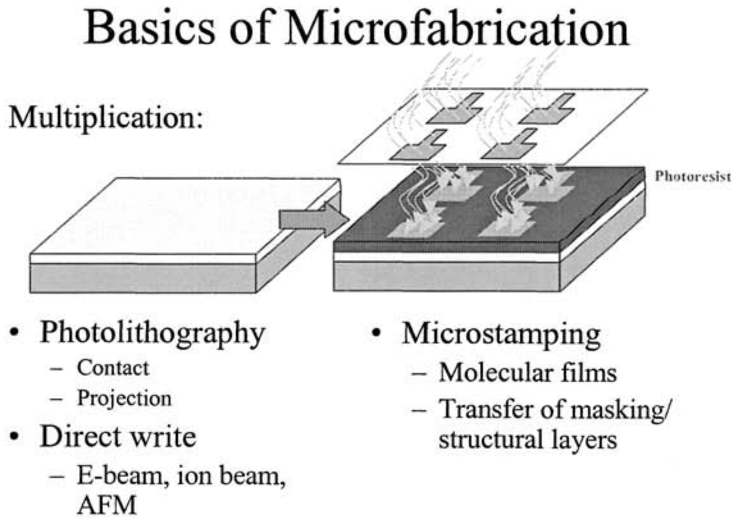


Fig. 1.4. Microfabrication by the addition of a thin solid film

Multiplication of features can be performed using a number of processes such as direct writing of features using electron beam, ion beam, and atomic force microscopic techniques. Contact lithography is another popular technique for depositing features in addition to new methods of micro/nanoscale feature generation using microstamping processes.

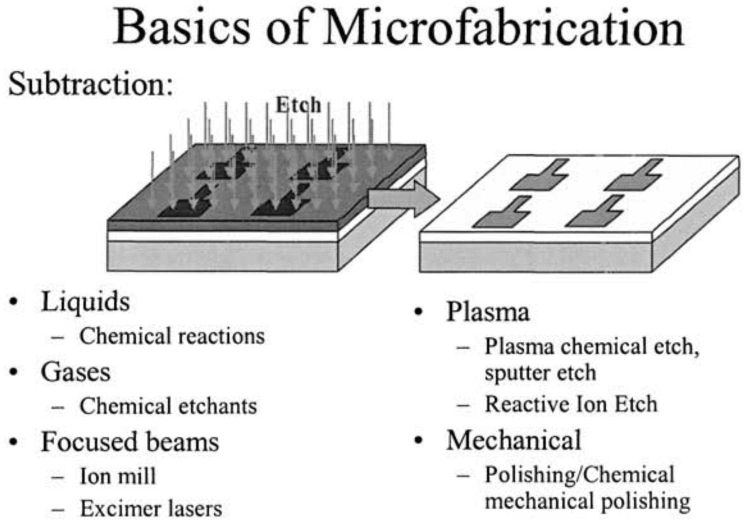


Basics of Microfabrication

Multiplication:

- Photolithography
  - Contact
  - Projection
- Direct write
  - E-beam, ion beam, AFM
- Microstamping
  - Molecular films
  - Transfer of masking/ structural layers

Fig. 1.5. Microfabrication by the multiplication of a thin solid film



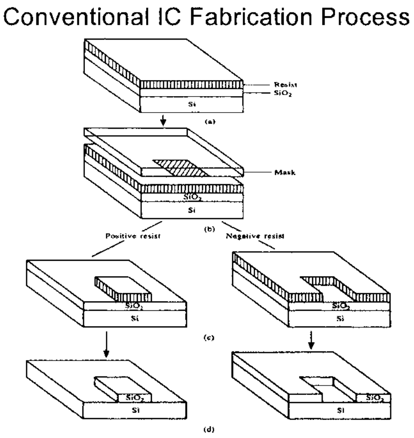
Basics of Microfabrication

Subtraction:

- Liquids
  - Chemical reactions
- Gases
  - Chemical etchants
- Focused beams
  - Ion mill
  - Excimer lasers
- Plasma
  - Plasma chemical etch, sputter etch
  - Reactive Ion Etch
- Mechanical
  - Polishing/Chemical mechanical polishing

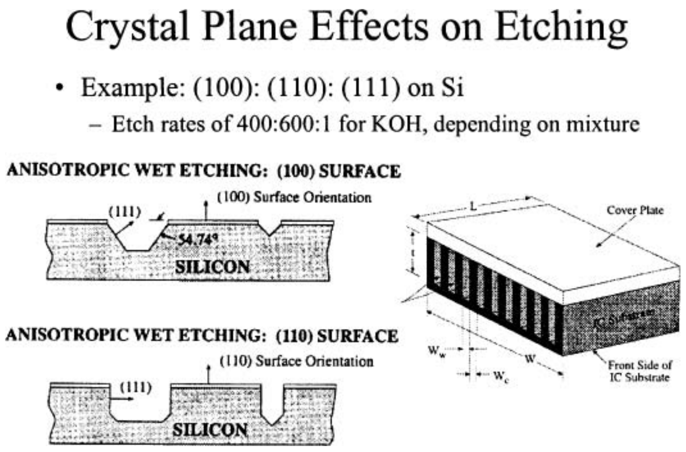
Fig. 1.6. Microfabrication by the subtraction of parts of a thin solid film

Subtraction of material to create features can be performed using a variety of techniques shown in Fig. 1.6. In materials other than silicon, subtraction processes can include mechanical micromilling, laser ablation, water micromachining, and a great number of other processes. These processes can remove material at much higher material removal rates and are discussed further in subsequent chapters in this textbook. Combinations of all of these techniques can be used to produce features of different size, shape, and scale. The standard way of creating features on single pieces of silicon is being surpassed by new microfabrication processes that achieve improved performance of individual devices. The standard way of producing integrated circuits is shown in Fig. 1.7, which shows the process of depositing a thin film on the surface of silicon, which is selectively removed by etching processes that produce wells or channels with known geometry owing to the texture of the silicon crystal.


Conventional IC Fabrication Process

Source: *Introduction to Microelectronics Fabrication*, Volume V, Modular Series on Solid State Devices, by R.C Jaeger, edited by G.W. Neudeck and R.F. Pierret. © 1988 by Addison-Wesley Publishing Company. Reprinted by permission.

Fig. 1.7. Typical fabrication process for an integrated circuit [2]



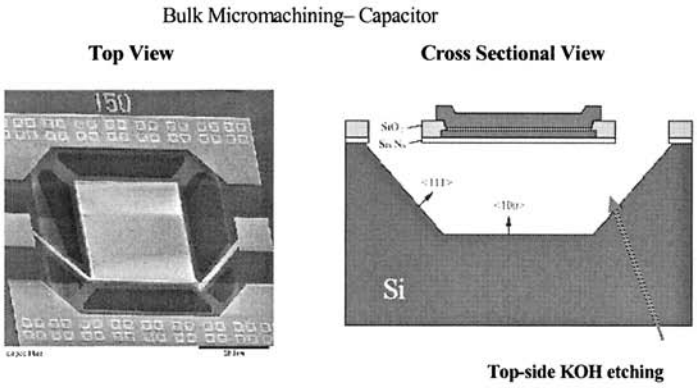
Crystal Plane Effects on Etching

- Example: (100): (110): (111) on Si
  - Etch rates of 400:600:1 for KOH, depending on mixture

Fig. 1.8. Crystal plane etching on (100), (110), and (111) planes of silicon using KOH etchant. The figure shows the shape of the channel produced in silicon by bulk micromachining [2]

The removal of silicon in certain directions of crystal planes is known as bulk micromachining [2]. Figure 1.8 shows the characteristic planes of silicon etched by using KOH etchant. The shape of the channel, or trench, produced is fixed by the way atoms are arranged in known directions.

The process of bulk micromachining to produce electronic devices such as capacitors is shown in Fig. 1.9. Here, (a) the feature is cleaned to prepare the substrate for deposition of the mask, (b) the mask is etched using KOH etchant, and (c) the substrate is etched to produce a deep trench. Trenches for microfluidic devices made from silicon can be produced in this way, but the shape of the trench is controlled by the way atoms are arranged in crystallographic planes.



Y. Sun, H. van Zeijl, J.L. Tauritz and R.G.F. Baets, "Suspended Membrane Inductors and Capacitors for Application in Silicon MMIC's," Microwave and Millimeter-wave Monolithic Circuits Symposium Digest of Papers, IEEE, 1996, pp. 99-102.

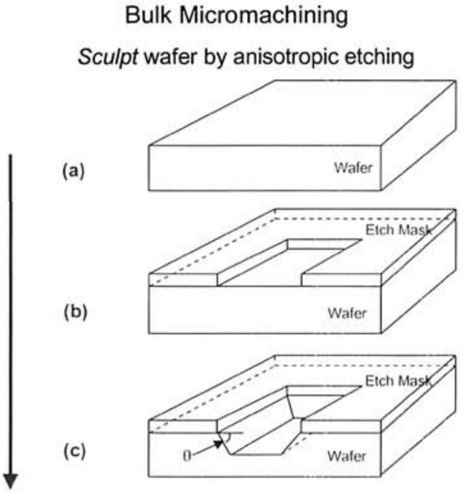
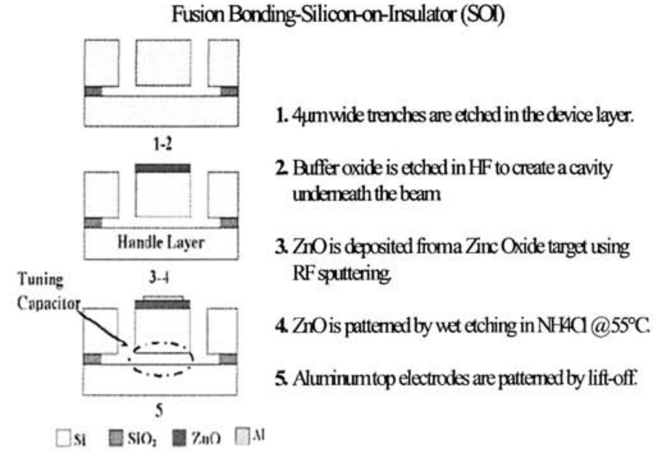


Fig. 1.9. Bulk micromachining by anisotropic etching to produce features such as a capacitor [3]

Another method used for bonding thin films to silicon substrates is fusion bonding. Figure 1.10 shows the basic principle used for bonding silicon on an insulator material to create a voltage tunable, piezo-electrically transduced SCS resonator (Fig. 1.11). Figure 1.11

shows the basic construction of the resonator, and also shows how etching a thin ZnO film can create a Q-enhanced resonating device. This process can also be used for creating stepped features in microfluidic devices and other micromachined products.

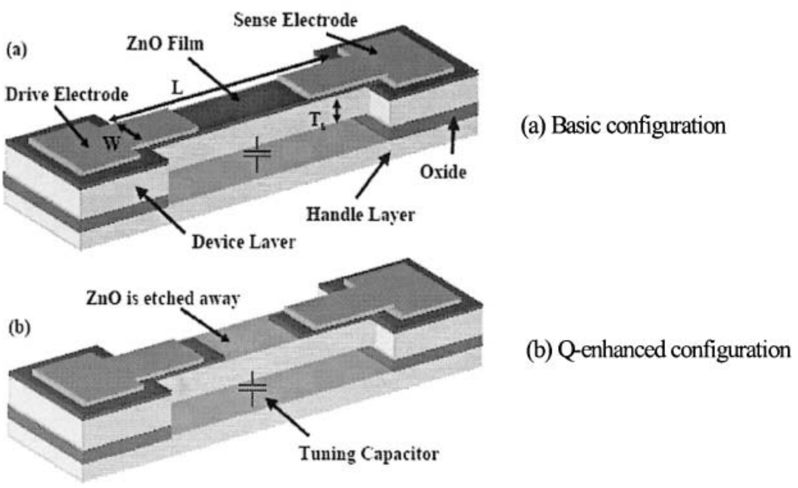

Fusion Bonding-Silicon-on-Insulator (SOI)

1. 4μm wide trenches are etched in the device layer.
2. Buffer oxide is etched in HF to create a cavity underneath the beam
3. ZnO is deposited froma Zinc Oxide target using RF sputtering.
4. ZnO is patterned by wet etching in NH4Cl @55°C.
5. Aluminum top electrodes are patterned by lift-off.

Piazza, G., R. Abdolvand, and F. Ayazi, Voltage-Tunable Piezoelectrically-Transduced Single-Crystal Silicon Resonators on SOI Substrate," *2003 IEEE MEMS* Conference, Kyoto, Japan, Kyoto, Japan, January 19 - 23, 2003, pp 149-152.

Fig. 1.10. Fusion bonding of silicon on an insulator showing the various steps of the process [4]

The formation of the trench in the previous application can take a long time to produce when using wet etchants. One way of increasing the aspect ratio of a trench to make it deeper is to reactively ion etch the substrate to produce a deeper feature. This principle of this process is shown in Fig. 1.12. The etching speed is typically 1 – 2 microns per minute, which is slow compared to mechanical micromilling processes and laser-based micromachining processes. The formation of features in engineering materials such as steel, copper, and aluminum alloys is usually achieved by using the aforementioned processes.

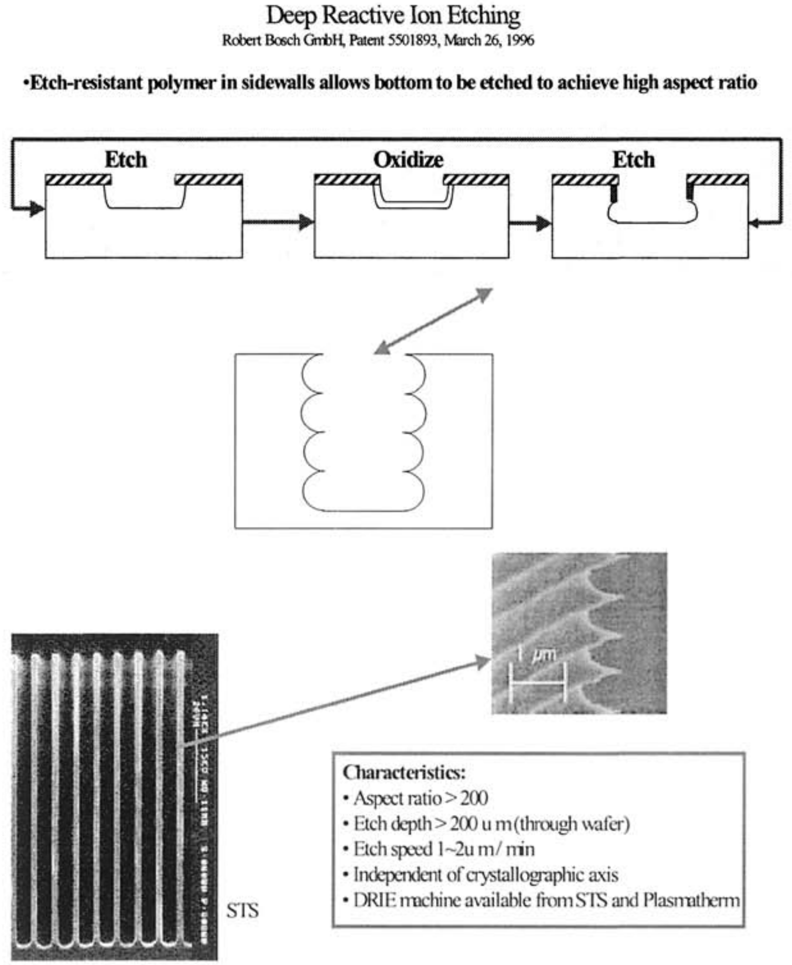


Voltage-tunable, piezoelectrically-transduced SCS resonators

Piazza, G., R. Abdolvand, and F. Ayazi, Voltage-Tunable Piezoelectrically-Transduced Single-Crystal Silicon Resonators on SOI Substrate," *2003 IEEE MEMS* Comference, Kyoto, Japan, Kyoto, Japan, January 19 - 23, 2003, pp 149-152.

Fig. 1.11. Voltage tunable, piezoelectrically-transduced SCS resonantor showing the manufacturing process used to produce the Q-enhanced configuration [4]

Deep reactive ion etching is a way of producing masters for manufacturing products on the mass scale. When coupled with micro molding techniques, a wide variety of microproducts can be produced. Deep reactive ion etching of deep trenches is used to produce tunable capacitors. Figure 1.13 shows such an application. This type of process is discussed in detail in Chapter 3.



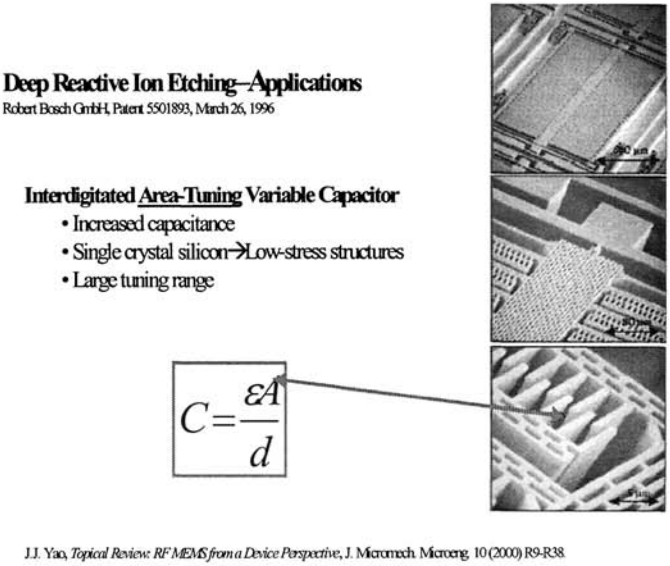
Deep Reactive Ion Etching

Robert Bosch GmbH, Patent 5501893, March 26, 1996

•Etch-resistant polymer in sidewalls allows bottom to be etched to achieve high aspect ratio

Characteristics:
- Aspect ratio > 200
- Etch depth > 200 u m (through wafer)
- Etch speed 1~2u m / min
- Independent of crystallographic axis
- DRIE machine available from STS and Plasmatherm

Fig. 1.12. Deep reactive ion etching of silicon substrate to produce trenches with aspect ratios greater than 200 at an etching speed of 1 - 2µm per minute [5]



Deep Reactive Ion Etching–Applications

Robert Bosch GmbH, Patent 5501893, March 26, 1996

Interdigitated Area-Tuning Variable Capacitor

- Increased capacitance
- Single crystal silicon→Low-stress structures
- Large tuning range

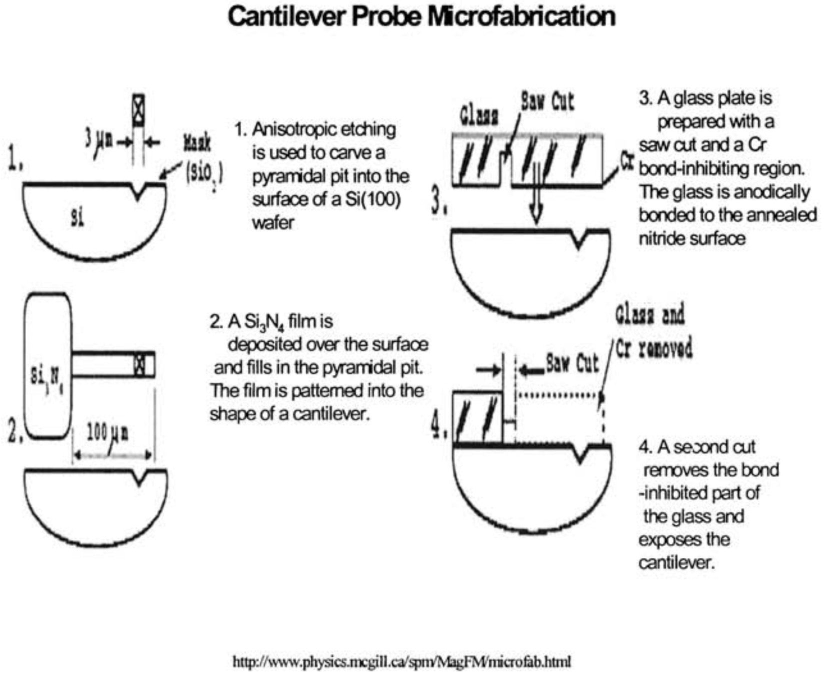
$$\boxed{C=\frac{\varepsilon A}{d}}$$

J.J. Yao, *Topical Review: RF MEMS from a Device Perspective*, J. Micromech. Microeng. 10 (2000) R9-R38.

Fig. 1.13. Area tunable variable capacitors [6]

In the field of nanofabrication, microfabrication processes can be used to make cantilever probes for atomic force microscopes that can be used for multiplying features on silicon and other materials by direct writing. The subsequent chapters of this book explain how microfabrication techniques have been developed to produce single products through fabrication, and also explain how multiple microproducts can be produced through manufacturing. An example of how microfabrication can produce nanofabrication tools is shown in Fig. 1.14. A cantilever made from silicon and glass is etched to produce the features required to produce a probe that is required to directly write to the surface of the substrate. This type of cantilever can be used to produce nanofabricated features that are discussed at length in the next section.

When producing the cantilever, anisotropic etching is used to form the pit into the (100) surface of the silicon wafer.



Cantilever Probe Microfabrication

1. Anisotropic etching is used to carve a pyramidal pit into the surface of a Si(100) wafer

2. A Si$_3$N$_4$ film is deposited over the surface and fills in the pyramidal pit. The film is patterned into the shape of a cantilever.

3. A glass plate is prepared with a saw cut and a Cr bond-inhibiting region. The glass is anodically bonded to the annealed nitride surface

4. A second cut removes the bond -inhibited part of the glass and exposes the cantilever.

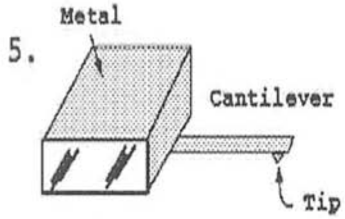
http://www.physics.mcgill.ca/spm/MagFM/microfab.html

Fig. 1.14. Initial stages of fabrication of a cantilever probe

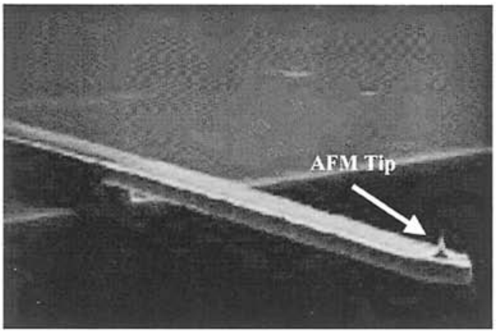
A silicon nitride film is deposited to the surface and fills the pit created by etching. The beam of the tip is prepared by using a glass plate from which the silicon is etched away to leave a silicon nitride cantilever beam that is connected to a metal block.

In addition to producing nanofabrication tools for the manipulation of single atoms or clusters of atoms and molecules, the semiconductor industry began producing field effect transistors with nanoscale features in the year 2000. The Pentium 4 microprocessor contains some 42 million transistors connected to each other on a single piece of silicon. To do this, silicon grown via the Czochralski process no longer produces a defect free substrate for the deposition of nanoscale transistors. Producers of silicon wafers routinely deposit a defect free single crystal silicon layer using a gaseous deposition technique.

Cantilever Probe Microfabrication



5. Silicon is etched away leaving the Si_3N_4 microcantilever attached to the edge of the glass block. The reverse side of the cantilever is coated with a reflective metal coating for the deflection detector.



http://www.physics.mcgill.ca/spm/MagFM/microfab.html

Fig. 1.15. Cantilever probe used for direct writing to a substrate

Engineers also deposit an oxide layer with low capacitance prior to the deposition of the thin silicon layer. This is known as silicon-on-insulator technology, which increases the speed transistors can be switched on and off. Another novel way of increasing the speed further still is to slightly strain the silicon lattice by forming a silicon-germanium blend that increases the mobility of electrons. To insulate the gate of the transistor, traditionally a thin layer of silicon dioxide has been deposited to conventional substrates. A material with a high dielectric constant is being developed to replace the use of silicon dioxide. Hafnium oxide and strontium titanate are likely contenders that will allow the gate oxide layer to be slightly thicker without compromising the switching ability of the transistor. This is achieved by atomic layer deposition. The first-generation nanoscale field effect transistor is shown in Fig. 1.16.

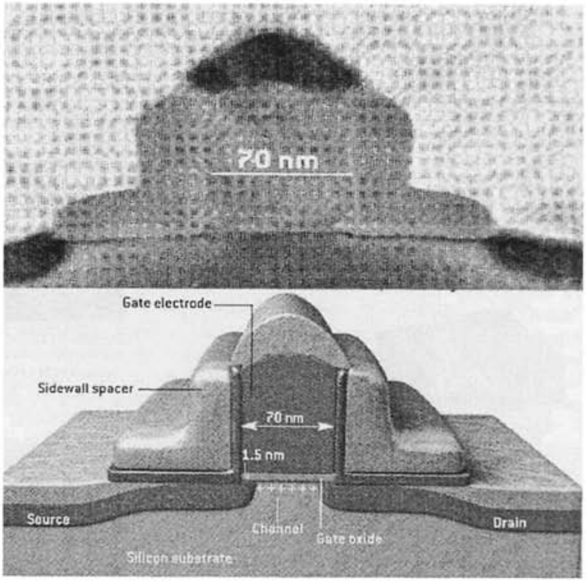
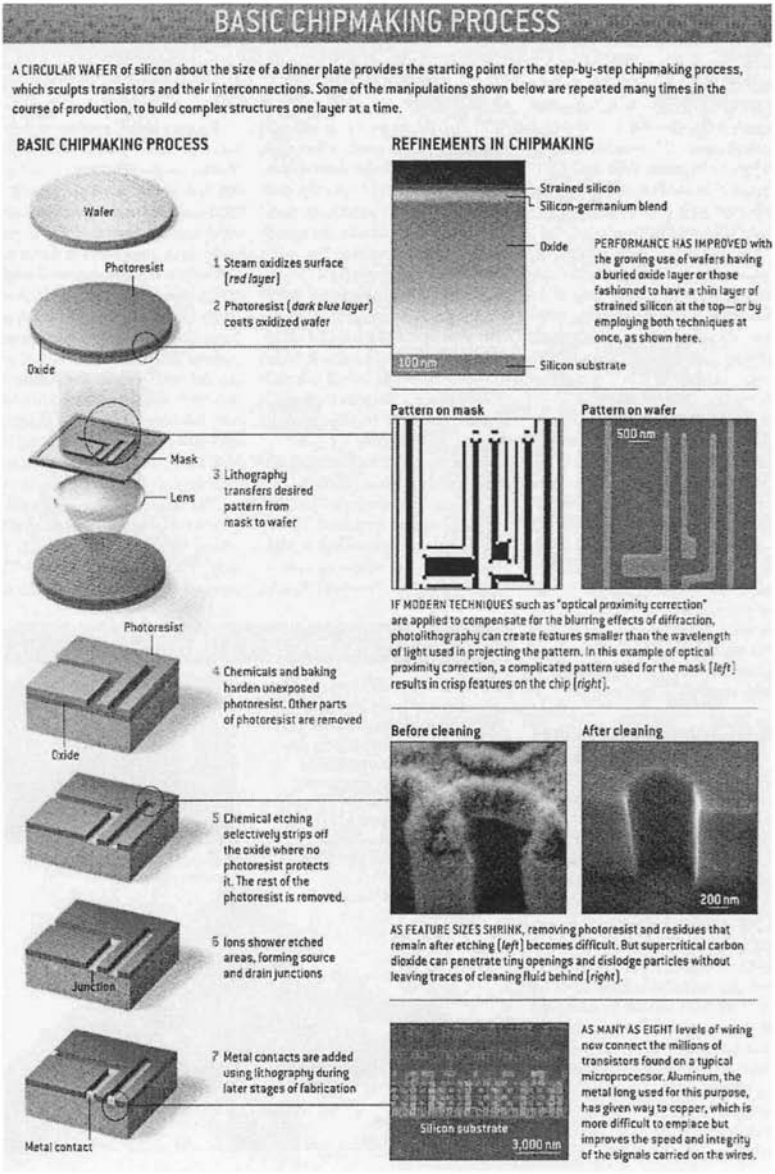


Fig. 1.16. The first generation of nanoscale field effect transistor [7]

After the gate insulators have been deposited, parts of the structure must be selectively removed to achieve the appropriate pattern on the silicon wafer. The lithographic procedure developed so far is needed to create transistors and their interconnections. The process of lithography traditionally created difficulties when feature sizes were smaller than the wavelength of light used to deposit small features to the silicon substrate. Since 2000, features in the range of 70 nm have been created using ultraviolet light that has a wavelength of 248 nm. Figure 1.17 shows the basic manufacturing process for producing microprocessors that employ nanoscale field effect transistors. To achieve this resolution, methods such as optical proximity correction, phase-shifting masks, and excimer lasers have been used to correct the aberrations. The latest technique employed using light with a wavelength of 193 nm produces features in the range of 50 nm. The next step is to use 'soft' x- rays such as extreme ultraviolet light, but difficulties occur using this technique because materials absorb light at extreme ultraviolet wavelengths and lenses become opaque; therefore projection would be aided by the use of multilayered mirrors. The solution to manufacturing at the nanoscale lies in the ability to pattern using mechanical techniques such as soft lithography and nanoimprint lithography.

Semiconductor manufacturers are also using a technique called "immersion lithography" that was developed in 2004 to overcome the diffraction limit imposed by optical lithography. Here, the process works by channeling water through the gap between the imaging machine and the photoresist that coats a semiconductor wafer, thereby improving the resolution of features on the chip and the depth of focus. As the stage that holds the wafer moves, the water supply is channeled away from the surface of the wafer (Fig. 1.18). Using this technology will reduce the resolution to 32 nm that will be required for the 2011 generation of chips. The use of sapphire lenses in the immersion lithographic technique is predicted to reduce the resolution further to 25 nm, i.e., 25 nm distance between transistors, for the 2015 generation of chips. Further advances to reduce the resolution further will require the use of extreme ultra-violet lithography, which is projected to reduce the resolution to 13 nm. However, the mechanical techniques provide great promise for future generations of chips employing techniques such as soft lithography and nanoimprinting. Figure 1.18 shows the principle of immersion lithography as shown in *Scientific American* (July 2005).

This monograph presents fabrication and manufacturing processes that can be used for materials other than silicon. The purpose of this book is to introduce the reader to micro- and nanoscale manufacturing processes so that an informed choice of selecting manufacturing processes can be made for products other than those used in the semiconductor industry. This initial chapter introduces the reader to micro- and nanofabrication processes that have already been developed for the purpose of building micro- and nanoscale products. Subsequent chapters will focus on emerging processes that may prove useful for the manufacture of future micro- and nanoscale products.



BASIC CHIPMAKING PROCESS

A CIRCULAR WAFER of silicon about the size of a dinner plate provides the starting point for the step-by-step chipmaking process, which sculpts transistors and their interconnections. Some of the manipulations shown below are repeated many times in the course of production, to build complex structures one layer at a time.

BASIC CHIPMAKING PROCESS

1 Steam oxidizes surface [*red layer*]

2 Photoresist [*dark blue layer*] coats oxidized wafer

3 Lithography transfers desired pattern from mask to wafer

4 Chemicals and baking harden unexposed photoresist. Other parts of photoresist are removed

5 Chemical etching selectively strips off the oxide where no photoresist protects it. The rest of the photoresist is removed.

6 Ions shower etched areas, forming source and drain junctions

7 Metal contacts are added using lithography during later stages of fabrication

REFINEMENTS IN CHIPMAKING

PERFORMANCE HAS IMPROVED with the growing use of wafers having a buried oxide layer or those fashioned to have a thin layer of strained silicon at the top—or by employing both techniques at once, as shown here.

IF MODERN TECHNIQUES such as "optical proximity correction" are applied to compensate for the blurring effects of diffraction, photolithography can create features smaller than the wavelength of light used in projecting the pattern. In this example of optical proximity correction, a complicated pattern used for the mask [*left*] results in crisp features on the chip [*right*].

AS FEATURE SIZES SHRINK, removing photoresist and residues that remain after etching [*left*] becomes difficult. But supercritical carbon dioxide can penetrate tiny openings and dislodge particles without leaving traces of cleaning fluid behind [*right*].

AS MANY AS EIGHT levels of wiring now connect the millions of transistors found on a typical microprocessor. Aluminum, the metal long used for this purpose, has given way to copper, which is more difficult to emplace but improves the speed and integrity of the signals carried on the wires.

Fig. 1.17. Schematic diagram of the processing procedure required to manufacture microprocessors with nanoscale features with resolutions of the order of 200 nm[7]

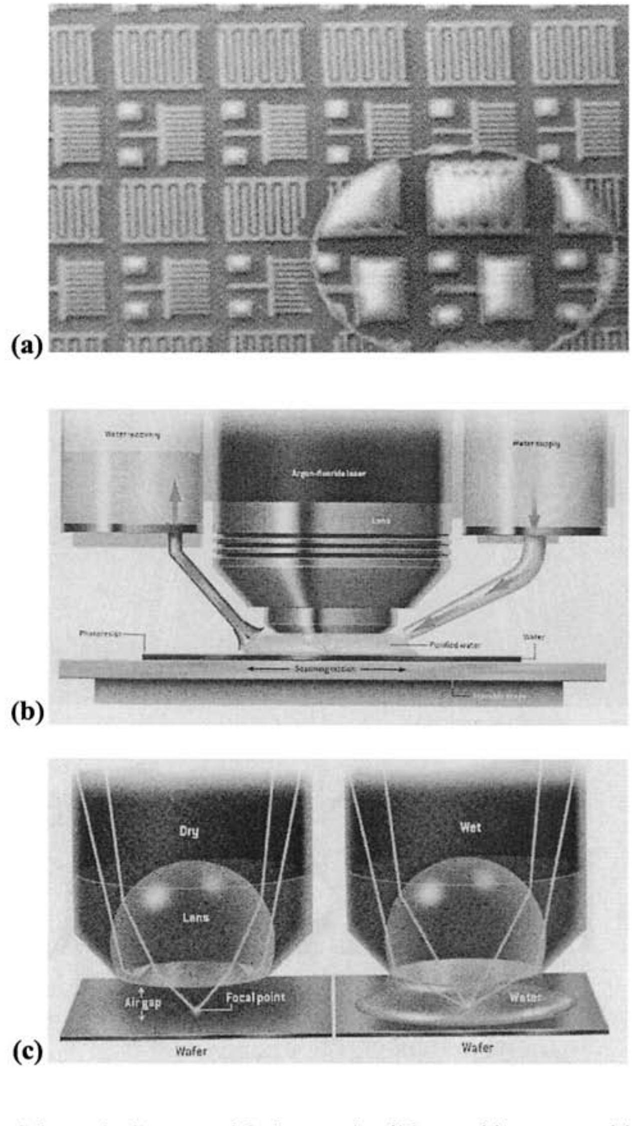
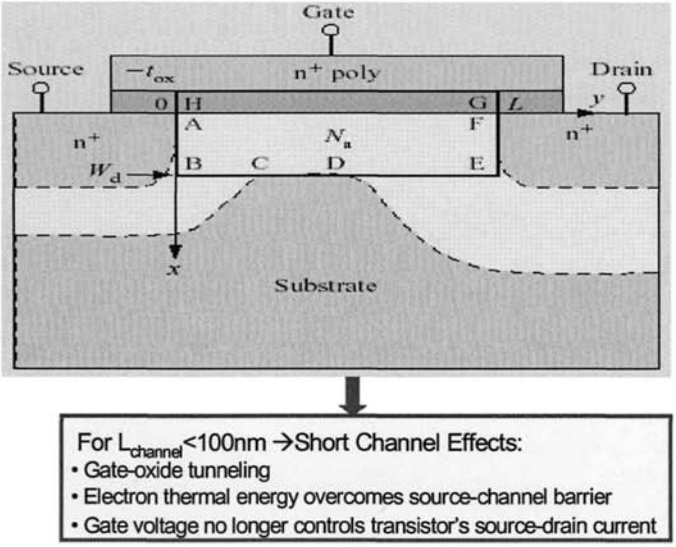


Fig. 1.18. Schematic diagram of the immersion lithographic process: (a) water drop showing change in resolution; (b) process showing the supply and extraction of water between lens and silicon wafer; and (c) principle of light reflection between air gap and liquid drop showing position of focal point on chip and path of reflected light waves. (Reproduced courtesy of *Scientific American* – "Shrinking circuits with water" by G. Stix, July 2005.)

1.1.2 Nanofabrication of Semiconductor Devices

Nanofabrication Using Soft Lithography

Nanofabrication has developed from a direct requirement to increase the density of transistors to a single piece of silicon. However, nanofabrication can be used to develop products other than for the semiconductor industry. In the first instance, nanofabrication is being developed to construct devices such as resonant tunneling diodes and transistors, and single-electron transistors and carbon nanotube transistors. The most common type of transistor being developed for use at the nanoscale is the field effect transistor. Figure 1.19 shows such a transistor and also its physical features such as source, drain, and gate, and each component of the fabricated transistor in relation to the substrate.



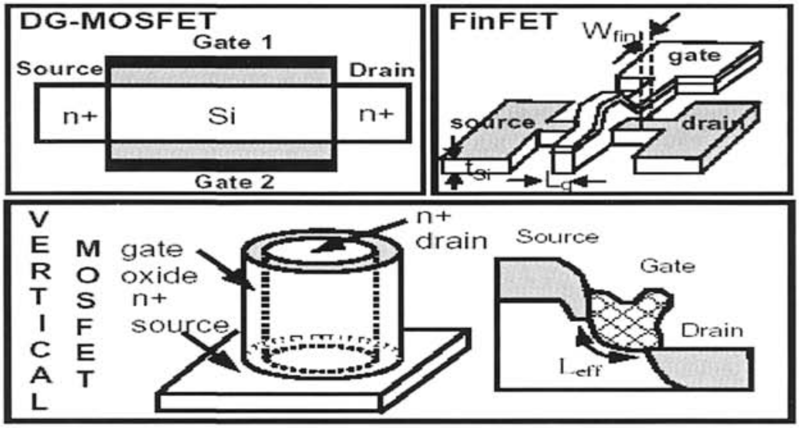
For $L_{channel}$<100nm →Short Channel Effects:

- Gate-oxide tunneling
- Electron thermal energy overcomes source-channel barrier
- Gate voltage no longer controls transistor's source-drain current

Y.. Taur,
IBM
J. Res. &
Dev.
,vol. 46, No.
2/3, 2002

Fig. 1.19. Schematic diagram of the field effect transistor [8]

For very short channels of less than 100 nm, gate oxide tunneling effects occur where gate voltages no longer control the transistor's source-drain current flow. The challenge for nanofabrication of these devices is to deposit materials in a physical way that will faithfully reproduce device function. Figure 1.20 shows the physical layout of different types of field effect transistor.



A.M. Ionescu, *et al.* "Few Electron Devices: Towards Hybrid CMOS-SET Integrated Circuits," *39th Design Automation Conference (DAC) 2002*, pp. 88-93, June, New Orleans, Louisiana, USA

Fig. 1.20. Physical layout of various field effect transistors [9]

A very simple and novel way of reproducing nanoscale features is to use a technique known as soft lithography. In soft lithography, a liquid known as polydimethylsiloxane is poured on a master pattern of the feature to be produced. The liquid cures to form a "rubbery" solid that can be peeled over the master pattern to reveal a very simple mold that can be attached to a stamp. Figure 1.21 shows the basic principle of soft lithography. The basis of nanoelectronic fabrication of field effect transistors using the soft lithographic technique has been demonstrated using a process known as microcontact printing. In the self-assembly process, a stamp is coated with a solution of molecules known as thiols. Thiols then self-assemble on contact with a thin gold film that has been deposited to the silicon substrate.