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CHALLENGES AND METHODOLOGIES

FRONTIERS IN ELECTRONIC TESTING

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ADVANCES IN ELECTRONIC TESTING

CHALLENGES AND METHODOLOGIES

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Foreword

by Vishwani D. Agrawal

About five years ago, I was engaged in co-authoring a text-book on electronic testing for the *Frontiers in Electronic Testing* Book Series. We had to make some difficult decisions about what to include and what not to include. A text-book must contain all or most of the essentials of the established practices, and should not exceed a convenient, somewhat "standard," size. Those requirements do not leave room for what are the needs of the future and many of the groundbreaking developments. As a result, stuck-at tests win over delay tests, conventional analog tests are selected while radio frequency testing is ignored, and defect-oriented testing of nanometer devices is barely mentioned. So, no sooner the text-book was completed, I developed a feeling of discomfort about leaving out a vast amount of material on testing that could have been included.

What I have said about the text-book in the *Frontiers Series* applies to other text-books as well. As years go by the gap between those text-books and what is considered up-to-date has been widening. There is a definite need for documenting the advances in testing. It is for these reasons that I find the work of this edited volume by Dimitris Gizopoulos and his team of authors to be significant and timely.

The field of modern electronic testing can be regarded as about half a century old. Two things are obvious. First, the field has gained maturity. We have well established conferences and workshops all over the world organized by IEEE

Computer Society's Test Technology Technical Council. The attendance at these meeting remained quite steady even through down turns of the semiconductor industry. There is an over ten years old *Journal of Electronic Testing: Theory and Applications* that is entirely devoted to testing. The IEEE Computer Society has been publishing the *IEEE Design & Test of Computers* magazine for over two decades. Clearly, the field of electronic testing has developed a core but, and this is my second point, the field of testing now has a divergence of specializations. It is this divergence that an advanced book like this one captures.

While no one argues that the idea of an advanced book is good, there are problems with its implementation. Specialization demands experts and no single expert feels competent to write about all areas. Dimitris Gizopoulos has gathered a team of experts to write this book. Hence, the book provides, besides novel test methodologies, a collective insight into the emerging aspects of testing. This, I think, is beneficial to practicing engineers and researchers both of whom must stay at the forefront of technology.

Let me share a few of these insights with the reader. In Chapter 1, Rob Aiken states a theme, "*Defect-oriented tests for digital logic typically include comprehensive structural logic tests, a current test … and at-speed tests. All these tests share the property that they measure some aspect of circuit behavior that is directly affected by defects,…*" before expanding on it.

In Chapter 2, Jaume Segura, Charles Hawkins and Jerry Soden give a motivation for statistical test methods by saying, "*Deep submicron structures don't affect test and diagnosis just because they are small. They primarily impact test because the manufacturing parameters are not tightly controlled as they were in the past*."

Doug Josephson and Bob Gottlieb share their insights on silicon debug in Chapter 3. According to them, "*... test cases that are interesting for electrical validation are likely very different from those that are interesting for functional validation. For the ALU example, a CMOS dynamic circuit implementation may perform differently electrically if there are two add instructions executed in consecutive clock cycles than it would if there was a long period of inactivity between the add instructions … from a functional validation point of view, these cases would be identical*." Besides, I was fascinated with, "*An interesting example of "debugging" was in 1945 when a computer failure was traced down to a moth that was caught in a relay between contacts (Figure 3-1)*."

Discussing delay testing in Chapter 4, Adam Cron candidly admits, "*Much of this "information" about the prominent defect types is from informal discussions with engineers and researchers "in the trenches"*. "

Continuing on the theme of high-speed test in Chapter 5, Wolfgang Maichen points out, "*... any chain is only as strong as its weakest link. In this case it means that even the best performing, highest bandwidth, most accurate tester will fail to reliably sort good devices from bad ones or give accurate characterization results if the connection between tester and device – i.e. the interface – does not perform equally well ...*"

Chapter 6 on low-cost testers, written by Al Crouch and Geir Eide, is particularly timely in view of the rising costs of testing and the test equipment. This subject is almost always found missing from the usual text-books.

Today, it is unthinkable that a VLSI chip will be designed without embedded cores. In Chapter 7, Rubin Parekhji points out the problems with applying the conventional test methodology to core-based System-on-Chip (SOC). He goes on to provide test solutions that use the conventional test methods and the IEEE standards like 1149.1 and 1500.

A majority of the embedded cores are memories. Dean Adams, the author of Chapter 8, describes the design for test structures and test methods in detail. The following sentence in that chapter very well represents the nature of the memory test problem and its solution: "*All of the testing and redundancy calculation must be performed by built-in self-test logic embedded on chip around the memory structures. The BIST must be implemented and integrated on the chip through the use of EDA tools which understand the memories, the process, and the physical constraints of the chip*."

It is often said that testing of 10% analog circuitry of a mixed-signal device may contribute to 90% of the total test cost. Clearly, analog testing cannot be ignored. In Chapter 9, Stephen Sunter gives a complete coverage of analog test methodologies, fault modeling, design for testability including the IEEE 1149.4 test bus standard, and test tools.

For many digital test professionals radio frequency (RF) testing, mostly neglected during education, remains an unavoidable mystery. The wireless communication systems of today require SOCs that contain RF components. What I said above about the cost of analog testing is even more applicable to RF testing. Chapter 10 by Randy Wolf, Mustapha Slamani, John Ferrario and Jayendra Bhagat contains a comprehensive discussion on RF testing methods and tools that very few books on testing can boast of.

If we consider the varieties and the total number of printed circuit boards (PCB) manufactured in the world it will immediately become evident that the PCB test problem is no less important than the semiconductor device test problem. In Chapter 11, Kenneth Parker gives a detailed account of the PCB test methods oriented toward the board-specific defects, the conventional in-circuit testing (ICT), and the modern IEEE 1149.1 boundary-scan testing.

Considering that the eleven chapters of this book were written by different authors, the tasks of technical coordination and that of providing a uniform formatting and flow are not easy ones. I thank Dimitris Gizopoulos for his untiring effort on getting all chapters together and an excellent technical editing. This latest addition to the *Frontiers Series* is destined to serve an important role. However, "*Advances*" in the title of the book suggests that we keep track of the test technology as it advances. It is my hope that we will bring out future volumes of this type.

Vishwani D. Agrawal

Consulting Editor
Frontiers in Electronic Testing Book Series

September 2005

Preface

Electronic circuits testing has always been a very vibrant area of scientific research and development. The engineering adventure of discovering whether an integrated circuit has been properly manufactured and operates in accordance with its specifications advanced significantly over the last few decades. Every new manufacturing technology generation—already supporting feature sizes of a few tens of nanometers today—brings with it enhanced functionality, more transistors per unit area, elevated performance and reduced power consumption at lower costs per circuit unit. On the other hand, each shrinking manufacturing process also carries new types of failure mechanisms and defects which were either unknown or of less importance in previous generations of larger geometries and lower operating frequencies. Each integrated circuit generation packs more modules of improved or completely new functionality (digital logic, memories, analog and mixed-signal as well as radio frequency components) into half or even less of the space; as a consequence, improved or completely new testing techniques are necessary for them. To make matters worse, the rising instance count and shrinking pin-to-gate ratio exacerbate the difficulties of controlling and observing the internal nodes of the circuit.

The definitions of *test quality* and *test cost* have never been more complex than they are today. Electronic testing methodologies should be able to detect the new types of failure modes in modern manufacturing technologies. The population of

integrated circuit physical defects that are not accurately modeled by traditional fault models is rapidly increasing. Moreover, the majority of defects can only be detected when the circuit operates at its regular, full-speed frequency. This can only be guaranteed if the performance and accuracy of test application and response capturing are extremely high. The volume of test data (stimuli and responses) that should be applied to each manufactured circuit to provide high levels of confidence of it being correctly implemented, along with the need of applying tests at very high performance, precision and accuracy have launched the costs of capable test equipment alarmingly upwards. Reducing the cost of automatic test equipment while maintaining the ability to perform high performance, precise and accurate testing has been and will continue to be a major concern: careful embedding of test-related mechanisms on the chip itself, and communicating this information to the tester has shown a promising path to reach this cost and quality goal.

If new defect types are not given special consideration, integrated circuits released to the market, mounted in boards, and connected in their final system have an increased probability of malfunctioning. Conversely, if testing the manufactured circuit takes too long and/or costs too much (in an effort to exhaustively deal with new defect types) the price of testing will severely affect product development costs and the resulting delayed entry to the market will jeopardize product success. If testing is not performed with accurate measurement techniques, the product development cost will also be severely affected due to yield loss: fault-free devices will be rejected only because of inaccuracies in high-speed test measurements.

The major *challenge* of test technology researchers and practitioners today is to define and apply electronic testing methodologies that keep a *balance* between quality and cost. This fundamental test technology challenge is an essential component of a key term of modern electronics: *manufacturability*—the extent to which a new product can be easily and effectively manufactured at minimum cost and with maximum quality and reliability meeting customer expectations. Production of high quality electronic circuits at profitable yield levels requires carefully implemented testing strategies.

For the majority of electronic circuits today, it is crucial that the appropriate test budget (in terms of time or allocated expenses—these are usually directly related) must be utilized, no more, no less. All the *advances* of the last decades in electronic circuits test technology have led us to a maturity point that can make this happen. *Methodologies* and *practices* of the near future should take advantage of this knowledge base to effectively answer today's *challenges* of test cost and test quality; all that needs to be done is to understand and focus on these challenges. This is the motivation and inspiration behind this book: to provide a comprehensive text that focuses on the advances of the research and development community in key test technology topics, records today's industrial practices and new needs, elaborates on the challenges that emerging testing methodologies have to deal with, and provides a vision for the near future of this amazing journey. Hopefully, the book provides the necessary information to understand and assess the tradeoffs to achieve the ideal balance of meeting the appropriate test budget.

PURPOSE AND CONTENT OF THIS BOOK

This edited volume is a unique compilation of chapters on many electronic testing topics of importance today and in the foreseeable future. The topics discussed are those on which the vast majority of the research and development community in test technology works today; topics where the electronic circuits industry needs effective answers, methodologies and practices that can be applied in the short term.

Every chapter of the book includes the following pieces of information for the reader:

- *Insight* about the *importance* of the chapter topic today. Unless improved or new methodologies and solutions are devised in the topic, electronic testing will either lead to poor test quality or unacceptable test costs. This part of the chapters gives the *motivation* for further research and development in each topic.
- Detailed snapshot of the *state-of-the-art* in the topic and recent *advances* and *industry practices* related to it. The chapter authors allocated a significant portion of their efforts in distilling the literature and providing a comprehensive set of references that represent significant recent research in the topic and can be used as a compass for further in-depth study of each area.
- Identification of the *challenges* in the topic today. Challenges in a topic are either due to the topic being in its infancy and the lack of effective methodologies providing solutions, or due to new problems that emerging manufacturing technologies or product needs have introduced to mature topics. Both types of challenges are discussed in this book along with *vision* and *forecasting* about the near future as well as *guidelines* for the focus of emerging testing methodologies.

Chapter authors provide all this information based on their long experience in the corresponding topic, lots of industrial success and failure cases, supported by a deep understanding of what test quality and test cost mean today for the electronics market. The entire book has a strong industrial and practical orientation. Each chapter is written in a unique way corresponding to the specifics of the topic and representing the authors' background, experience, and way of addressing challenges, problems and solutions. There are several interconnecting relationships among the chapters of the book: chapters touch on the topics of each other, and the reader of one piece can refer to other locations in the book where more specialized elaboration can be found. The matched pieces of this puzzle give the entire picture of *Advances in Electronic Testing: Challenges and Methodologies*.

This book serves a different and unique purpose compared to the comprehensive list of test technology books in the *Frontiers in Electronic Testing* series—a series that continues to support the education of the international test technology community and has done so for the past ten years. This book is neither an introductory book in test technology nor a detailed and specialized study of a single research topic. These two purposes are very successfully served by the other books of the series. *Advances in Electronic Testing: Challenges and Methodologies*

enriches the series with a new type of edited volume on *recent advances* in modern electronic circuits testing. The book focuses on a carefully selected and broad set of topics among those in which intensive research and development takes place today and is expected to continue attracting the interest of researchers and practitioners in the near future.

The intention of this edited volume is to be an advanced textbook and valuable reference point for senior undergraduate students, graduate students in MSc or PhD tracks, researchers and professors conducting research in the electronic testing domain; this book can support orientation of their research plans. The book is also for industry engineers and managers seeking a global view and understanding of test technology and a dense elaboration on test technology issues they deal with in their development projects.

The book chapters are organized in a coherent sequence covering several aspects of electronic testing: failures, defects, bugs, fault models, test interfaces, tester-related considerations, circuit-specific aspects (cores, Systems-on-Chips, memories, mixed-signal and radio frequency circuits) as well as loaded boards testing. The list of chapters and contributing authors is as follows.

Chapter	**Author(s)**
Defect-Oriented Testing	Robert C. Aitken
Failure Mechanisms and Testing in Nanometer Technologies	Jaume Segura Charles Hawkins Jerry Soden
Silicon Debug	Doug Josephson Bob Gottlieb
Delay Testing	Adam Cron
High-Speed Digital Test Interfaces	Wolfgang Maichen
DFT-Oriented, Low-Cost Testers	Al Crouch Geir Eide
Embedded Cores and System-on-Chip Testing	Rubin Parekhji
Embedded Memory Testing	R. Dean Adams
Mixed-Signal Testing and DfT	Stephen K. Sunter
RF Testing	Randy Wolf Mustapha Slamani John Ferrario Jayendra Bhagat
Loaded Board Testing	Kenneth P. Parker

ACKNOWLEDGEMENTS

The authors of the book chapters have devoted several hours in putting together the material of this volume and presenting it in an as useful as possible way to the reader sharing their knowledge and experience in test technology. The most difficult task we faced during the writing of this book was to squeeze so much technical information in a topic in just a few pages; this took several revisions, lots of disk space and hundreds of emails. I want to warmly thank all authors for their

contribution to this volume and for having the patience to revise the chapters several times. Rob, Jaume, Chuck, Jerry, Doug, Bob, Adam, Wolfgang, Al, Geir, Rubin, Dean, Steve, Randy, Mustapha, John, Jayendra, Ken, it has been a pleasure working with you for this book.

I would like to acknowledge the continuous support and useful suggestions of Prof. Vishwani D. Agrawal, the Consulting Editor of *Frontiers in Electronic Testing* book series. It is my honor to have the Foreword of this volume written by him.

I also want to thank Mark de Jongh, Springer's Senior Publishing Editor, Cindy Zitter, Senior Assistant as well as Springer's production staff for the excellent collaboration.

Several corrections and improvements are due to the help of Mihalis Psarakis who did a thorough review of the entire book. Dimitris Kostakis saved many hours of work by providing valuable hints and answers for the formatting of the book. Ken Parker provided a great help since the beginning with his advises and hints on the structure and layout of the book. Many people have provided inputs and reviews to the authors of the chapters and are separately acknowledged in each chapter.

Dimitris Gizopoulos
September 2005

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Dedication

This book is dedicated to the moments when
one becomes two, two become three and ten become eleven.

Chapter 1

Defect-Oriented Testing

Robert C. Aitken

The integrated circuit manufacturing process is imperfect, and as a result defects are introduced into some of the fabricated chips. Defects take a wide variety of forms, from localized spot defects, typically extra or missing material caused by contamination, to defects affecting much larger areas, such as transistor changes caused by implantation variation.

Some defects affect circuit behavior. Testing is used to find these before products are shipped, in order to ensure high quality. Defect-oriented testing is a way to improve the efficiency of testing by targeting tests directly at the defects that cause incorrect circuit operation.

Defects occur in random places and can have unpredictable effects. The processes that cause them are continuous over a wide range of variables. In order to simplify the problem of identifying defective circuits, this infinite defect space is approximated by a finite set of faults. A fault is a deterministic, discrete change in circuit behavior. Faults are often thought of as being localized within a circuit (e.g. a particular gate is broken), but they may also be modeled mathematically as transformations that change the Boolean function implemented by a circuit. Many fault models are time-independent; some use an arbitrary form of time progression,

D. Gizopoulos (ed.), Advances in Electronic Testing: Challenges and Methodologies, 1-42.

while a few include time behavior explicitly. The fault effects associated with fault models can be as simple as replacing a subcircuit function with a constant value or be so complex as to require SPICE simulation to evaluate. The choice of fault model depends on its intended use (e.g. test generation, manufacturing quality prediction, defect diagnosis, characterization for defect tolerance, etc.)

This chapter provides an overview of the Defect-Oriented test approach, beginning with a brief history of the subject, an overview of defect mechanisms, with special emphasis on advanced technologies. This is followed by a discussion of how these change the behavior of circuits (fault models). Next is a catalog of the types of tests used in Defect-Oriented test, and a survey of relevant published experimental results on the effectiveness of Defect-Oriented test approaches. Finally, some thoughts on future directions are given as part of the conclusions.

1.1 HISTORY OF DEFECT-ORIENTED TESTING

Historically, all testing was functional, and asked the question "Does the device do what it is supposed to?" Functional tests are primarily defined logically (outputs are a function of the inputs). For digital logic, functional tests became too expensive to develop, due partly to the amount of manual effort required to write the tests, but more to the complexity required to translate verification testbenches and tests from a simulation or characterization environment into an ATE environment. As a result, functional tests in production have largely (but not completely) been replaced by structural tests. Structural tests changed the basic questions being asked by test, and expanded the "Does it work?" question into a new question and a syllogism: "Are all circuit elements present and working? If so, and the design is correct, then it must work". This approach is the basis of scan testing. *Defect-Oriented testing* takes a step beyond structural testing to ask, "What could go wrong with this design, how would the design's behavior change if this happened, and how can that be measured?" Any measurable circuit property could be affected: logical values, timing, current consumption, etc., whether part of the specification or not. Defect-Oriented tests for digital logic typically include comprehensive structural logic tests, a current test (typically a variant of I_{DDQ} test[1]), and at-speed tests. All these tests share the property that they measure some aspect of circuit behavior that is directly affected by defects, regardless of their direct applicability to normal circuit functionality.

A key aspect of Defect-Oriented Testing is measurability, and measurability involves overcoming multiple sources of error or variability, including:

1. Defect-dependent variation, since defects can change circuit behavior in a variety of ways.
2. Circuit-dependent variation, including manufacturing process related variation (e.g. gate length, oxide thickness, etc.).

[1] I_{DDQ} testing measures the quiescent (Q) current (I_{DD}) consumed by a device. In standard CMOS circuits, the defect-free current is mainly transistor leakage. Many defects raise the level of this current enough to be measured in production test.

3. Environment-dependent variation, since many circuit behaviors change depending on temperature and voltage.
4. Equipment-dependent variation, due to limitations in resolution, repeatability of measurement equipment, as well as drift over time and other machine-dependent variations.

A defect detection method is not useful unless it consistently separates defect-dependent variation from circuit- and environment-dependent variation in the context of equipment variation. We will concentrate mainly on the first two sources of variation in this chapter.

An interesting question is whether we can separate defect behavior from circuit variation. A given flaw, such as a resistive via, can have a range of resistance values. Some of these will cause the circuit to fail logically, others will cause timing failures under some operating conditions, and others will never fail. Defect-Oriented Testing needs to work with the design margin process in order to effectively distinguish between these cases.

Defect-Oriented test requires information exchange between design, test development, process R&D, wafer manufacturing and manufacturing test to be successful. Historically, all these elements have been present inside vertically organized companies, and this is still true today in many cases. In these cases, information exchange between various entities is relatively straightforward, since all are motivated to action by the ultimate financial success of the company. Most published success stories in Defect-Oriented Testing originate within vertically integrated companies.

However, the semiconductor industry has substantially disaggregated, allowing chip designers the freedom to select from a number of IP providers, wafer foundries, packaging and test houses, among others. Some of these complex relationships are shown in Figure 1-1.

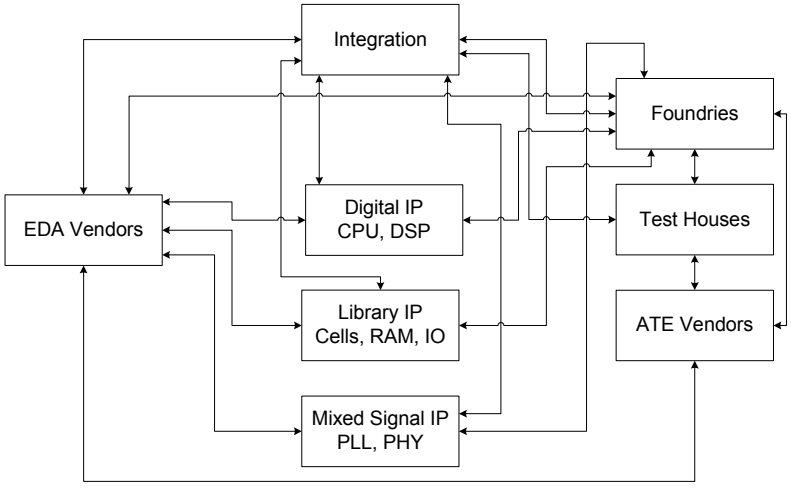

Figure 1-1: Value chain relationships in semiconductor industry.

In this situation, information exchange is not guaranteed, and in some cases may be hindered, based on economic interests of the various parties involved. To succeed in this context, a Defect-Oriented test methodology must provide some form of value to all companies involved. This constrains the problem significantly from the original vertically integrated case, but successful partnership approaches are possible, since all parties benefit from successful silicon.

This new format of the semiconductor industry should still be able to implement Defect-Oriented Testing, although in a modified form. For instance, in a single company, process engineers, library design engineers, and test engineers could easily collaborate on the best approach to designing a defect-robust scan flip-flop. In the disaggregated model, each of these three could belong to a different organization, different even from the design integrator and end customer. In such a model, the library design engineers need to develop flip-flop architectures that were robust across a variety of foundries, when used with standard EDA tools in standard ways. Similarly, the test house would need to be prepared for a variety of approaches. In each case, an effective flow can be established through standardization, through a robust methodology that can account for a variety of implementation techniques, or through a specific cooperative effort between organizations.

1.2 CLASSIC DEFECT MECHANISMS

The causes and manifestations of CMOS failures are many, but they have historically been lumped into two broad categories: Shorts, where conduction occurs when none is desired, and opens, where desired conduction does not occur. In aluminum processes, shorts have been more common and more problematic than opens, and so most research has focused on them [1]. Both shorts and opens have standard electrical properties. Of these, the most commonly studied has been resistance. Failure mechanisms will be discussed in detail in Chapter 2 of this book, but are introduced in brief here since they are key to understanding Defect-Oriented test.

1.2.1 Shorts

Shorts can be caused both by extra conducting material and by missing insulating material. Examples include:

- Photolithographic printing error
- Conductive particle contamination
- Incomplete etch
- Incomplete metal polish
- Crack in the insulator
- Gate oxide defect causing pinhole

For a comprehensive list, see Chapter 2 of this book. An example metal short by a conductive particle and gate oxide short are shown in Figure 1-2.

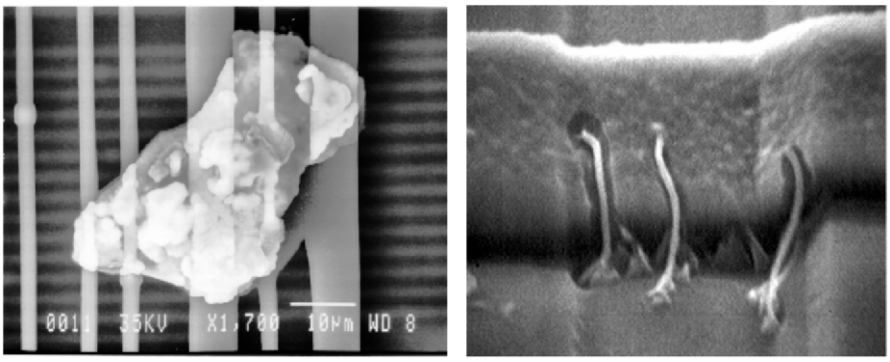

Figure 1-2: Particle and gate oxide shorts.

The electrical behavior of a short is determined by where it lies in a circuit. Shorts at the diffusion level often involve only the terminals of a single transistor. Shorts in poly or metal 1 affect the internals of one or more standard cells. Shorts in higher levels of metal interconnect typically involve gate outputs, power, and /or ground.

Shorts are active when the two nodes involved are driven to opposite values. A conducting path is formed from the power supply through active P transistors through the short (modeled as a resistance) through active N transistors to ground. The shorter (less resistive) the short, the more likely this conducting path will disrupt circuit operation. This basic idea can be extended to the concept of a "critical resistance" [2] below which the short "wins" and the circuit operates incorrectly, and above which the circuit "wins" and continues to operate correctly. There are actually multiple critical resistances for any short, as shown by Table 1-1 below, which lists delays associated with a bridge between an inverter output and ground in 0.13um technology. The waveforms associated with this Table can be seen in Figure 1-3. There is a logical critical resistance, where the circuit will fail under all circumstances (below about 1700 ohms), a set of timing critical resistances (e.g. at 1800 ohms, a delay of about 150ps results), where the critical resistance depends on required timing and also on operating environment, and finally, a set of I_{DDQ} critical resistance, where the defect will cause a significant enough increase in I_{DDQ} to be observed. An I_{DDQ} technique with 100uA resolution will be able to identify this short at 1.0V for resistances below 10kohms.

Resistance (Ω)	1700	1720	1730	1750	1800	2000	3000
Delay	SA0	600ps	400ps	250ps	150ps	70ps	<10ps

Table 1-1: Resistance and delay for short in 0.13um technology [3].

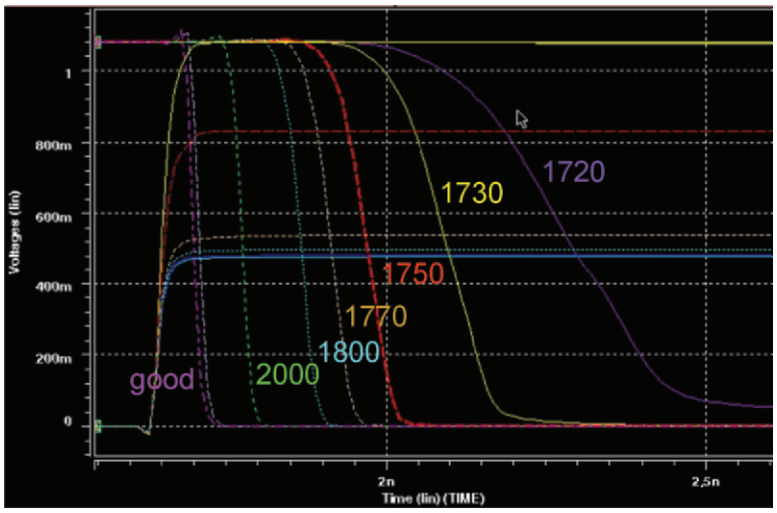

Figure 1-3: Resistance delay curves for a short in 0.13um technology.

Actual bridge resistance has been studied experimentally, and a wide distribution has been reported [4]. As technology advances, critical resistance is tending to rise, because timing requirements are tighter. Slack times – the difference between the required arrival of a signal and its actual arrival – are shrinking to the order of 100ps or less. At the same time, better synthesis algorithms are making more timing paths critical or near critical. So with more paths having less slack, even high resistance shorts are able to disturb circuit behavior enough to cause a fault.

1.2.2 Opens

Opens are caused by missing conducting material or extra insulating material. Examples of these include:

- Photolithographic printing error
- Step coverage
- Incompletely filled via
- Electromigration
- Silicide agglomeration
- Incomplete via etch or via foreign material
- Insulating particle contamination

As with shorts, the behavior of an open is determined by where it is located, whether in the transistor structure (diffusion, poly or metal 1) or in the interconnect between transistors (higher level metal). Logically, opens can be within a cell, or between cells. In many cases, a complete open results in a node that is electrically isolated from its surroundings. Charge stored on this node during fabrication can

affect its subsequent operation. For small opens, Fowler-Nordheim tunneling[2] can occur, resulting in a circuit that operates more slowly than expected. Many complex open behaviors have been postulated (see Chapter 2 of this book for details), but some of these have proven difficult to identify in practice. High levels of leakage and mutual capacitance in modern processes mean that open behavior will likely be more deterministic in future, in that stored charge will bleed away, or nodes will follow their neighbors.

In practice, many opens are partial or "almost opens". Such opens are challenging to detect and will be addressed later in this chapter. An experimental analysis of resistances was made in [5] and is given in Figure 1-4.

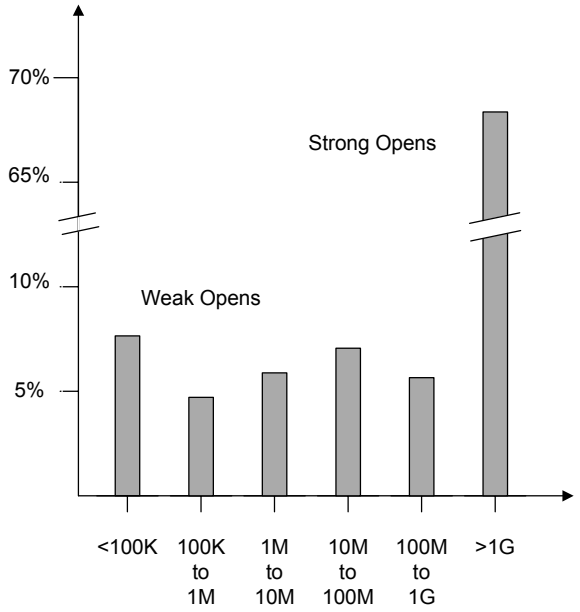

Figure 1-4: Resistance distribution for opens [5].

1.2.3 Parametric Changes

Defective behavior is not always caused by a single isolated problem such as a short or an open. Sometimes a circuit parameter is out of specification across a wide area, and this can cause a failure, or an increased susceptibility to other problems (e.g. temperature effects, crosstalk, etc.). These problems will also be discussed later in the chapter. Parametric variation begins with a physical change (e.g. variation in printed transistor gate length) and affects the circuit via electrical change (e.g. transistors that are faster and leakier than expected). In addition to gate length, other

[2] Fowler-Nordheim tunneling is the process by which an electron is able to "tunnel" under the potential barrier represented by the physical break in conducting material. As a result, current is still able to flow across a physically small open.

parameters of interest include dopant concentration (device mobility, capacitance), metal thickness (resistance, capacitance), oxide thickness (leakage, performance). Some variation is expected, and design must accommodate it, but at some point variation will exceed the tolerance or margin in the design, and it becomes a defect.

1.3 DEFECT MECHANISMS IN ADVANCED TECHNOLOGIES

This section covers some defect mechanisms that are becoming increasingly common in manufacturing processes at the 130nm node and below, and which need to provide the basis for ongoing efforts in Defect-Oriented test.

1.3.1 Copper-related Defects

For most of the history of CMOS, metal has meant aluminum. Since 130nm, however, copper has become the metal of choice, and this means that changes must be made in the way metal defects are considered. Aluminum metallization is a subtractive process: an entire layer of metal is deposited, a mask is applied and unwanted metal is etched away. This metal etch is inherently "dirty" and results in many particles being present, some of which lead to shorts. The etching process has led to shorts being far more common faults than opens in CMOS processes for many years.

Copper, on the other hand, uses a dual *damascene*[3] process. A layer of insulator is applied to the wafer. Next troughs for wires are etched (first damascene step). Next additional troughs for vias are etched. A layer of copper is electroplated into the trenches (on top of a small tantalum barrier/seed layer). Finally, excess copper is removed via *chemical/mechanical polishing* (*CMP*). There is no metal etch to provide a slurry of particles. As a result, additional defect mechanisms become important. Figure 1-5 summarizes the processing differences. Note that the process is highly simplified when copper is used.

In addition to a metal etch, aluminum processing also features two via/wire interfaces (tungsten to aluminum). Copper has only a single via/wire interface, since both vias and wires are deposited together. The absence of the metal etch and the reduced number of interfaces can result in a lower defect level for copper metalization than aluminum. However, there are some specific new defect mechanisms associated with copper. These were particularly troublesome in the early days of copper processing, but are now at more acceptable levels.

[3] The term "damascene" comes from metal inlaid with gold or silver, an intricate craft associated with the city of Damascus.