DIGITAL PHASE LOCK LOOPS

Digital Phase Lock Loops
Architectures and Applications

by

SALEH R. AL-ARAJI
Etisalat University College, Sharjah, UAE

ZAHIR M. HUSSAIN
RMIT University, Melbourne, Australia

and

MAHMOUD A. AL-QUTAYRI
Etisalat University College, Sharjah, UAE

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Preface

Since their introduction by de Bellescize in 1936, analogue Phase-Locked Loops (PLLs) have continued to play a major role in the advancement of several fields such as communications, signal processing and control [11]. Despite their performance advantages, analogue PLLs suffer from major drawbacks related to their analogue nature. These include aging and temperature drift effects, the sensitivity to component tolerances and operating conditions. In an attempt to combat the aforementioned drawbacks, Digital Phase-Locked Loops (DPLLs) were introduced in the 1970s as a result of the advent of digital technology and the urgent need for robust methods of synchronization for space communications [12]. One of the most promising versions of the DPLL is the Digital Tanlock Loop(DTL), which was introduced [13]. This loop offered many appealing features such as the linearity of the phase characteristics and the insensitivity to the variations in signal power. However, it did not gain a lot of popularity due to the complexities faced in the design of the Hilbert transformer, one of its major components.

Recently, an approach was proposed to rid the DTL from the Hilbert Transformer and its complexities by replacing it with a fixed time delay unit. This approach preserves most of the desirable characteristics of the DTL except for the linearity. The loop was named the Time Delay Digital Tanlock Loop (TDTL) [71].

Motivated by the desirable features of the TDTL, this book aims at analyzing the performance of the TDTL and implementing it as a reconfigurable system, which will serve as a testbed for future experimentations. The flexibility offered by reconfigurable computing devices, especially Field Programmable Gate Arrays (FPGAs), is being utilized in most communication systems to implement complex high-speed algorithms [14]. In addition to that, it will facilitate in upgrading and modifying of the TDTL testbed with minimum effort and complexity.

FPGAs are on the verge of revolutionizing digital signal processing in the manner digital signal processors did two decades ago. This is expected since FPGAs offer various attractive features such as rapid prototyping, on-the-fly upgradeability, code reuse and reduction in size and power consumption [14, 15].

The Main Contributions

The main contribution offered by this book is the introduction of modified architectures of the newly proposed TDTL that overcome the inherent limitations of the loop and undermines the tradeoffs between the locking range and speed of acquisition requirements. The proposed architectures are purely digital, therefore lending themselves to the implementation using reconfigurable modules without a significant increase in the complexity of implementation or design procedures.

Another major contribution offered is what may be considered as the first documented implementation of the TDTL using FPGAs. The implemented system will serve as a testbed for the performance enhancement and optimization of the loop.

Organization of Book

The first chapter provides a general review of phase-lock loops. Chapter two reviews the uniform and non-uniform type Digital Phase Lock Loops (DPLL). Chapter three covers the Time Delay Digital Tanlock Loop (TDTL) and it's convergence behavior. The following two chapters will focus on the Hilbert Transformer and Time-Delay, and the analysis of the TDTL in noise. The sixth chapter will cover the analysis, modified architectures, and the simulation results of the various TDTL architectures for improved performance. Chapter seven documents the design and implementation of a reconfigurable TDTL system using Field Programmable Gate Arrays, and analyzes the acquired results. Finally, chapter eight covers selected applications of the TDTL.

About the Authors

Professor Saleh Al-Araji

Prof. Al-Araji received the B.Sc., M.Sc., and Ph.D. degrees from the University of Wales Swansea, (UK), all in electrical engineering in 1968, 1969, and 1972 respectively. Since September 2002, Professor Al-Araji was appointed Professor and Head of Communications Engineering Department at Etisalat University College (Emirates Telecommunication Cooperation), Sharjah, UAE. Prior to that and for six years he was working at the Transmission Network Systems, Scientific-Atlanta, Atlanta, Georgia, USA as Senior Staff Electrical Engineer. During the academic year 1995/1996, Prof. Al-Araji was visiting professor at the Ohio State University, Columbus, Ohio, USA. He was visiting professor at King's College, University of London, England, during the summers of 1988 and 1989. Prof. Al-Araji was professor and Department Head at the University of Baghdad, Iraq, and the University of Yarmouk, Jordan. Prof. Al-Araji was awarded the British IERE Clerk Maxwell Premium for a paper published in 1976 and the Scientific-Atlanta award for outstanding achievement in the year 2000. He was an Iraqi National member of URSI Commissions C and D, and the ITU (CCIR Group 8). His research interests include synchronization techniques, communication signal processing, and CATV systems and networks. He has published over 50 papers in international Journals and Conferences and holds 6 US Patents and one International Patent. He is a reviewer to a number of international conferences and journals, and is involved in the organization of a number of international conferences in various capacities. Prof. Al-Araji is a senior member of the IEEE. His e-mail address is: alarajis@euc.ac.ae.

Associate Professor Zahir M. Hussain

Zahir M. Hussain took the first rank in Iraq in the General Baccalaureate Examinations 1979 with an average of 99%. He received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Baghdad, Iraq, in 1983 and 1989, respectively, and the PhD degree in electrical engineering from Queensland University of Technology (QUT), Brisbane, Australia in 2002. He has over 15 years of experience in teaching and research in various universities. He worked in several projects including the EEG biomedical project at QUT (1999-2001), where he contributed to solving the problem of instantaneous frequency estimation of multicomponent signals. In July 2001 he joined the School of Electrical and Computer Engineering, RMIT University, Melbourne, Australia as a Research Fellow in a 3G commercial project, then Lecturer of Signal Processing and the academic leader of another 3G communications project in November 2001. In March 2002 he was promoted to Senior Lecturer. In November 2005 he was promoted to Associate Professor and received the RMIT Publications Award. Since 2001, he has been the principal supervisor of nine PhD students; six of them have recently completed their studies successfully. Dr. Hussain is the author/co-author for over 120 technical papers on various fields. His current research interests are signal processing, communications, and mathematics. His joint work with Queensland University of Technology on single-bit processing has been acknowledged by the Australian Research Council (ARC) through an ARC Discovery Grant. Dr. Hussain is a member of Engineers Australia (previously IEAust), IEE, and a senior member of IEEE. He is a reviewer for the IEEE, Elsevier, and many other Journals on signal processing and communications. His e-mail address is zmhussain@ieee.org.

Dr. Mahmoud Al-Qutayri

Dr. Mahmoud Al-Qutayri received the B.Eng. degree in electrical engineering from Concordia University, Quebec, Canada, in 1984, the M.Sc. degree in electronic engineering from Manchester University, UK, in 1987, and the Ph.D. degree in electronic engineering from University of Bath, UK, in 1992. He has over fifteen year of experience in teaching and research at various universities. From 1988-1992 he was a research officer at the University of Bath, UK were he worked on testing techniques for analogue and mixed-signal integrated circuits. The project was in collaboration with another two universities and an integrated circuits design company. Dr. Al-Qutayri has also carried out consultancy work for a number of companies including ViewLogic, Lucas, Gent, Philips and others. From 1992-1996 he was a Senior Lecturer at DeMontfort University, Leicester, UK. He subsequently joined Etisalat (Telecommunications) University College in the UAE where he is currently an Associate Professor in the Department of Electronic Engineering. His research interests include testing and design for testability of mixed-signal integrated circuits, and application of reconfigurable computing to signal processing and communication systems, steganography and steganalysis. He published over forty technical papers in international journals and conferences. He is a reviewer to a number of international conferences and journals, and is involved in the organization of a number of international conferences in various capacities. Dr. Al-Qutayri is a Senior Member of the IEEE, member of the IEE and Chartered Engineer (Ceng.) in the UK. His e-mail address is: mqutayri@euc.ae.

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Acronyms

ADC	analog-to-digital converter
CDTL	conventional digital tanlock loop
CR	Cramer-Rao (bound)
DCO	digital controlled oscillator
DPLL	digital phase-locked loop
DTL	digital tanlock loop
FIR	finite impulse response
FM	frequency modulated signal
FT	Fourier transform
HT	Hilbert transformer
IF	instantaneous frequency
i.i.d.	independent and identically distributed
PLL	phase-locked loop
MSB	most significant bit
PDF	probability density function
PED	phase error detector
SNR	signal-to-noise ratio
TDTL	time-delay digital tanlock loop
var	variance
VCO	voltage controlled oscillator
ZC-DPLL	zero-crossing digital phase-locked loop
VD-TDTL	variable delay TDTL
SS-ATDTL	sample sensing adaptive TDTL
EES-ATDTL	early error sensing adaptive TDTL
ATDTL	adaptive TDTL
VO-TDTL	variable order TDTL

Chapter 1

General Review of Phase-Locked Loops

1.1 Overview of Phase-Locked Synchronization Schemes

Although not explicitly stated, the presence of transmitter-receiver synchronization is usually assumed in analyzing the performance of communication systems. For example, in the case of coherent Phase-Shift Keying (PSK) demodulation, the receiver is required to perform maximum-likelihood symbol decisions by comparing the incoming signals with a set of internally-generated reference signals. Generating these reference signals, which are assumed to be identical to those of the signaling alphabet at the transmitter, requires the receiver to be synchronized with the received carrier. This means that the there has to be phase alignment between the incoming carrier and the generated replica at the receiver, and therefore, the incoming carrier and the replica in the receiver would pass through zero simultaneously if there were no information modulated on the incoming carrier. The receiver in this state is said to be in phase-lock with the transmitter, and this condition must be closely approximated if coherently modulated signals are going to be accurately demodulated [6, 80].

Being in phase-lock means that the receiver's local oscillator is synchronized in both frequency and phase with the received carrier. In addition to that, phase-lock must also be established with the received subcarriers if the information-bearing signal is not modulated directly on the carrier. If the carrier and subcarrier are not kept in phase concurrence by the transmitter, the receiver is required to generate a replica of the subcarrier and control it's phase separately from that of the carrier replica, and therefore, enabling the receiver to achieve phase-lock on both the carrier and subcarrier [5].

The receiver is also required to achieve Symbol Synchronization by tracking the start and end of incoming symbols. These are required to determine the proper intervals for integrating the energy of symbols, and ensure making correct symbol decisions. This is achieved by producing a square wave whose zero transitions are aligned with the incoming signal's transitions between symbols in order to reach a symbol-lock state. The typically large number of carrier cycles per symbol period necessitate that achieving this level of synchronization with different circuitry than that used for phase synchronization [6, 7].

In the context of communication systems, synchronization is also required in a higher level, namely frame synchronization. Since information is usually organized into blocks, which are coded for forward error control and multiple access purposes, the knowledge of the boundaries between code words must be available at the decoder to ensure correct message or data extraction. In Time Division Multiple Access (TDMA), where multiple users are time-sharing common channels, it is necessary to know where the boundaries between channel users are in order to distribute the information appropriately. Similar to symbol synchronization, frame synchronization is equivalent to being able to generate a square wave at the frame rate, with the zero crossings matching the transitions from one frame to the next [6, 7].

All levels of synchronization, namely phase, symbol and frame, are required in most digital communication systems employing coherent modulation techniques. Conversely, noncoherent-modulation-based system usually make use of symbol and frame synchronization, and another level called frequency synchronization, in which the replica of the carrier generated by the receiver is allowed to have an arbitrary constant phase offset from the received carrier. The choice between coherent and noncoherent modulation methods is governed by the desired performance and complexity of implementation [80].

Although so far it seems that the synchronization is related only to the receiver, there are some communication systems that utilize the transmitter in performing a great deal of the synchronization role by tuning the timing and frequency of its transmissions to match the expectations of the receiver. For example, many terrestrial terminals in satellite communication networks are directing their transmissions toward a single satellite receiver. These transmitters rely on the receiver return paths to determine the accuracy of their synchronization, and therefore, transmitter synchronization often implies two-way communications or a network in order to be successful. Thus, transmitter synchronization is often called network synchronization [6].

1.2 The Synchronization Challenge

As mentioned earlier, there is a compromise between the performance and the implementation complexity. Extra levels of synchronization come at the cost of additional hardware or software in the receiver for acquisition and tracking. There are also costs associated with the synchronization overhead, energy and power consumption. However, the outcome of improved performance and versatility still outweighs the aforementioned costs, and communications system designers are always oriented towards designing systems with high degree of synchronization [7].

An example of this design strategy is the case of commercial analogue radio broadcast employing Amplitude Modulation (AM). This system is usually comprised of a central transmitter serving multiple receivers within its coverage area, and involves no synchronization. However, the passband of the receiver must be wide enough to house the modulating (information-bearing) signal, and account for its abrupt shifts in frequency due to the fluctuations in the output frequency of the local oscillator generating the carrier [6]. With this extra requirement, the performance of the receiver will degrade due to the fact that extra noise energy will be passed to the detector, which was not accounted for in the theoretical analysis. Adding the element of synchronization to this receiver will solve the problem, and improve the performance considerably. If the receiver contains extra circuitry for tracking the incoming carrier, the receiving filter will be centered about the carrier even if it fluctuates, and the detected noise energy will be decreased leading to a lower signal-to-noise-ratio (SNR) [6].

Moving to the digital communications domain, the same compromise can be demonstrated in the choice of modulations schemes. For example, noncoherent Binary Frequency Shift-Keying (BFSK) is considered among the simplest digital receivers in terms of implementation, requiring only symbol and frequency synchronization. However, choosing this modulating scheme will result in a 4-dB penalty in terms of bit error performance, i.e. the more complex coherent BPSK receiver can achieve the same bit error probability with 4 dB less SNR [7]. The trade-off between complexity and performance is further extended with the use of error-control coding algorithms. While they offer better performance under stringent operating conditions, they also result in more complex implementations, and require higher levels of synchronization between blocks, messages, and frames [81, 80]. Having discussed the principles and levels of synchronization, and the trade-offs between implementation costs and performance, the next section will explain the basic building block of almost all synchronization systems, namely the Phase-Locked Loop (PLL).

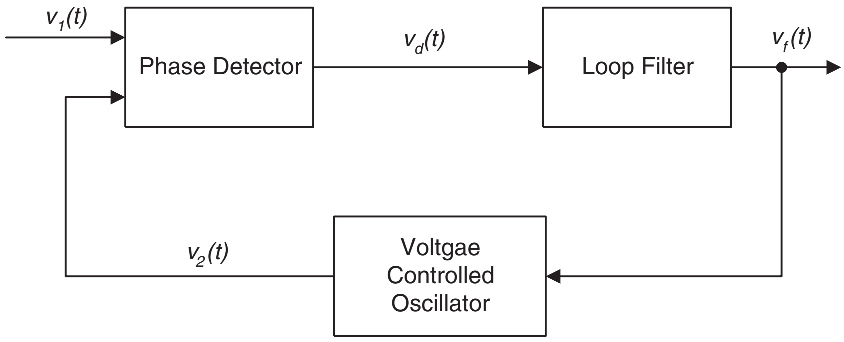

Figure 1.1: Block Diagram of the PLL.

1.3 Phase-Locked Loops

The PLL represents one of the most active topics in signal processing and communication theory. The initial ideas started as early as 1919 in the context of synchronization of oscillators. The theory of phase-locked loop was based on the theory of feedback amplifiers. The PLL contributed significantly to communications and motor servo systems. Due to the rapid development of integrated circuits (IC's) since the 1970's, PLLs are widely used in modern signal processing and communication systems, and it is expected that PLL will contribute to improvement in performance and reliability of future communication systems. The applications of PLLs include filtering, frequency synthesis, motor-speed control, frequency modulation, demodulation, signal detection, frequency tracking and many other applications [1, 9, 10, 11].

1.3.1 Analog Phase-locked Loops

A PLL is defined as a circuit that enables a particular system to track another one. More precisely, a PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in the frequency as well as in phase [5].

In the synchronized or the locked state, the phase error between the oscillator's output and the reference signal is either zero or an arbitrary constant. In the case of a phase error building up, the oscillator is tuned by a control mechanism in order to reduce the phase error to a minimum. In such a control system, the phase of the output signal is actually locked to the phase of the reference input. This is the reason behind calling this specific control system a Phase-Locked Loop [5]. The basic functional components of a PLL are: A voltage controlled oscillator (VCO), A phase detector (PD), and A loop filter (LF).

The signals of interest in the PLL block diagram shown in Figure 1.1 are defined as follows: The reference (or input signal) $v_1(t)$ with an angular frequency ω_1, The output signal $v_2(t)$ of the VCO with an angular frequency ω_2, The output signal $v_d(t)$ of the phase detector, The output signal $v_f(t)$ of the loop filter, and The phase error θ_e, defined as the phase difference between signals $v_1(t)$ and $v_2(t)$.

The VCO oscillates at an angular frequency ω_2 which is determined by the output signal v_f of the loop filter. The angular frequency ω_2 is given by

$$\omega_2(t) = \omega_o + K_o v_f(t) \tag{1.1}$$

Where ω_o is the centre frequency of the VCO and K_o is the VCO gain. The PD compares the phase of the output signal with the phase of the reference signal and generates an output signal v_d that is approximately proportional to the phase error θ_e, the former signal is given by:

$$v_d(t) = K_d \theta_e, \quad \theta_e \to 0 \tag{1.2}$$

where K_d represents the gain of the PD. The output signal $v_d(t)$ consists of a dc component and a superimposed ac component. Since the latter is undesired, it is cancelled by the loop filter. Assuming the angular frequency of the input signal $v_1(t)$ is equal to the centre frequency ω_o, the VCO then operates at its centre frequency ω_o, and the phase error is zero, indicating the output signal of the loop filter v_f is also zero. If the phase error θ_e was not initially zero, the PD would develop a nonzero output signal v_d. After some delay the loop filter would also produce a finite signal v_f, which will cause the VCO to change its operating frequency in such a way that the phase error finally vanishes.

Now, assume that the frequency of the input signal is changed suddenly at a time instant t_o by the amount of $\Delta\omega$. This will cause the phase of the input signal to lead the phase of the output signal, and a phase error will build up and increase with time. The PD develops a time-increasing signal $v_d(t)$, which will cause $v_f(t)$ to rise after some delay introduced by the loop filter. This causes the VCO to increase its frequency in order to minimize the phase error, and after some settling time the VCO will oscillate at a frequency that is exactly the frequency of the input signal. Depending on the type of the loop filter used, the final phase error will have been reduced to zero or to a finite value.

The VCO now operates at a frequency that is greater than its center frequency ω_o by an amount $\Delta\omega$, this will force the signal $v_f(t)$ to settle at a final value of $v_f = \Delta\omega/K_o$. If the centre frequency of the input signal is frequency modulated by an arbitrary low-frequency signal, then the output signal of the loop filter is the demodulated signal. The PLL can consequently be used as an

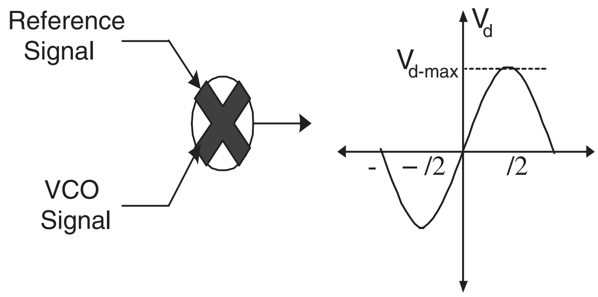

Figure 1.2: Classical Mixing Phase Detector.

FM demodulator, or in more general terms, it can be used as a demodulator of any scheme that stores the information in the frequency of the phase of the modulated carrier [5].

One of the most interesting capabilities of the PLL is its ability to suppress noise superimposed on its input signal. Assuming that the input signal of the PLL is degraded by noise, the PD will attempt to measure the phase error between the input and output signal. The noise at the input causes the zero crossings of the input signal $v_1(t)$ to be advanced or delayed in a stochastic manner, causing the PD output signal $v_d(t)$ to jitter around an average value.

If the cut-off frequency of the loop filter is low enough so that almost no noise will be noticeable in the signal $v_f(t)$ and the VCO will operate in such a way that the phase of the signal $v_2(t)$ is equal to the average phase of the input signal $v_1(t)$, it can be stated that the PLL is able to detect a signal that is badly degraded by noise. These simplified considerations show that the PLL is a typical servo system that controls the phase of the output signal $v_2(t)$ [1, 5].

1.3.2 PLL Basic Components

The Phase Detector

As previously mentioned the function of the phase detector block is to compare the phases of the input and output signals and generate an error signal proportional to the phase deviation between them. The most prevalent device capable of achieving this function is the mixer, which generates the sums and differences of the frequencies at its input terminals.

The mixing phase detector shown in Figure 1.2 will be discussed later in Section 1.3.3. This PD has a superior noise performance to all the other detectors, due to the fact that it operates on the entire amplitude of the input and VCO signals, rather than quantizing them to 1 bit [12]. Balanced mixers are best suited for PLL applications in the microwave frequency range as well as in low noise frequency synthesizers. However, this results in a loop whose gain is dependent upon the signal amplitude. Furthermore, nonidealities in the circuit implementation of the mixer result in nonlinear responses. When noise is not an issue, it is advantageous to move to a detector that has immunity to these effects [1, 2, 3, 4].

The Voltage-Controlled Oscillator

The actual clock generated by a PLL comes from the voltage-controlled oscillator (VCO), which generates a periodic oscillation. The frequency of this oscillation can be controlled by modulating some control voltage. In a PLL, the control voltage corresponds to some filtered form of the phase error. In response to this, the VCO adjusts its frequency. As the VCO frequency is slewed by the control voltage, the phase error is driven towards zero. This frequency adjustment to achieve phase lock results in the model of a VCO as an integrator [1, 5].

VCOs are generally of the form of a ring oscillator, relaxation oscillator or a resonant oscillator. The ring oscillator takes the form of an odd number of inverters connected in a feedback loop. The relaxation oscillator uses a Schmitt-trigger to generate a stable square wave [2]. The latter puts a resonant circuit in the positive feedback path of a voltage to current amplifier as shown in Figure 1.3. The resonant circuit in the positive feedback path has poles close to the $j\omega$ axis. Consider the bandpass filter:

$$F(s) = \frac{2\zeta\omega_o s}{s^2 + 2\zeta\omega_o s + \omega_o^2} \tag{1.3}$$

and $G(s) = K < 1$. Then

$$VCO(s) = \frac{G(s)}{1 - G(s)F(s)} = K\frac{s^2 + 2\zeta\omega_o s + \omega_o^2}{s^2 + 2\zeta_1\omega_o s + \omega_o^2} \tag{1.4}$$

where $\zeta_1 = (1 - K)\zeta$. The lowering of the damping ratio is called "Q amplification" ($Q = 1/2\zeta$) and moves the poles even closer to the $j\omega$ axis. The frequency is controlled by altering the capacitance of the resonator by using a varactor diode as a capacitor. A simple circuit diagram for a resonant circuit VCO is shown in Figure 1.4, where the frequency is controlled by adjusting the reverse bias of the varactor diode C_1 [1]. Other forms of VCOs, such as crystal