INTEGRATED CIRCUIT PACKAGING, ASSEMBLY AND INTERCONNECTIONS

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Springer

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Integrated Circuit Packaging, Assembly and Interconnections

Library of Congress Control Number: 2006927423

ISBN 0-387-28153-3 e-ISBN 0-387-33913-2
ISBN 978-0387-28153-7 e-ISBN 978-0387-33913-9

Printed on acid-free paper.

9 8 7 6 5 4 3 2 1

springer.com

DEDICATION

To my family,

my wife Joan

and

our children, their spouses and grandchildren

Karen – Christopher, Ryan, Kevin
Billy and Cathy – Alli, Jeff, Shauna
Joni and Fred – Danny, Kerri, Traci Jo
Jimmy and Colleen – Maggie, Molly, Katie, Claire
Ronny and Meryl – RJ, Connor
Steven
Kenny

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Preface

The integrated circuit with each new generation has been characterized by increasing functionality. In the 1980's Very Large Scale Integrated Circuits (VLSIC) began to emerge with transistor counts approaching one million plus per chip! The IC package quickly became more than a "chip carrier". Now the packaging had to address the electrical, mechanical and thermal requirements of the IC, and had to do so cost-effectively. A package costing more than the chip was not an option. In addition, the demands of the marketplace for product that was "smaller, better and cheaper" came into play.

As a result the late '80s saw paradigm shifts in IC packages and packaging options. Area array packages, in particular, the Ball Grid Array (BGA) began to emerge that more effectively addressed increasing chip I/O count. Ceramic packaging for high performance circuits (microprocessors digital signal processors) gave way to organic based packages, the plastic BGA (PBGA), offering a more favorable solution to package cost. And the hybrid circuit suddenly became a multichip module!

Over the past 15 years the author has developed and presented professional development courses at various technical symposia as well as on-site at semiconductor, component and equipment manufacturers and materials suppliers facilities. The courses have covered topics that make up the electronic manufacturing arena focusing on packaging and assembly of the integrated circuit.

This book evolved from these courses and discusses the many changes that have taken place not only with the physical package itself but also the currently available packaging options and assembly technologies. It is intended to serve as an *introduction* to IC packaging and assembly providing sufficient coverage to afford a working knowledge of the basic concepts and technologies. The book is intended for personnel new to the industry and, those indirectly involved in electronics manufacturing such as upper management, quality assurance, procurement, marketing and sales, and equipment manufacturers and material suppliers. For those directly involved the book can serve as a useful *overview* of new and emerging technologies.

The First Chapter is discussion of electronic manufacturing that basically describes the packaging and assembly of the integrated circuit. It identifies the various levels of microelectronic assembly, i.e., Level 1.0 interconnects – chip to package and Level 2.0 – chip or package to a substrate board and the packaging options, – single chip, multichip and chip on board.

The Second Chapter briefly reviews the integrated circuit manufacturing process and the *applicability* of much of the procedures and practices to IC packaging and assembly. It highlights the significance of a cleanroom operating environment and the photolithographic process in particular, as a model for implementing a proven high yield cost effective manufacturing technology.

Subsequent Chapters 3 and 4, discuss the trends in the IC package, the Chip Scale Package, and Wafer Level Packaging. Chapter 5 covers Multichip Packaging and the various sub-classifications – the hybrid circuit, the multichip module, System in Package, System on Packaging and the rapidly developing 3-D Packaging that includes stacking of both multiple die and packages.

Working with bare die as opposed to package devices is discussed in Chapter 6 and covers the subject of Known Good Die or KGD. It presents the concerns associated with bare die and multichip applications and the problem related to the lack of sufficient electrical testing of unpackaged die to insure the device meeting full electrical specifications. Various approaches to resolving this problem and providing for Known Good Die are discussed.

The assembly of a bare die onto an organic board, Chip on Board (COB) is covered in Chapter 7. Implementation and incorporation into Surface Mount Assembly lines and concerns are included. A "packageless packaging" approach makes it a viable packaging option offering both increased component density and an enhanced reliability at the Level 2.0 printed circuit board (PCB) assembly.

The Level 1.0 interconnect technologies are covered in subsequent chapters, C&W Assembly in Chapter 8, TAB in Chapter 9, and Flip Chip Bumping and Assembly, Chapter 10 and 11 respectively.

The last four chapters, 12 through 15, cover the manufacturing technologies, namely Thin Film, Thick Film, Cofired Ceramic and the Organic Laminate Technology, for packages – SCP and MCP, and High Density Interconnect (HDI) substrates. The Thin Film process technology is highlighted as the leading technology in meeting the challenges that arise with the packaging and assembly of current and future integrated circuits. It basically emulates the IC manufacturing and therefore has the inherent capability for achieving very fine line conductor circuitry and the high wiring density required for high density interconnects supporting Levels 1.0 and 2.0. The application of the Thin Film Technology to Thick Film, Cofired and Laminate, to further enhance the overall advantages of each is also discussed. Chapter 15 presents a discussion of a combined Thin Film and Laminate process (Build Up Technology, BUT) as a key enabler for Level 2.0 interconnect substrates that adequately accommodates all current and future IC packaging and assembly technologies.

Acknowledgements

I was fortunate in having spent my early years in the electronics industry at RCA working on materials and process development supporting the early manufacture of both the transistor and the integrated circuit that followed. I am indebted to my mentor during those early years, the late Arnold Rose, who guided me and provided me the opportunity to become deeply involved in the many process technologies that are still part of IC manufacturing.

Over the years that followed there were many individuals who help expand my areas of expertise and made it possible for me to write this book. There were and are many and to attempt to recognize everyone would be nearly impossible and would add many pages to this book. And I am certain I would be missing many as well. They come from all areas of industry and include: component manufacturers, equipment manufacturers and material suppliers, manufacturer reps and of course, my colleagues in consulting.

There are several however that I must acknowledge since they were particularly helpful in bring this book to fruition. In particular I am extremely thankful to Richard Brown, an industry consultant, author, instructor of professional development courses who provided invaluable insight. I am most grateful for the many discussions, his suggestions and critiques he provided that were so helpful.

I must also recognize and thank the following all of whom contributed in many and varied ways: Russ Atkinson, Avid Associates; Lee Levine, K&S; Tom Terlizzi, Aeroflex Plainview Inc.; Ray Fillion, GE Global Research; and Bruce Romenesko, Johns Hopkins University, Applied Research Laboratory.

I would be remiss if I didn't also thank the many companies that granted permission to use the copyrighted photographs, figures and tables used in the book. Finally, I want to thank the editorial staff at Springer without whose help there simply would not be any book.

In all probability I omitted several individuals who also made valuable contributions and for this I am truly sorry. I thank them "in absentia".

About the Author

A graduate of Fordham University with a BS in Physics Bill has had extensive experience in Microelectronics covering semiconductor processing and assembly, hybrid circuits, and PWB fabrication and assembly. He began his career with RCA Semiconductor Division and subsequently worked for General Electric and Lockheed Electronics. While at RCA he was awarded six U.S. patents covering wafer processing and semiconductor assembly. At General Electric he was a staff engineer and consultant for hybrid circuits and PWB manufacturing.

As Manager of Advanced Development at Lockheed, he was directly responsible for the design, construction, and operation of a state of the art Microelectronic Packaging facility supporting research, development, and manufacture of advanced hybrid circuits and multichip modules.

He became an independent consultant in 1988. His clients have included material suppliers, assembly equipment manufacturers, and component manufacturers.

His consulting activities has included work at NASA Headquarters in Washington D.C. where he provided technical expertise and assistance in developing an Advanced Integrated Circuit Packaging and Assembly Program.

Bill specializes in packaging and assembly, focusing on high density substrate manufacturing, and chip assembly including flip chip and chip scale packaging.

His company offers assistance in technology assessment and implementation, and specializes in technical audits of manufacturing operations directed towards yield improvement and reliability enhancement.

He has developed several educational and training courses which are offered at various national and international symposia and on-site presentations.

He is an active member of IMAPS where he is a Fellow of the Society and Past President of the Garden State Chapter.

1 Electronic Manufacturing and the Integrated Circuit

1 — MICROELECTRONICS AND THE TRANSISTOR [1]

The "Microelectronics Age" essentially began in 1947 with the invention of the transistor at Bell Laboratories. This historic solid state device was capable of both amplifying and switching (on/off) electrical signals. Its introduction spawned many new electronic products featuring major changes affecting end product characteristics, performance, and reliability.

The first transistor was based on the semiconductor Germanium (Ge), and became commercially available in the early 1950s. Transistors based on the superior properties and manufacturability of silicon (Si) followed later in the decade replacing Ge in almost all applications.

The overall impact of the transistor in the marketplace was immediate with rapid growth in high volume production. Compared to the then active electronic component, the vacuum tube, the transistor was significantly smaller and lighter, and required a considerably lower level of power for operation. Transistors made possible a quantum jump in electronic product *miniaturization*. Early applications were in the consumer market and included portable radios and hand-held calculators.

Use of the transistor as a switching device lead to early applications in the computer industry This quickly accelerated further development of the transistors highlighted by higher operating frequencies and faster switching speeds.

1.1 — The Integrated Circuit and Moore's Law (2-5)

A little over a decade after the transistor went into production, a major development in solid state device technology occurred with the invention of the Integrated Circuit (IC). Co-invented by Jack Kilby of Texas Instruments and Bob Noyce of Fairchild Semiconductor in 1958, the IC consisted of multiple transistors interconnected on a single silicon die.

The IC went into production in the 1960s. Like the transistor, IC manufacturing experienced an equally rapid growth characterized by the introduction of ICs with increasing transistor count and functionality.

The number of transistors on the IC obviously determined the IC's ultimate level of functionality. It therefore represented another quantum jump in miniaturization while at the same time provided a major increase in electrical functionality and performance.

In 1965, Gordon Moore, at Fairchild at the time, published a paper in which he noted that the IC's "complexity" was roughly doubling every year of manufacture and predicted that it would continue to do so in the future. This subsequently became known as Moore's Law. Over the years Moore's Law has undergone some modification, namely in the timeframe for doubling and the definition of "complexity" (Figure 1-1).

In 1971 another significant but related event occurred with the invention of the microprocessor [6] at Intel Corporation. Basically, a "computer on a chip", its introduction had a far reaching impact on the entire electronics industry. The demand for microprocessors with increased performance was immediate and a driving force in a continuing and intensive development effort of all aspects of the technology covering IC design, manufacturing, and applications engineering.

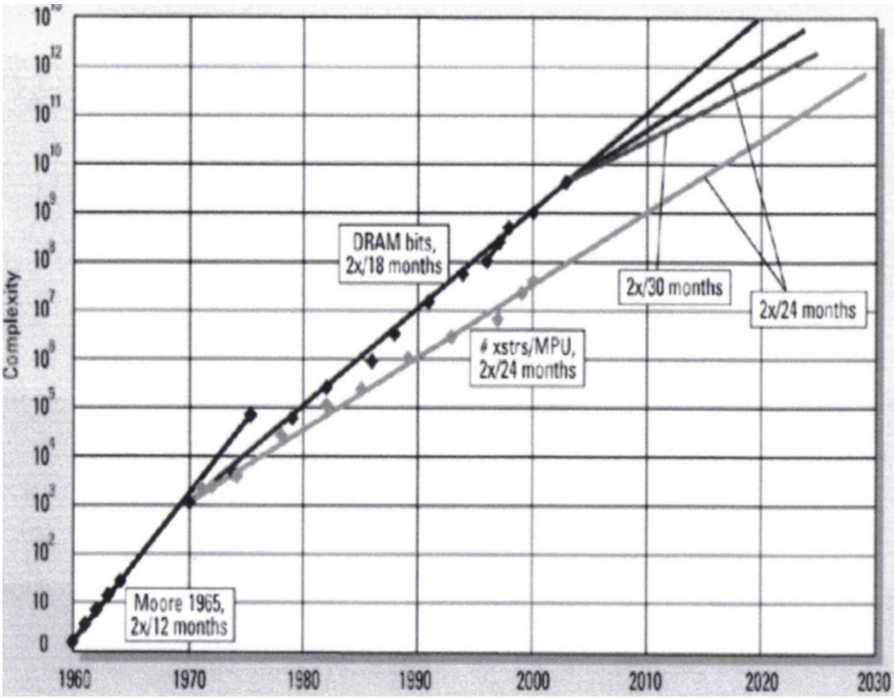


Figure 1-1. Moore's Law [3]

With the introduction of the microprocessor and the Dynamic Random Access Memory (DRAM) during the 1970s, some parameter modifications to Moore's Law were needed. In particular, the timeframe for doubling is a best fit at 24 months for the microprocessor and 18 months for the DRAM. In addition, for the microprocessor "complexity" indicates the number of transistors per device while for the DRAM it is the number of bits per device. Further modifications with Moore's Law are expected in the future particularly with the DRAM extending the doubling to 24 months and possibly 30 months.

The single transistor device of the early ‘50s is now, slightly over 50 years later, an IC containing literally millions of transistors and expected to reach a billion transistors by the end of the decade.

1.2 — Electronics Manufacturing and the Technology Drivers

Perhaps not surprising, the IC as well as the marketplace (i.e. end product) are the drivers that influence the packaging and assembly technologies that are the heart of the manufacturing process. It is a marketplace for example, that during the last decade has experienced a tremendous increase in the number, variety and the availability of electronic products. All have taken advantage of the ever-increasing performance potential of the integrated circuit. The marketplace can be segmented into two types of product. One is driven primarily by the requirement for high performance, and the other by size and cost. The latter is represented by the high volume but low cost products, all requiring portability, such as cell phones, camcorders, laptops, digital cameras, personal digital assistant (PDAs) and the like. The high-performance, high-reliability products are typically those used for avionics, space, and military applications.

The life cycle of many of the products, particularly in the high volume consumer categories, is on the order of one year or less. To be marketable and remain competitive, however, next generation models must be “smaller, better, and cheaper”. This requirement has in fact become the mantra of the electronics industry and strongly influences product manufacture impacting both the packaging and assembly of ICs.

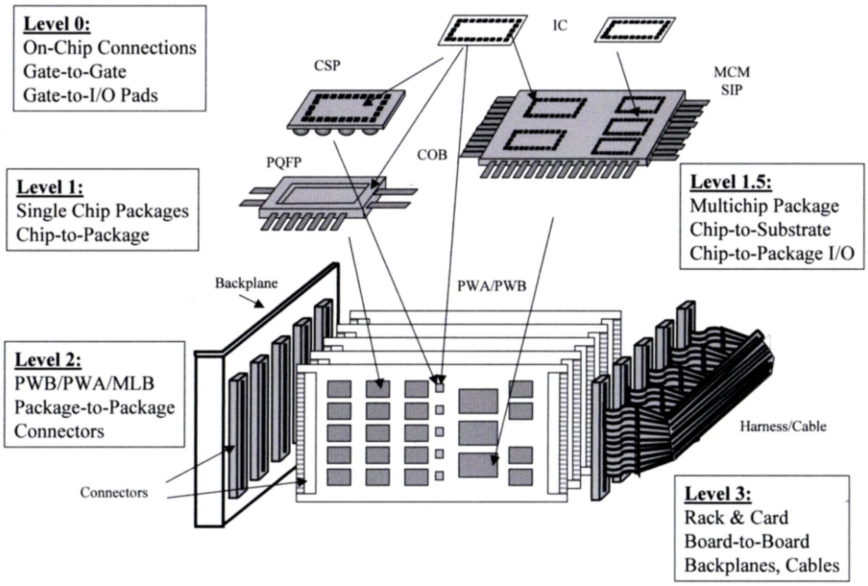
1.2.1 — The Manufacturing Process [7,8]

The Electronics Manufacturing Process is graphically represented in Figure 1-2. The process starts with the IC and takes it through a series of steps, referred to as “Packaging Levels” or “Levels of Interconnection” involving assembly of both bare die and packaged components.

Successful manufacturing ideally means realizing chip level performance in the end product. It therefore requires attention to the following:

- Identifying and accommodating the electrical, mechanical and thermal requirements inherent in the IC, and
- Selecting those manufacturing technologies that incorporate attributes that will contribute to an end product that is “smaller, better, and cheaper”.

Meeting this challenge is a continuing and on going effort. It has resulted in the IC’s physical package, as well as the assembly of both the die and the package, undergoing paradigm shifts in both materials and process technologies.



(Courtesy General Electric Global Research)

Figure 1-2. The Electronic Manufacturing Process

1.2.2 — Packaging Options

The graphical representation of the process shows three packaging options or paths: Single Chip Packaging (SCP), Multichip Packaging (MCP), and Chip on Board (COB). SCP (Figure 1-3(a)) has been the industry's standard from the beginning, while MCP (Figure 1-3(b)) is a variant involving assembling multiple die in a single package. COB (Figure 1-3(c)) is an option that basically eliminates the packages with bare die assembled directly to the second level interconnect substrate, the printed wiring board (PWB).

The three packaging scenarios each offer specific advantages and disadvantages. Selection of a particular option is dependent on several factors based on both the IC and the end product requirements. These are discussed in Chapters 3, 5, and 7, respectively.

1.2.3 — Levels of Interconnect/Packaging

The manufacturing process for mostly all electronic products follows the three "Packaging Levels" indicated. They are described as:

- ✓ **Level 1.0**—covering the connection (assembly) of the die to a package (SCP) or substrate (MCP).

The interconnect technologies, Figure 1-4, include:

(a) Chip and Wire—C&W
(b) Tape Automated Bonding
(c) Flip Chip (FC) Bonding

Each of these is discussed in detail in Chapters 8, 9, 10 and 11.

When multiple die are connected to a package/substrate, (**Level 1.5** in Figure 1-2), the substrate must provide the necessary interconnections between die. This is accomplished by an embedded conductor interconnect network within the package. These package/substrates are manufactured using thick film/cofired ceramic, thin film or laminate printed wiring board (PWB) processes that are discussed in chapters 12, 13, 14 and 15, respectively.

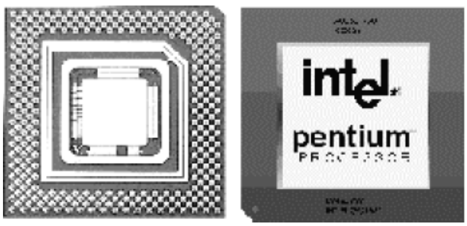


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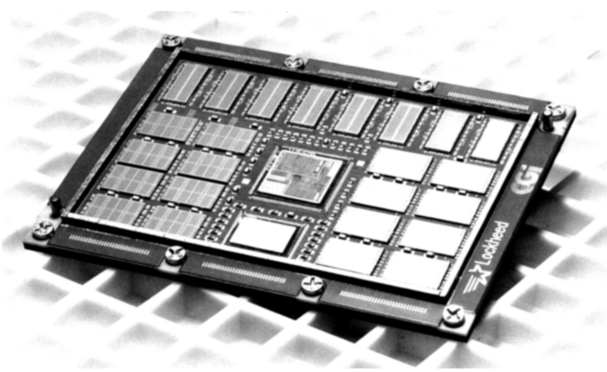
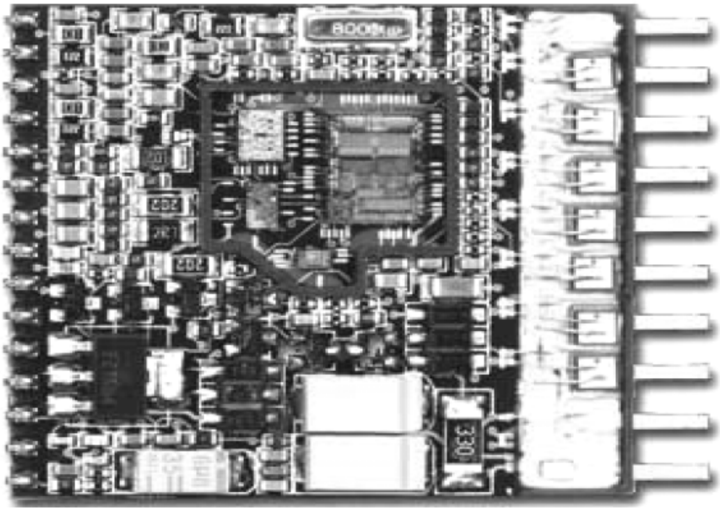
Figure 1-3(a). Single Chip Packaging



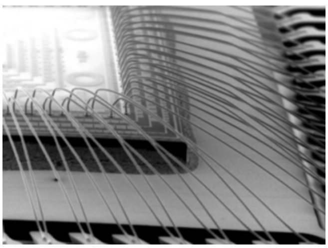
(Courtesy Lockheed Martin)

Figure 1-3(b). Multichip Packaging



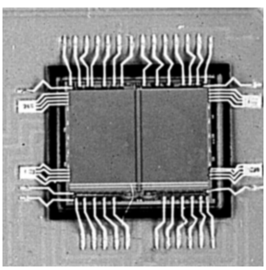
(Courtesy Stellar Microelectronics)

Figure 1-3(c). Chip On Board



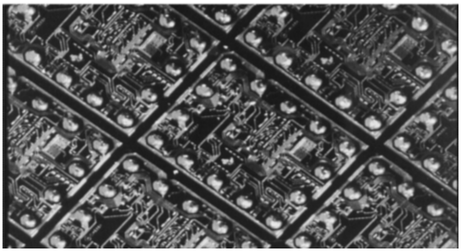
(Courtesy Kulicke & Soffa)

Figure 1-4(a). Chip & Wire



(Courtesy International Micro Industries)

Figure 1-4(b). TAB

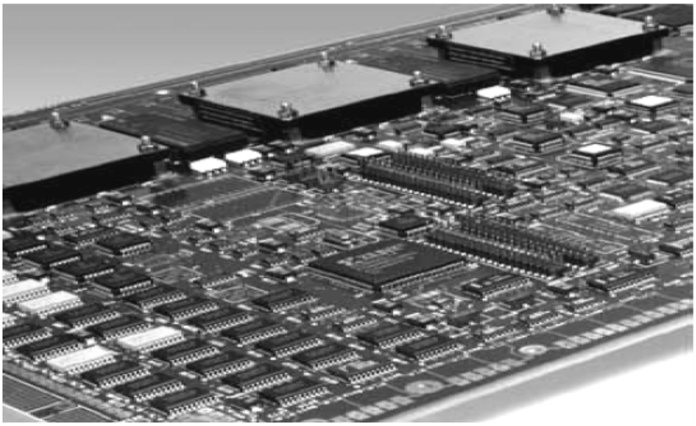


(Courtesy IBM Corp.)

Figure 1-4(c). Flip Chip

- ✓ **Level 2.0**—refers to the interconnection of multiple bare die and/or packages through a substrate interconnect. This is typically a printed wiring board (PWB), an organic based substrate but can also be ceramic. The board, with components attached, is referred to as a printed circuit board (PCB) or a printed wire assembly (PWA). (Figure 1-5).

- ✓ **Level 3.0**—refers to assembly to a PWB (motherboard) of multiple Level 2.0 board assemblies. Again, the motherboard provides the interconnections between assemblies.



(Courtesy IBM Corp.)

Figure 1-5. Printed Circuit Board (PCB) or Printed Wiring Board Assembly (PWBA)

1.3 — A Technology Driver—The Integrated Circuit

Obviously packaging must address the needs of the IC, accommodating the performance and/or reliability. In doing so, not only the packaging, but also the device assembly is impacted.

The IC has changed significantly over the years and will continue to do so. As a consequence changes in the packaging and associated assembly processes were necessary and have occurred. Knowing future device needs should therefore be equally important.

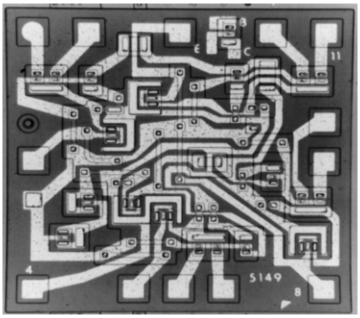
1.3.1 — About the Integrated Circuit

Silicon (Si), Gallium Arsenide (GaAs) and Silicon Germanium (SiGe) are the semiconductor materials currently available and used in IC manufacturing. However, the overwhelming majority of ICs are still silicon based.

Fabrication of the IC involves sophisticated materials, processes, and highly specialized and dedicated equipment that have been developed over a period of 40 years. Because the IC contains features as small as tenths of micrometers (microns, µm) and nanometers (nm), an ultraclean manufacturing environment is necessary to minimize the presence of the many "contaminants" that can adversely affect the manufacture. Yield is a critical process metric that dictates the eventual cost of these functionally dense and sophisticated devices.

1.3.2 — The Integrated Circuit—Physical Characteristics

Figure 1-6 is a photograph of an IC manufactured in the late '60s with minimum feature size in the 10-micrometer range. Individual transistors are readily discernible under low magnification interconnected by a single level of aluminum (Al) metal. The minimum line width for the Al interconnect is 20 micrometers. Aluminum metallization interconnects the many transistors that make up an IC.



(Courtesy RCA)

Figure 1-6. IC circa 1970, Single Level Al Metallization ≈ 20 Micrometers Minimum Line Width