Metric-Driven Design Verification

An Engineer's and Executive's Guide to First Pass Success

Hamilton B. Carter
Shankar Hemmady

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Table of Contents

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Hamilton Carter has been awarded 14 patents in the field of functional verification. The patents address efficient sequencers for verification simulators, MESI cache coherency verification and component-based reusable verification systems. Carter worked on verification of the K5, K6, and K7 processors and their chipsets at AMD. He staffed and managed the first functional verification team at Cirrus Logic and has served as a manager, engineer, or consultant on over 20 commercial chips and EDA projects.

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Shankar Hemmady is a senior manager at Cadence responsible for verification planning, methodology, and management solutions. Mr. Hemmady has verified and tested, or managed the functional closure of over 25 commercial chips over the past 18 years during his tenure in the industry as an engineer, manager, and consultant at 12 companies, including AMD, Cirrus Logic, Fujitsu, Hewlett Packard, Intel, S3, Sun, and Xerox.

Dedications

To my Parents who removed the word "cannot" from my vocabulary!

Hamilton Carter

To Seema, Shona, & Anand who make each and every moment a special one!

Shankar Hemmady

Preface

With the alarming number of first pass silicon functional failures, it has become necessary for all levels of engineering companies to understand the verification process. This book is organized to address all verification stakeholders at all levels of the engineering organization. The book is targeted at three somewhat distinct audiences:

- *Executives*. The people with their jobs on the line for increasing shareholder value.
- *Project, design, and verification managers*. The people responsible for making sure each design goes out on time and perfect!
- *Verification and design engineers*. The innovators responsible for making sure that the project actually succeeds.

The book is divided into three parts corresponding to its three audiences. The level of technical depth increases as the book proceeds.

Part I gives an overview of the functional verification process. It also includes descriptions of the tools that are used in this flow and the people that enable it all. After outlining functional verification, Part I describes how the proper application of metric-driven techniques can enable more productive, more predictable and higher quality verification projects. Part I is targeted at the executive. It is designed to enable executives to ask appropriate educated questions to accurately measure and control the flow of a project.

Part I also holds value for project managers and verification engineers. It provides an overall view of the entire chip design process from a verification perspective. The chapters on a typical verification project and the overview of verification technologies will be of use to entry level verification engineers as well. This part of the book also provides a unique viewpoint on why management is asking for process data and how that data might be used.

Part II describes the various process flows used in verification. It delves into how these flows can be automated, and what metrics can be measured to accurately gauge the progress of each process. Part II is targeted at design and verification project managers. The emphasis is on how to use metrics within the context of standardized processes to react effectively to bumps in the project's execution.

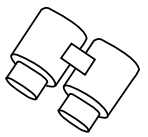
Part III's audience is the design and verification engineering team. It focuses on the actual verification processes to be implemented and executed. This section of the book is divided with respect to the various verification technologies. Each chapter on a given technology is further subdivided into sections on how to plan effectively, and how to track metrics to closure.

Entire books have been written on implementing verification using the technologies discussed in Part III. We will not reiterate what those excellent volumes have already stated, nor do we intend to reinvent the wheel (yet, we are engineers after all). Implementation details will be discussed when they will make the metric-driven techniques discussed more effective.

Part IV contains various case studies and commentaries from experts in the metric-driven verification field.

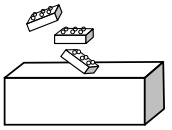
The various parts of the book can also be described as a progression of process abstractions. The layers of abstractions are "Observational Processes," "Container Processes," and "Implementation Processes."

Observational Processes



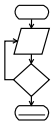
Part I looks at the verification process from an observational point of view. The various aspects of a project that should be observed are described to the reader along with informal suggestions about how to strategically manage a verification project based on these observations.

Container Processes



Part II looks at processes that are necessary regardless of the verification technology you are using; processes such as regression management, revision control, and debug. Part II describes how to implement these processes using metric-driven methodologies. It also also discusses the inter-relations of these processes.

Implementation Processes

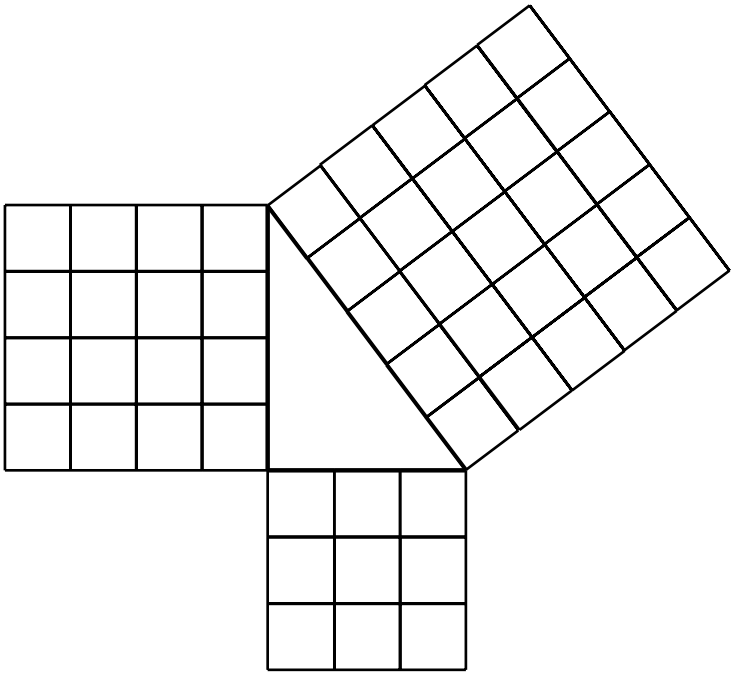


Part III describes each of the verification technologies and explores how a metric-driven methodology can be used to enhance the productivity, predictability, and quality offered by each of these technologies.

Finally, *Part IV* leaves the world of abstraction altogether and presents several concrete case studies that illustrate metric-driven processes in action. In addition to these case studies are several commentaries offered by industry experts in metric-driven methodologies.

Introduction

Legend has it that 2300 years ago, Euclid walked the beaches of Egypt with his students. They were exploring the fundamentals of a new field: geometry. Each day, Euclid would draw a new problem in the sandy shores of the Mediterranean Sea. He'd ask his students to reflect on each problem and discover what they could. One day he sketched a diagram that would come to be known as Euclid's 42nd Problem.



One of his particularly bright students worked on the diagram and came back with a simple formula:

$$a^2 + b^2 = c^2$$

This formula became so famous that it is now known simply by its discoverer's name: the Pythagorean Formula.

Pythagoras thirsted for knowledge and spent most of his life traveling the various countries of the ancient Hellenic world searching for it. In his travels, he encountered many cultures and gleaned valuable knowledge from each of them applying it to the burgeoning new field of geometry.

Today we're witnessing the birth of another new field, Metric-Driven Verification. Like Euclid, we hope to layout templates that not only illustrate the basics of this promising new field, but also inspire the reader to make even greater discoveries. Like Pythagoras, we have traveled the world searching for the best applications of this knowledge.

This book contains more than our basic understanding of the principles of metric-driven verification. The book also contains examples and experiences gleaned from many industry experts in verification and design. All of these are presented in their entirety in Part IV.

The last three chapters of Part III are about emerging technologies in the field of metric-driven verification:

- System verification
- Mixed-signal verification
- Verification of DFT hardware

These chapters use a different format. Each chapter contains a complete case study from one of the industry leaders in each of these three emerging areas.

Contributing Authors in Order of Appearance

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Jason Andrews is a project leader at Cadence Design Systems, where he is responsible for hardware/software coverification and methodology for system-on-chip (SoC) verification. He is the author of the book "Co-Verification of Hardware and Software for ARM SoC Design" and holds a bachelor's degree in electrical engineering from The Citadel (Charleston, SC) and a master's degree in electrical engineering from the University of Minnesota (Minneapolis).

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Ms. Chiavacci cofounded Yogitech in 2000. She is responsible for the mixed signal division. She worked as an analog designer from 1998 to 2000 after receiving her degree cum laude in electronic engineering at the Pisa University. Her work experiences include high-reliability systems in critical environments such as biomedical, space, and high-voltage automotive applications.

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Mr. Zarri is a verification engineer at Yogitech. He is responsible for the development of verification IPs, verification environments for many international customers, and trainings on verification methodologies. His experience includes automotive protocols such as LIN, CAN, and Flexray. He is expert in OCP protocol, a universal complete socket standard for SoC design, and has recently acquired experience in the verification of mixed signal circuits. Gabriele specialized in Microelectronics and Telecommunications with an MS from Nice Sophia-Antipolis University.

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Jean-Paul Lambrechts has over 20 years experience in leading hardware design in the networking and computer areas. His experience covers board-level hardware design, FPGA, and verification. Jean-Paul has now been with Cisco for 9 years where he has been responsible for line cards, packet forwarding engines, and layer 4–7 processor card. Jean-Paul holds a MSEE degree from the Louvain University in Belgium.

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In 1995, after obtaining his MA at the University of Erlangen and his Ph.D. in electronic engineering at Technical University of Munich, Dr. Dieckmann began working at Siemens AG. He was initially responsible for board and fault simulation. From 1997, Dr. Dieckmann gained expertise in system simulation and verification of ASICs. Since 2001, he has been in charge of coordinating and leading several verification projects employing simulation with VHDL and Specman "e," formal property and equivalence checking, emulation, and prototyping.

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Susan Peterson has been trying to escape from the EDA industry for the past 20 years, where she has spent her time listening to customers and trying to help them to solve their critical problems in various sales and marketing roles. Prior to that, she was a practicing engineer, and earned her MBA from the University of Denver.

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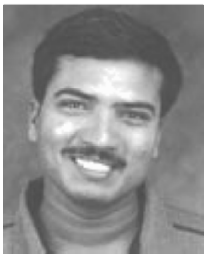
Paul Carzola is a senior consulting engineer for verification at Cadence. He received a Bachelor of Science Degree in computer engineering at Florida Atlantic University in 1995. Since then, Paul has spent the last 10 years in functional verification and the pursuit to finding effective and powerful methods to verification while making it easier and enjoyable to apply. For the past 5 years, he has served in a consulting role in the area of functional verification methodology and has seen first hand the power of a Coverage-Driven approach.



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YJ Patil is a senior verification engineer at Genesis Microchip, where he is responsible for managing the verification of digital television (DTV) controller ASICs. Prior to Genesis, Mr. Patil was a verification engineer at several technology leaders including ATI, Silicon Access Networks, and Philips Semiconductors. He was a board designer at Tektronix. Mr. Patil holds an MS in software systems from BITS Pilani, India and BE in electronics and communication from Gulbarga University, India.

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Dean D'Mello is a solutions architect at Cadence Design Systems. He works closely with key customers worldwide to deploy advanced verification technologies, and with R&D to plan, develop, and introduce new methodologies and products. Prior to Cadence, Mr. D'Mello held ASIC design and verification roles at LSI Logic, Cogency Semiconductor, and Celestica, and product and test engineering roles at IBM. Dean holds a Masters of Applied Science (MASc) in electrical and computer engineering, from the University of Toronto, Canada.

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Roger Witlox joined Philips Research Laboratories in Eindhoven, The Netherlands in 1992, where he has been working on optical coherent communications systems and access networks. Mr. Witlox was earlier involved in the development of analog laser temperature and current control system. In 2000, he joined the CTO organization at Philips Semiconductors, where he was responsible for development and support of an in-house verification tool. He has been responsible for functional verification methodologies for hardware IP and was a member of the Verification Technical Work Group of the SPIRIT consortium. In 2004, he joined the DSP Innovation Center and is currently focusing on DSP subsystems, both specification and verification.

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Ronald Heijmans studied at the Hoge School Eindhoven and graduated in 1992 in the field of "Technical Computer Science." He started his career as a PCB designer at the Philips Research Laboratories. Later, Mr. Heijmans focused on DSP algorithm design and applications for multichannel audio and speech coding. In 1999, he became a verification engineer at ESTC Philips Semiconductors, where he focused on DSP core and subsystems. Currently, as a verification architect, Ronald is defining a new environment including new verification methodologies.

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Chris Wieckardt has been a verification engineer at Philips Semiconductors, Adelante Technologies and NXP Semiconductors in Eindhoven, The Netherlands since 2000. Prior to Philips, Mr. Wieckardt was a digital design engineer at Océ Research and Development, Venlo, The Netherlands.

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Frank Ghenassia is Director of the System Platforms Group in the HPC (Home, Portable, and Communication) sector at STMicroelectronics. Mr. Ghenassia focuses on IP/SOC verification, architecture definition, platform automation, and embedded software development based on high-level modeling approaches. He joined STMicroelectronics in 1995 and has worked on OS development, software debuggers, and system-to-RTL design flow activity. Mr. Ghenassia received his MS in electrical engineering in Israel.

Dr. Joseph Bulone

Joseph Bulone manages a team that provides central services in hardware emulation to STMicroelectronics divisions. Joseph defines and provides hardware-accelerated platforms for IP/SoC verification and software development. He joined the Central R&D division of STMicroelectronics in 1989, and was initially involved in the design of ATM chips. He began working on hardware emulation in 1993. He has been in charge of video chip validation, and hardware software co-design. He holds a Ph.D. in microelectronics from the Institut National Polytechnique de Grenoble, France.

Part I
Analyzing and Driving Verification: An Executive's Guide

Chapter 1
The Verification Crisis

If everything seems under control, you're not going fast enough.
– Mario Andretti

The time is at hand! This book proposes to revolutionize verification engineering! "It's rote work," you say? Can't be done!? Well get ready to be surprised and even mystified!

What is Verification?

So what is verification? Simply put, it is a process that ensures the *implemented device* will match the *product intent* defined for the device prior to sending the device for manufacturing. Notice the selection of words in the previous sentence. It didn't mention the device specification, or the device requirements. Every document that corresponds to the device (such as a specification or requirements list), is merely a translation of the actual intent of the device functionality as originally conceived. This is an important distinction. All the methodologies in this book will have at their heart, the goal of ensuring that the device does what it was *intended* to do, not necessarily what it was documented to do. Quite frequently, the first defects we find are specification issues, *not* design defects. Figure 1.1 shows the many translations of intent.

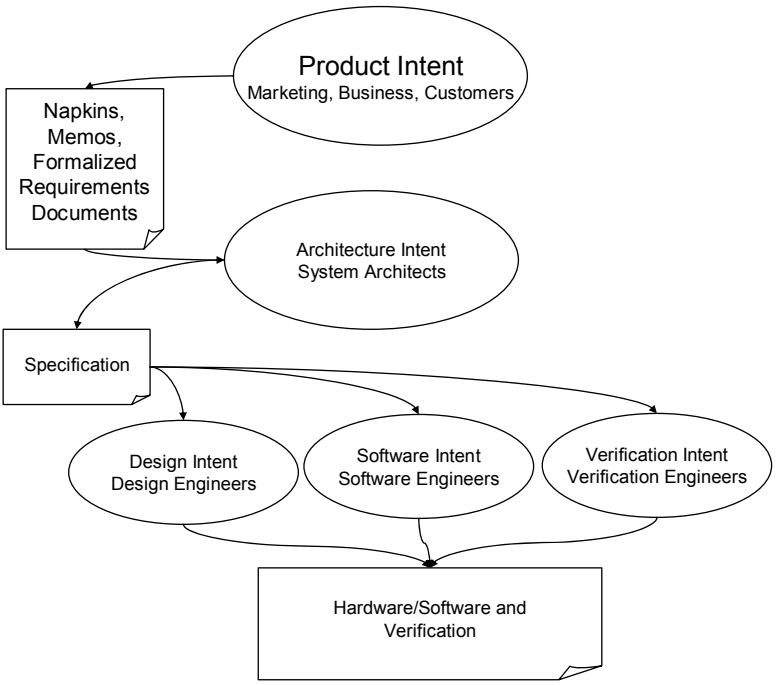


Figure 1.1 Intent Translation

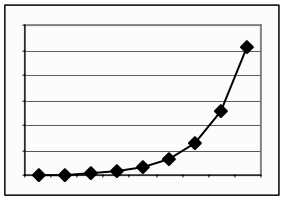
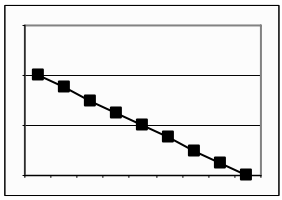
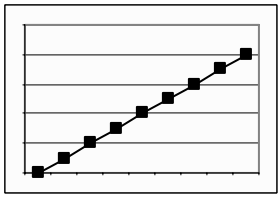
The Crisis

The size of designs is increasing. Market window size is decreasing. These factors combine to create a rapidly increasing cost of failure (Table 1.1).

As designs become more and more complex and market windows become tighter and tighter, verification becomes crucial. More and more devices are now going directly into the mainstream consumer market. The mainstream consumer expects all features of a device to work properly. If they don't the consumer will return the device, get their money back, and go with a different supplier. There's really no room for error.

Rapidly shrinking silicon geometries have been both a blessing and a curse. It is possible to build more powerful, feature rich devices than ever before. However, along with all the new features comes an exploding multidimensional space for verification requirements.

Table 1.1 Design Size, Market Window, and Cost of Failure

Design size	
Market window	
Cost of failure	

For example, consider a “simple” digital sound output port. The port can output sound in mono or stereo mode. In stereo mode, the sound frames can be transmitted with either the left channel or right channel first. Sound can be output in 8-, 12-, 16-, or 24-bit resolution. The gap between sound samples can be 0, 1, or 2 bits. In addition to all these specifications on the format of the output stream, the port can also be configured to use five different FIFO sizes for buffering input data and can run in either polling or interrupt-driven mode. This simple output port has over 240 functional combinations that must be verified. If even one of these combinations fails and it’s the combination that our key customer had to have, we’re facing a costly silicon respin.

Respins are expensive at more than a million dollars a piece, but in today’s accelerated business atmosphere, there are even worse repercussions. A nonfunctional first tape-out can result in the loss of a job, the closing of a company and the ruin of a career. Clearly, it’s important to get verification right the first time. By getting verification right the first time, companies can save millions of dollars on

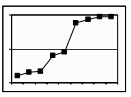
respins alone. Then they can make millions more by hitting their market windows on time.

The Need for Metric-Driven Processes

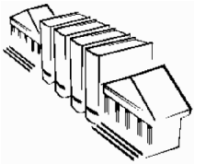
So, how do we solve the verification crisis? How do we ensure that our designs will go out "first silicon clean" every time? With a cultural change and newly available technology, it's actually quite simple.

For years verification has been done in a rather haphazard manner. Each company or project team within a company slowly assembled their own best practices. Some project teams developed very successful, rigorous processes for making sure verification was implemented and managed correctly. Others executed on their verification projects in a haphazard way. Still other teams did verification merely as an afterthought as the project started to wind up. The process-oriented teams had far higher success rates.

Effective project closure tracking was also frequently ignored. Here again, many disparate techniques have been documented and used. Some of these techniques included bug rate tracking, code coverage, functional coverage, and everyone's favorite: "Tape it out because management said so!"



By objectively tracking important metrics, management can allocate resources more effectively, better predict the schedule of the project, and ensure a higher quality of the final product. Management and engineering productivity can be further enhanced if these objective metrics can be measured automatically. This book will show how to define what metrics are important to measure, how to measure those metrics automatically, and how to most effectively utilize those metrics to streamline engineering processes.



While other disciplines have reaped great rewards in productivity and effectiveness by moving to well-documented, accepted and established methodologies, ASIC design engineering is one of the few

engineering activities where a "cowboy" mentality is still accepted and even expected! In other areas where large teams integrate work flows, processes have been defined for years. Accounting has the FASBs, manufacturing has ISO standards. No one argues about the format of a ledger entry, they worry about more important things like the actual analysis of the financial data. No one argues about where the header block on an architectural drawing should be placed or on the size of the page. They concentrate their effort on the actual architectural design.

Let's look at a small example of why tracking progress is so crucial to any activity. Imagine that on your rare Sunday off, you sit down in front of the TV, cold beer in hand and turn on your favorite sporting event. As the players enter the field, we hear the commentators begin to speak.

"Jack, someone will definitely win this game today. Both teams have entered the field with that goal in mind, and we feel it will definitely happen."

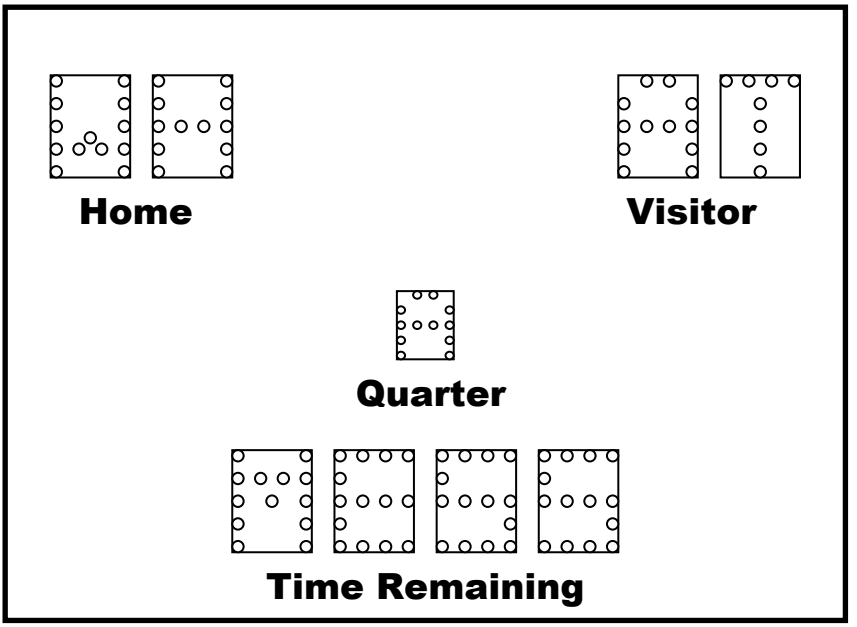
"Folks we're really not certain what two teams are playing today, but we've got someone looking into it and we'll have that information to you as soon as we can."

"After all, what is important is that the teams play often and hard, right? We expect to see lots of really hard effort put in today."

"Ah, and the players have begun. There's a really tall player (Fred get me his name), carrying the ball down the field. Oh! He's been tackled by a rather small chap (Fred, we're going to need another name!) And, the team is up and carrying the ball again! Did anyone think to find out how many yards to first down? Folks, we'll get you more stats right after this commercial break!"

When we watch sports, we want to know everything about the game from the first instant, right? We don't give the teams respect for beginning the game immediately and running around willy-nilly with the ball when we know nothing about the game, do we? Then

why are we so content to execute on our engineering projects in this manner?



When we watch our sporting event, we expect to have a multitude of information at our fingertips:

- The amount of time left in the game
- The score of the game
- Progress toward the current goal
- The history and statistics of the player that most recently carried the ball

As the coach of the team, we'd expect to have all the information above and much more like:

- What to do when the opposing team does something we don't expect, like fumbling the ball
- The statistics of each of the players on the opposing team
- A plan for how to counter each of the other team's plays

- Information about how our players match up vs. the players on the other team
- How each player on both teams is playing vs. their statistics

To accumulate this data, we'd employ an entire coaching staff to gather and analyze data both before the game and as the game progressed. Before the game, we'd build a plan of what we expected to do based on available data. As the game progressed we'd constantly adjust our plan to work with the situation at hand. And that's exactly how we should be executing our engineering projects.

But maybe we don't have to hire that pricey coaching staff. Maybe we can automate that part.

The message so far has been:

- Verification is hard! Brutally hard!
- If we're going to successfully verify today's designs we *have* to move to a process-oriented approach.
- Process isn't enough, we also have to be able to measure the output of our processes and use that information to adjust our direction.

Using emerging technology, we're going to show you how to move to a metric-driven, process-oriented verification flow. In Chapter 2, we'll outline exactly what these processes look like and how we measure and use process metrics. And don't worry, *we will* replace all those coaches with an automated system that will automatically capture and analyze metrics.

Now we'll spend a little bit of space explaining the logistics of the book so you can get the most out of it.

The Verification Hierarchy of Needs

In the year 1943, Maslow unveiled the hierarchy of needs to the world. This hierarchy described a set of basic needs that humans strive after. Each new level of needs can be reached only after the