FinFETs and Other Multi-Gate Transistors

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Preface

The adoption of Silicon-on-Insulator (SOI) substrates for the manufacturing of mainstream semiconductor products such as microprocessors has given SOI research an unprecedented impetus. In the past, novel transistor structures proposed by SOI scientists were often considered exotic and impractical, but the recent success of SOI in the field of microprocessor manufacturing has finally given this technology the credibility and acceptance it deserves.

The classical CMOS structure is reaching its scaling limits and "end-of-roadmap" alternative devices are being investigated. Amongst the different types of SOI devices proposed, one clearly stands out: the multigate field-effect transistor (multigate FET). This device has a general "wire-like" shape with a gate electrode that controls the flow of current between source and drain. Multigate FETs are commonly referred to as "multi(ple)-gate transistors", "wrapped-gate transistors", "double-gate transistors", "FinFETs", "tri(ple)-gate transistors", "Gate-all-Around transistors", etc. The International Technology Roadmap for Semiconductors (ITRS) recognizes the importance of these devices and calls them "Advanced non-classical CMOS devices".

There exists a number of textbooks on SOI technology. Some of these books tackle the subject of multigate FETs, but there is no book that contains a comprehensive description of the physics, technology and circuit applications of this new class of devices. This is why we decided to compile chapters dedicated to the different facets of multigate FET technology, written by world-leading experts in the field. This book contains seven chapters:

- *Chapter 1:* ***The SOI MOSFET: from Single Gate to Multigate***, by Jean-Pierre Colinge, is a general introduction that shows the evolution of the SOI MOS transistor and retraces the history of the multigate concept. The advantages of multigate FETs in terms of electrostatic integrity and short-channel control are described, and the challenges posed by the appearance of novel effects, some of quantum-mechanical origin, are outlined.

- *Chapter 2:* ***Multigate MOSFET Technology***, by Weize (Wade) Xiong, outlines the issues associated with multigate FET manufacturing. This chapter describes thin-fin formation techniques, advanced gate stack deposition and source/drain resistance reduction techniques. Issues related to fin crystal orientation and mobility enhancement via strain engineering are tackled as well.

- *Chapter 3:* ***BSIM CMG: A Compact Model for Multi-Gate Transistors***, by Mohan Vamsi Dunga, Chung-Hsun Lin, Ali M. Niknejad and Chenming Hu, describes the physics behind the BSIM-CMG (Berkeley Short-channel IGFET Model – Common Multi-Gate) compact models for multigate MOSFETs. A compact model serves as a link between process technology and circuit design. It is a concise mathematical description of the device physics in the transistor. Some simplifications in the physics, however, can be made to enable fast computer analysis of device/circuit behavior.

- *Chapter 4:* ***Physics of the Multigate MOS System***, by Bogdan Majkusiak, analyzes the electrostatics of the multigate MOS system. Using quantum-mechanical concepts, it describes electron energy quantization and the properties of a one-dimensional and two-dimensional electron gas. The effects of tunneling through thin gate dielectrics on the electron population of a device are studied as well.

- *Chapter 5:* ***Mobility in Multigate MOSFETs***, by Francisco Gámiz and Andrés Godoy, analyzes the behavior of electron mobility in different multigate structures comprising double-gate transistors, FinFETs, and silicon nanowires. Mobility in multiple gate devices is compared to that in single-gate devices and different approaches for improving the mobility in these devices, such as different crystallographic orientations and strained Si channels, are studied.

- *Chapter 6:* ***Radiation Effects in Advanced Single- and Multi-Gate SOI MOSFETs***, by Véronique Ferlet-Cavrois, Philippe Paillet and Olivier Faynot, describes the effects of ionizing radiations such as gamma rays and cosmic rays on SOI MOSFETs. These effects are extremely important in military, space and avionics applications. Multi-gate FETs show exceptional resistance to total-dose and single-event effects and could become the new standard in radiation-hardened electronics.

- *Chapter 7:* ***Multigate MOSFET Circuit Design***, by Gerhard Knoblinger, Michael Fulde and Christian Pacha, describes the interrelationship between the multi-gate FET device properties and elementary digital and analog circuits, such as CMOS logic gates, SRAM cells, reference circuits, operational amplifiers, and mixed-signal building blocks. This approach is motivated by the observation that a cost-efficient, heterogeneous SoC integration is a key factor in modern IC design.

Jean-Pierre Colinge, August 2007

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1 The SOI MOSFET: from Single Gate to Multigate

Jean-Pierre Colinge

1.1 MOSFET Scaling and Moore's Law

In 1965 Gordon Moore published his famous paper describing the evolution of the transistor density in integrated circuits. He predicted that the number of transistors per chip would quadruple every three years.[1] This prediction became known as Moore's law and has been remarkably followed by the semiconductor industry for the last forty years (Figure 1.1).

Since the early 1990's semiconductor companies and academia have teamed up to predict more precisely the future of the industry. This initiative gave birth to the International Technology Roadmap for Semiconductors (ITRS) organization.[2] Every year, the ITRS issues a report that serves as a benchmark for the semiconductor industry. These reports describe the type of technology, design tools, equipment and metrology tools that have to be developed in order to keep pace with the exponential progress of semiconductor devices predicted by Moore's law. Figure 1.1 shows the evolution of the number of transistors per chip predicted by the ITRS 2005 for DRAMs and high-performance microprocessors.

The semiconductor industry's workhorse technology is silicon CMOS, and the building block of CMOS is the MOS transistor, or MOSFET (MOS field-effect transistor). In order to keep up with the frantic pace imposed by Moore's law, the linear dimensions of transistors have reduced by half every three years. The sub-micron dimension barrier was overcome in the early 1980's, and in 2010 semiconductor manufacturers will produce transistors with a 20nm gate length on a regular basis. Since the first

integrated circuit transistors were fabricated on "bulk" silicon wafers. At the end of the 1990's, however, it became apparent that significant performance improvement could be gained by switching to a new type of substrate, called SOI (Silicon-On-Insulator) in which transistors are made in a thin silicon layer sitting on top of a silicon dioxide layer. SOI technology brings about improvements in both circuit speed and power consumption. In the early 2000's major semiconductor companies, including IBM, AMD and Freescale, began manufacturing microprocessors using SOI substrates on an industrial scale. SOI devices offer the advantage of reduced parasitic capacitances and enhanced current drive.

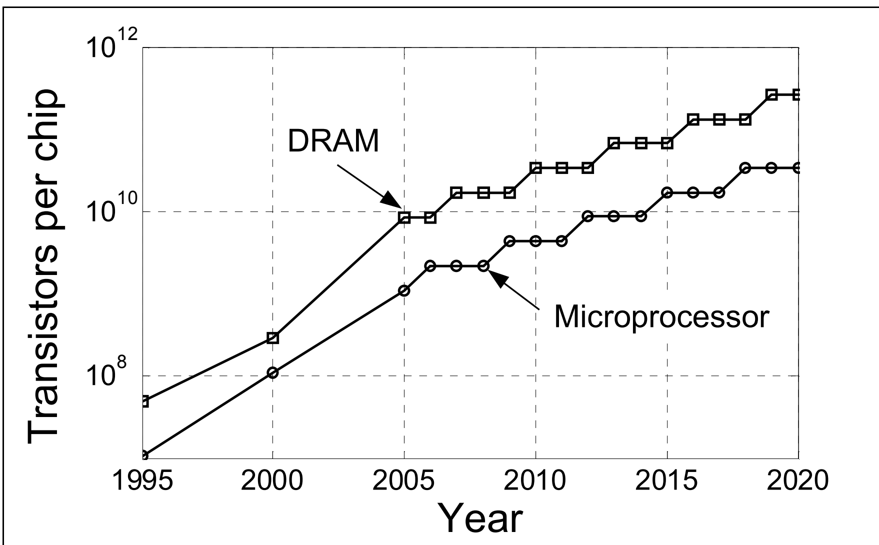

Fig. 1.1. Evolution of the number of transistors per chip (Moore's law) predicted by the ITRS 2005 for DRAMs and high-performance microprocessors.

1.2 Short-Channel Effects

As the dimensions of transistors are shrunk, the close proximity between the source and the drain reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region, and undesirable effects, called the "short-channel effects" start plaguing MOSFETs. For all practical purposes, it seems impossible to scale the

dimensions of classical “bulk” MOSFETs below 20nm. If that limitation cannot be overcome, Moore’s law would reach an end around year 2012.

There exists a simple tool, called the Voltage-Doping Transformation model (VDT) [3], that can be used to translate the effects of shrinking device parameters such as gate length or drain voltage into electrical parameters. In the particular case of the Short-Channel Effect (SCE) and the Drain-Induced Barrier Lowering (DIBL), the following expressions can be derived from the VDT model: [4]

$$SCE = 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{bi} \equiv 0.64\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EI\,V_{bi} \tag{1.1}$$

and

$$DIBL = 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{DS} \equiv 0.80\frac{\varepsilon_{Si}}{\varepsilon_{ox}}EI\,V_{DS} \tag{1.2}$$

where L_{el} is the electrical (effective) channel length, V_{bi} is the source or drain built-in potential, t_{ox} is the gate oxide thickness, x_j is the source and drain junction depth and t_{dep} is the penetration depth of the gate field in the channel region, which is equal to the depth of the depletion region underneath the gate in a bulk MOSFET. The parameter *EI* is called the “Electrostatic Integrity” factor. It depends on the device geometry and is a measure of the way the electric field lined from the drain influence the channel region, thereby causing SCE and DIBL effects. Based on the above expressions, the threshold voltage of a MOSFET with a given channel length L_{el} can be calculated using the following relationship:

$$V_{TH} = V_{TH\infty} - SCE - DIBL \tag{1.3}$$

where $V_{TH\infty}$ is the threshold voltage of a long-channel device. The decrease of threshold voltage with decreased gate length is a well-known short-channel effect called the “threshold voltage roll-off”.

As can be seen from these expressions, short-channel effects can be minimized by reducing the junction depth and the gate oxide thickness. They can also be minimized by reducing the depletion depth through an increase in doping concentration. For many years, designers have implicitly observed design rules that would ensure the fabrication of devices free of short-channel effects. For example, using $(x_j/L_{el})^2 = 1/3$, $t_{ox}/L_{el} = 1/30$ and $t_{dep}/L_{el} = 1/3$ we obtain a DIBL of 29 mV at V_{DS}=1V. In

modern devices, however, practical limits on the scaling of junction depth and gate oxide thickness lead to a significant increase of short channel effects and excessively large values of DIBL can quickly be reached.

1.3 Gate Geometry and Electrostatic Integrity

Short-channel effects arise when control of the channel region by the gate is affected by electric field lines from source and drain. These field lines is illustrated graphically in Figure 1.2. In a bulk device (Fig. 1.2.A), the electric field lines propagate through the depletion regions associated with the junctions. Their influence on the channel can be reduced by increasing the doping concentration in the channel region. In very small devices, unfortunately, the doping concentration becomes too high (10^{19} cm^{-3}) for proper device operation.

In a fully depleted SOI (FDSOI) device, most of the field lines propagate trough the buried oxide (BOX) before reaching the channel region (Fig. 1.2.B). Short channel effects in FDSOI devices may be better or worse than in bulk MOSFETs, depending on the silicon film thickness, buried oxide thickness, and doping concentrations. Short-channel effects can be reduced in FDSOI MOSFETs by using a thin buried oxide and an underlying ground plane. In that case, most of the electric field lines from the source and drain terminate on the buried ground plane instead of the channel region (Figure 1.2.C). This approach, however, has the inconvenience of increased junction capacitance and body effect. [5]

A much more efficient device configuration is obtained by using the double-gate transistor structure. This device structure was first proposed by Sekigawa and Hayashi in 1984 and was shown to reduce threshold voltage roll-off in short-cannel devices.[6-7] In a double-gate device, both gates are connected together. The electric field lines from source and drain underneath the device terminate on the bottom gate electrode and cannot, therefore, reach the channel region (Fig. 1.2.D). Only the field lines that propagate through the silicon film itself can encroach on the channel region and degrade short-channel characteristics. This encroachment can be reduced by reducing the silicon film thickness.

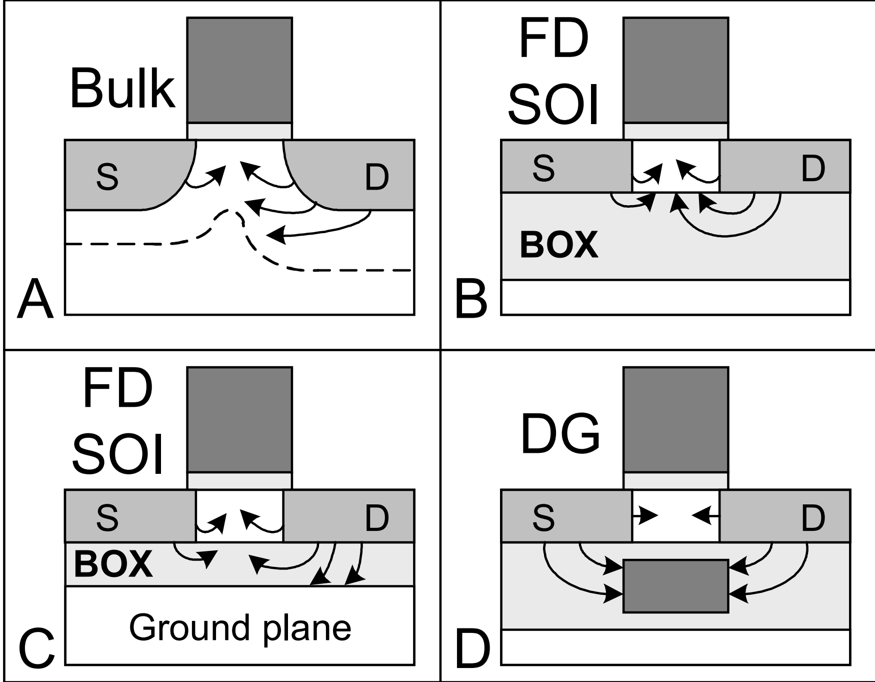

Fig. 1.2. Encroachment of electric field lines from source and drain on the channel region in different types of MOSFETs: A: Bulk MOSFET; B: Fully depleted SOI MOSFET, C: Fully depleted SOI MOSFET with thin buried oxide and ground plane; D: Double-gate MOSFET.

The Voltage-Doping Transformation model can readily be applied to fully depleted SOI and double-gate MOSFETs.[8] Using relationships (a) and (b), the Electrostatic Integrity factor of a *bulk device* can be written:

$$EI = \left[1 + \frac{x_j^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{dep}}{L_{el}} \tag{1.4}$$

The equivalent factor can be obtained for a *fully depleted SOI device* (FDSOI) by noting that the junction depth is equal to the silicon film thickness, t_{Si}, and by noting that the gate field in the channel region penetrates the entirety of the depleted silicon film, t_{Si}, and extends to some depth in the buried oxide, λt_{BOX}:

$$EI = \left[1 + \frac{t_{Si}^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{Si} + \lambda t_{BOX}}{L_{el}} \tag{1.5}$$

In a *double-gate device*, the effective junction depth and the effective gate field penetration for each gate is equal to $t_{Si}/2$, which yields:

$$EI = \frac{1}{2}\left[1 + \frac{t_{Si}^2/4}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{Si}/2}{L_{el}} \tag{1.6}$$

These expressions for the Electrostatic Integrity and the associated device cross sections are summarized in Figure 1.3. It is clear from relationships (1.1) and (1.2) that we want to minimize the *EI* factor in a device in order to keep short-channel effects under control. This can be achieved by reducing the thickness of the device, either by reducing the junction depth, $x_{j,}$ and the depletion depth, $t_{dep,}$ in a bulk device, by reducing the silicon film, t_{si}, and BOX thickness, t_{BOX}, in a fully depleted SOI device, or by reducing the silicon film thickness in a double-gate MOSFET. From an Electrostatic Integrity point of view, the double-gate device has the natural advantage of looking twice as thin the equivalent FDSOI transistor.

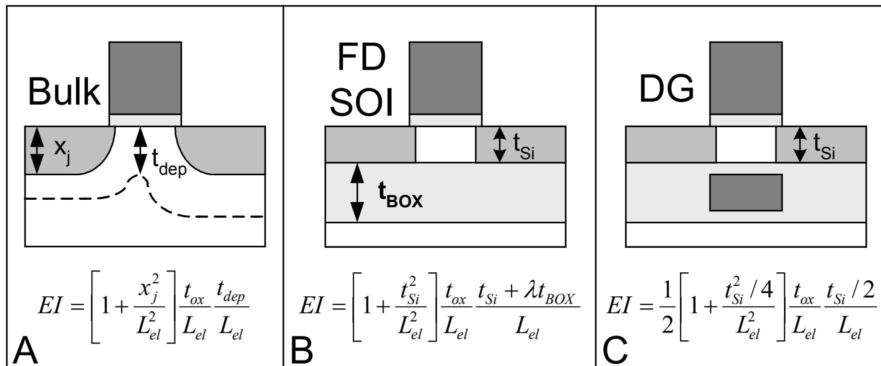

Fig. 1.3. Electrostatic Integrity in A: bulk, B: fully depleted SOI, and C: double-gate MOSFETs.

The VDT model has been implemented in a software package called MASTAR (Model for Analog and digital Simulation of mos TrAnsistoRs [9]). MASTAR has been extensively used in the ITRS 2005 Process Integration, Devices and Structures report to calculate the impact of transistor scaling on electrical characteristics.[10-11] Figure 1.4 shows typical values for DIBL in bulk, FDSOI and double-gate MOSFETs, as a function of gate length. Because thin-film SOI devices deliver better Electrostatic Integrity than bulk MOSFETs, SOI devices can be used at shorter channel lengths while keeping acceptable DIBL values (*e.g.* below

100 mV). The use of double-gate devices allows one to reduce gate length even further.[12-14]

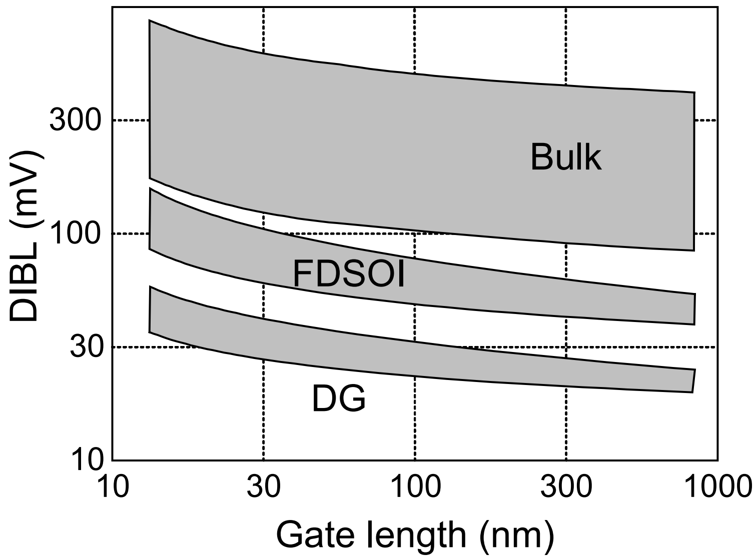

Fig. 1.4. Typical drain-induced barrier lowering in bulk, fully depleted SOI (FDSOI) and double-gate (DG) MOSFETs calculated by MASTAR.

Based on short-channel and DIBL considerations, the minimum gate length that can be used with the different technologies has been calculated with MASTAR and published in the 2005 ITRS. The result of these calculations is shown in Figure 1.5 for three different types of CMOS circuits: high-performance (HP), low operating power (LOP), and low standby power (LSTP) digital circuits. HP circuits are optimized for speed performance and feature the smallest available gate length at any moment in time, while the LSTP devices place the accent on low leakage currents, which necessitates the use of longer-channel devices.

An important conclusion can be derived from the data presented in Figure 1.5: bulk transistors run out of steam once they reach a gate length of 15-20 nm. FDSOI can be used until 10 nm, but smaller gate lengths can be only achieved by the double-gate structure.

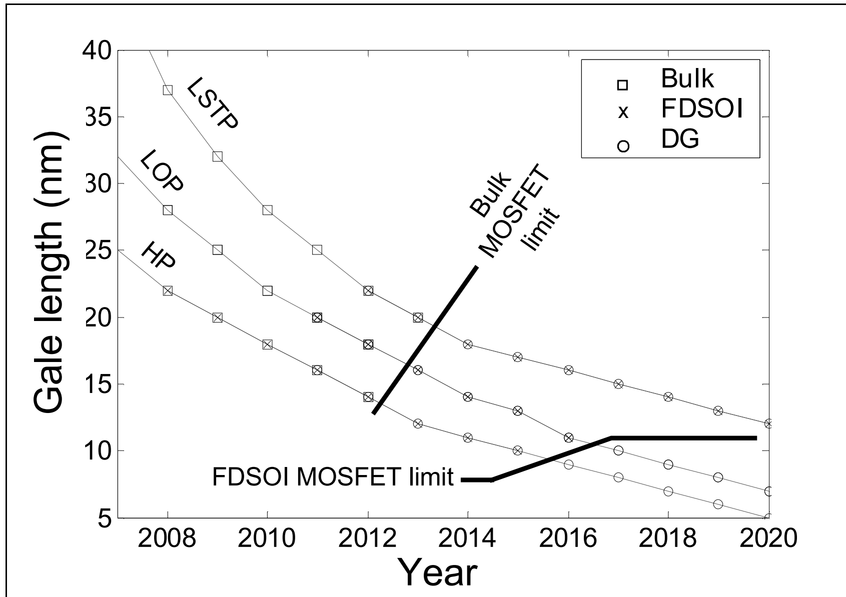

Fig. 1.5. Evolution of gate length predicted by the 2005 ITRS for high-performance (HP), low operating power (LOP), and low standby power (LSTP) digital circuits.

1.4 A Brief History of Multiple-Gate MOSFETs

In a continuous effort to increase current drive and better control short-channel effects, silicon-on-insulator MOS transistors have evolved from classical, planar, single-gate devices into three-dimensional devices with a multi-gate structure (double-, triple- or quadruple- gate devices). It is worth noting that, in most cases, the term "double gate" refers to a single gate electrode that is present on two opposite sides of the device. Similarly, the term "triple gate" is used for a single gate electrode that is folded over three sides of the transistor. One remarkable exception is the MIGFET (Multiple Independent Gate FET) where two separate gate electrodes can be biased with different potentials. It is also worth pointing out that one device may have several different names in the literature (Table 1.1).

Table 1.1. Device names found in the literature.

Acronym	Also known as
MuGFET (Multiple-Gate FET)	Multi-gate FET, Multigate FET
MIGFET (Multiple Independent Gate FET)	Four-terminal (4T) FinFET
Triple-gate FET	Trigate FET
Quadruple-gate FET	Wrapped-Around Gate FET Gate-All-Around FET Surrounding-Gate FET
FinFET	DELTA (fully DEpleted Lean channel TrAnsistor)
FDSOI (Fully Depleted SOI)	Depleted Silicon Substrate
PDSOI (Partially depleted SOI)	Non-Fully Depleted SOI
Volume Inversion	Bulk Inversion
DTMOS (Dual Threshold Voltage MOS)	VTMOS (Varied Threshold MOS) MTCMOS (Multiple Threshold CMOS) VCBM (Voltage-Controlled Bipolar MOS) Hybrid Bipolar-MOS Device

1.4.1 Single-gate SOI MOSFETs

Figure 1.6 shows the “Family Tree” of SOI MOSFETs and shows the evolution from partially depleted, single-gate devices to multi-gate, fully depleted structures. Partially depleted silicon MOSFETs are the successors of earlier SOS (Silicon-On-Sapphire) devices. PDSOI MOSFETs were first used for niche applications such as radiation-hardened or high-temperature electronics. At the turn of the century PDSOI technology became mainstream as major semiconductor manufacturers started to use it to fabricate high-performance microprocessors. The low-voltage performance of PDSOI devices can be enhanced by creating a contact between the gate electrode and the floating body of the device. Such a contact improves the subthreshold slope, body factor and current drive, but limits the device operation to sub-1V supply voltages. [15-23] Fully depleted SOI devices have a better electrostatic coupling between the gate and the channel. This results in a better linearity, subthreshold slope, body coefficient and current drive. FDSOI technology is used in a number of applications ranging from low-voltage, low-power to RF integrated

circuits. There exists a series of textbooks on SOI devices and technology, [24-26] as well as on SOI circuit design.[27-29]

Fig. 1.6. "Family tree" of SOI and multigate MOSFETs.

1.4.2 Double-gate SOI MOSFETs

The first article on the double-gate MOS (DGMOS) transistor was published by T. Sekigawa and Y. Hayashi 1984.[30] That paper shows that one can obtain significant reduction of short-channel effects by sandwiching a fully depleted SOI device between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter Ξ (*Xi*). Using this configuration, a better control of the channel depletion region is obtained than in a "regular" SOI MOSFET, and, in particular, the influence of the drain electric field on the channel is reduced, which reduces short-channel.[31] A more complete modeling that includes Monte-Carlo simulations, was published by Frank, Laux and Fischetti in 1992 in a paper that explores the ultimate scaling of the silicon MOSFET.[32] According to that article, the ultimate silicon device is a double-gate SOI MOSFET with a gate length of 30 nm, an oxide thickness of 3 nm, and a silicon film thickness of 5 to 20 nm. Such a (simulated) device shows no short-channel effects for gate lengths larger than 70 nm, and provides transconductance values up to 2300 mS/mm. The first fabricated double-gate SOI MOSFET was the "fully DEpleted Lean-channel TrAnsistor (DELTA, 1989)",[33] where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin" (Figure 1.7). The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin. [34-38] The hard mask is used to prevent the formation of parasitic inversion channels at the top corners of the device.

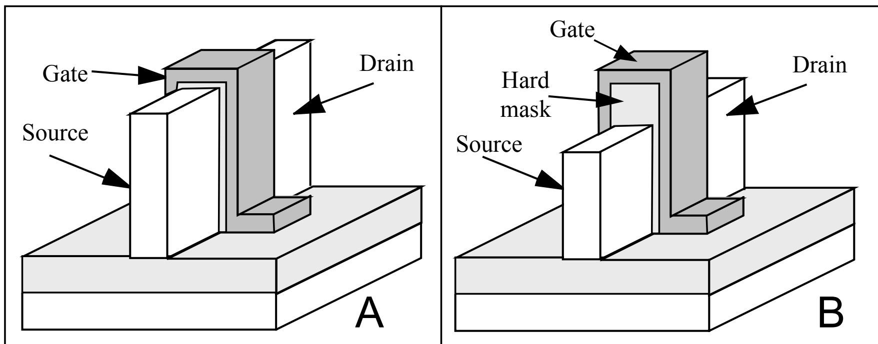

Fig. 1.7. Examples of double-gate MOS structure: A: DELTA MOSFET; B: FinFET.

Other implementations of vertical-channel, double-gate SOI MOSFETs include the "Gate-All-Around device" (GAA), which is a planar MOSFET with the gate electrode wrapped around the channel region (Figure

1.8.A)[39], the Silicon-On-Nothing (SON) MOSFET,[40-42] the Multi-Fin XMOS (MFXMOS) [43], the triangular-wire SOI MOSFET [44] and the Δ-channel SOI MOSFET.[45] It is worth noting that the original GAA device was a double-gate device, even though the gate was wrapped around all sides of the channel region, because the silicon island was much wider than thick. Nowadays, most people use the GAA acronym for quadruple-gate or surrounding-gate devices having a width-to-height ratio much closer to unity.[46-48]

The MIGFET (Multiple Independent Gate FET) is a double-gate device in which the two gate electrodes are not connected together and can, therefore, be biased with different potentials.[49-52,160] The main feature of the MIGFET is that the threshold voltage of one of the gates can be modulated by the bias applied to the other gate. This effect is similar to the body effect in FDSOI MOSFETs.[53] An application using MIGFET is signal modulation. A simple square law mixer can be formed using a single MIGFET by applying a small RF signal to one gate and a large low-frequency signal to the other gate. This single-device modulation is possible because the channel is fully depleted and the gates are perfectly symmetrical and aligned. This signal modulation circuit reduces transistor counts and rail-to-rail transistor stack, making it possible to design compact low-power mixers.[54]

1.4.3 Triple-gate SOI MOSFETs

The triple-gate MOSFET is a thin-film, narrow silicon island with a gate on three of its sides.[55] Implementations include the quantum-wire SOI MOSFET (Figure 1.8.B) [56-57] and the trigate MOSFET.[58-59]

The Electrostatic Integrity of triple-gate MOSFETs can be improved by extending the sidewall portions of the gate electrode to some depth in the buried oxide and underneath the channel region (Π-gate device [60-61] and Ω-gate device [62-64]). From an electrostatic point of view, the Π-gate and Ω-gate MOSFETs have an effective number of gates between three and four. The use of strained silicon, a metal gate and/or high-k dielectric as gate insulator can further enhance the current drive of the device.[65-68]

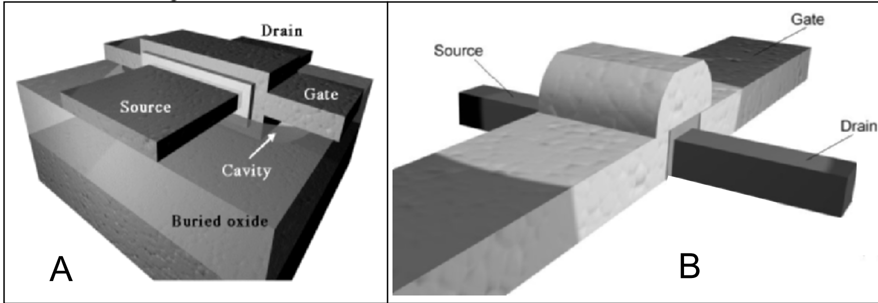

Fig. 1.8. A: Gate-All-Around (GAA) MOSFET; B: Triple-gate MOSFET.

1.4.4 Surrounding-gate (quadruple-gate) SOI MOSFETs

The structure that theoretically offers the best possible control of the channel region by the gate, and hence the best possible Electrostatic Integrity is the surrounding-gate MOSFET. The first surrounding-gate MOSFETs were fabricated by wrapping a gate electrode around a vertical silicon pillar. Such devices include the CYNTHIA device (circular-section device) [69-70] and the pillar surrounding-gate MOSFET (square-section device).[71] More recently, planar surrounding-gate devices with square or circular cross sections have reported.[72-73] Surrounding-gate SOI MOSFETs with a gate length as small as 5 nm and a diameter of 3 nm have shown to be fully functional.[74-75]

To increase the current drive per unit area, multiple surrounding-gate channels can be stacked on top of one another, while sharing common gate, source and drain. Such devices are called the Multi-Bridge Channel MOSFET (MBCFET), [76-77] the Twin-Silicon-Nanowire MOSFET (TSNWFET) [78], or the Nano-Beam Stacked Channels (GAA) MOSFET.[79] Analytical models for the electrical characteristics of cylindrical surrounding-gate MOSFETs can be found in the literature.[80-83]

Schematic cross sections corresponding to the different gate structures described in the previous sections are shown in Figure 1.9.

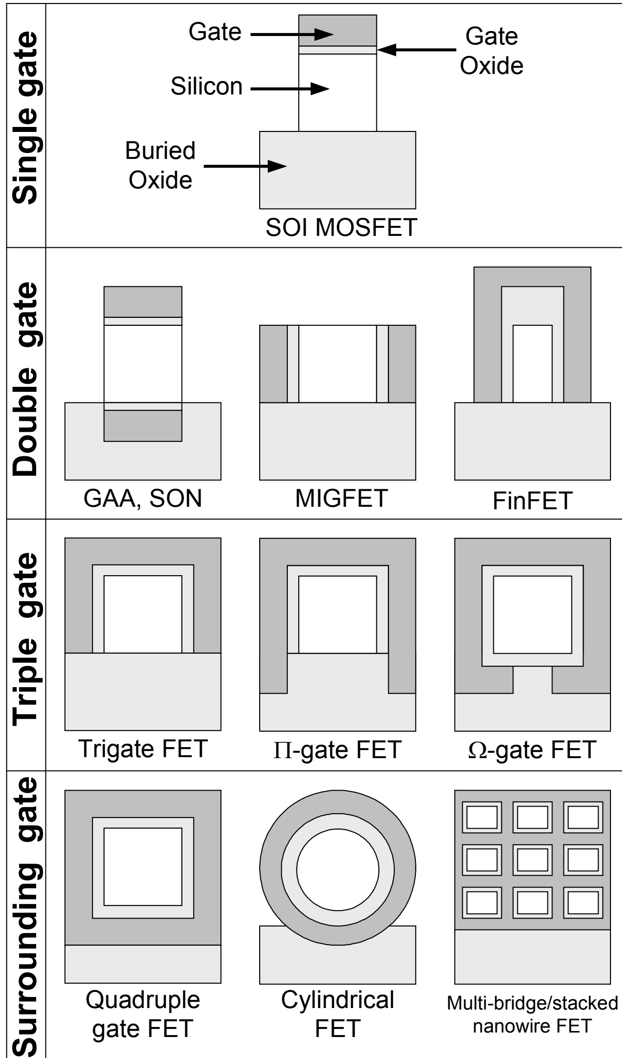

Fig. 1.9. Different gate structures.

1.4.5 Other multigate MOSFET structures

The Inverted T-channel FET (ITFET) combines a thin-film planar SOI device with a trigate transistor (Figure 1.10.A). [84-85] It comprises planar horizontal channels and vertical channels in a single device. The devices have multi-gate control around these channels. The Inverted T-gate

structure has several advantages: the large base helps the fins from falling over during processing; it also allows for transistor action in the space between the fins, which is left unused in other MuGFET configurations. These additional channels increase the current drive. Numerical simulation of an N-channel ITFET reveals different turn-on mechanisms in different parts of the device. The corners of the device turn on first**,** immediately followed by the surface of the planar regions and the vertical channel. Since each ITFET has about seven corner elements they constitute a significant current to each ITFET device and in a well-designed device can yield substantially more current than a planar device of equivalent area.

The bulk FinFET is a FinFET made on bulk silicon instead of an SOI wafer. Fins are etched on a bulk silicon wafer and trimmed using an oxidation step. Field oxide is deposited to avoid inversion between the fins (Figure 1.10.B). Device with fin width down to 10 nm have shown to have good punchthrough immunity down to the sub-20nm gate length regime.[86-87]

The multi-channel Field Effect Transistor (McFET) is a modified bulk FinFET where a trench is etched in the center of the fin.[88] The trench is filled by the growth of a gate oxide and the deposition of gate material. This process produces a device having two very thin “twin” fins running from source to drain (Figure 1.10.C).

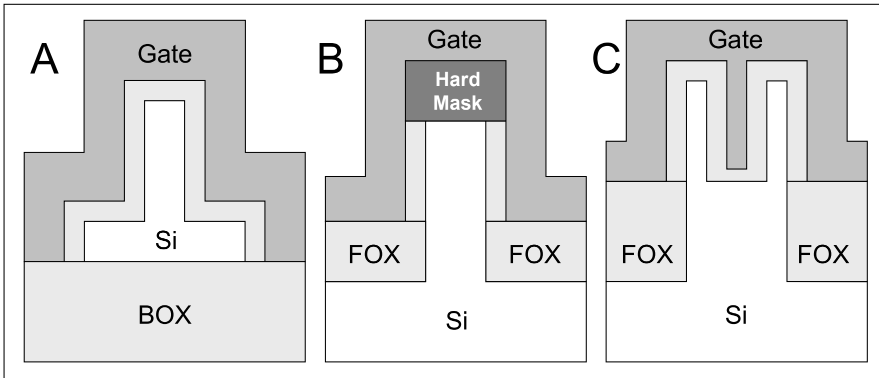

Fig. 1.10. Cross section of A: Inverted T channel FET; B: Bulk FinFET; C: Multi-channel Field Effect Transistor.

The 4-gate transistor (G^4 FET) has two (top and bottom) MOS gates and two (lateral) JFET gates. It is operated in accumulation mode and has the same structure as an inversion-mode partially depleted SOI MOSFET with

two independent body contacts. These lateral contacts play the role of source and drain in the G^4 FET, while the junctions are used as lateral gates. The current in the body of the device is controlled by the front and back MOS gates, and by the two lateral junctions. The height and width of the conductive path is modulated by a mix of MOS and JFET effects. Each gate has the ability of switching the transistor on and off.[89-91] A model for the G^4 FET has been published In the literature.[92]

1.4.6 Multigate MOSFET memory devices

SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) devices are non-volatile flash memory devices. They are essentially used in mobile applications. Flash devices have a small form factor, high storage density and low power consumption. For logic applications FinFET type devices are known to have good scalability down to 10-nm gate length. The FinFET device architecture combined with an ONO trapping layer as gate dielectric enables memory cells with feature sizes well below 50-nm. SONOS FinFET cells are programmed and erased using Fowler–Nordheim tunneling. SONOS FinFET memory devices show excellent functionality down to 20 nm channel length. [93-94] As an alternative to the ONO layer, nanocrystals embedded within the gate dielectric can be used to trap charges and achieve a similar memory effect. FinFET flash memory devices with a V_{TH} window larger than 1 volt have been demonstrated using silicon nanocrystals embedded in the gate oxide.[95]

The SOI Zero-capacitor RAM (ZRAM) memory cell consists of a single PDSOI transistor in the floating body of which a charge can be stored. Such a capacitorless, one-transistor memory cell is, of course much smaller than a classical DRAM cell that requires the use of both a transistor and a storage capacitor. In the ZRAM memory cell a “1” binary state is stored by biasing the transistor in saturation and injecting holes in the floating body. Applying a negative bias to the bit line (device source) removes the charge from the floating body and, therefore, stores a binary “0” in the device. Since the threshold voltage of the FET varies with the charge stored in the body the logic state can easily be read by measuring the drain current when the device is turned on. Even though the storage of a charge requires a floating body, and, therefore, a partially depleted device, it is possible to realize ZRAM cells in fully depleted FinFETs of trigate devices. By applying a back-gate bias to the device, a floating body can be created at the bottom of the otherwise fully depleted fin and ZRAM operation can be activated.[96] Retention times of few tens of milliseconds are observed at room temperature on FinFETs with 300 nm channel length.

These values suit well typical embedded DRAM specification. FinFETs provide better retention characteristics than trigate devices which have a retention time of approximately 2 ms. Retention time decreases at shorter channel length but even 100 nm devices still show retention time of few milliseconds.[97]

When a positive bias is applied to the underlying silicon substrate (back gate) and a negative bias is applied to the gate of a MuGFET, it is possible to create an inversion layer at the bottom of the device and accumulation at the other interfaces. In that case, the so-called "MetaStable Dip" (MSD) effect can be observed, in which the transconductance as a function of the gate voltage increases, then drops, and then increases again. This effect is time-dependent and presents an hysteresis effect which depends whether the gate voltage is scanned in the forward or reverse mode.[98] The hysteretic nature of the phenomenon makes it useful for potential single-transistor memory applications.[99]

1.5 Multigate MOSFET Physics

1.5.1 Classical physics

1.5.1.1 Natural length and short-channel effects

The Electrostatic Integrity (*EI*), which we know to be related to short channel effects, was compared between a bulk transistor, a FDSOI MOSFET, and a double-gate device in Figure 1.3. It was shown that the *EI* can be improved by reducing the gate oxide thickness and/or by decreasing the silicon film thickness (the junction depth in the case of a bulk device). We are now going to extend the analysis to all types of multigate MOSFETs.

The potential distribution in the channel of a fully depleted multigate MOSFET can be obtained by solving Poisson's equation using the depletion approximation:

$$\frac{d^2\Phi(x,y,z)}{dx^2}+\frac{d^2\Phi(x,y,z)}{dy^2}+\frac{d^2\Phi(x,y,z)}{dz^2}=\frac{qN_a}{\varepsilon_{si}} \tag{1.7}$$

Let us first understand the meaning of this equation. It can be rewritten in the form: