More than Moore

G.Q. Zhang • A.J. van Roosmalen

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Creating High Value Micro/Nanoelectronics Systems

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Editors
Guo Qi Zhang
Delft University of Technology
NXP Semiconductors
Delft, Eindhoven
The Netherlands

Alfred J. van Roosmalen
Delft University of Technology
NXP Semiconductors
Delft, Eindhoven
The Netherlands

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Preface

Since the first transistor was invented at Bell Laboratories in 1947, semiconductors rapidly evolved into a key enabler for providing solutions to societal, business, and consumer needs. Today, the semiconductor market has become the cornerstone of global high-tech economy, with more than 16% of the world economy built on semiconductors and with annual R&D budgets in the industry ranging up to 20% of revenue. At the same time, semiconductors have become the cornerstone of modern society, and pervaded and penetrated in numerous aspects of human lives.

Explosive technology development driven by Moore's law has been playing a vital role for the success of the semiconductor industry. In 2005, the strategic research agenda and vision for "More than Moore" (MtM) technology were formulated in a systematic manner by the European Technology Platform for Nanoelectronics ENIAC. Since then, we have witnessed the quick development of a new area of micro/nanoelectronics beyond the boundaries of Moore's law and into the area of "MtM," which creates and adds more nondigital functionality to conventional semiconductor technology, leading to virtually unlimited technology possibilities and application potentials for the semiconductor-based high-tech industry.

Based on the extensive results from the "MtM" technology domain team within ENIAC and the MEDEA+ working group ("Towards and beyond 2015"), this unique book presents the new semiconductor landscape by highlighting current and future semiconductor applications to meet various society needs, providing a systematic overview for the state-of-the-art of semiconductor technologies, especially the "MtM" technology, and summarizing the fast evolving business trends.

The semiconductor technology and business environment are very different today from what they were when G.E. Moore postulated the theorem now known as Moore's law, more than 40 years ago. We hope that this book can provide inspiration for the direction and future development of semiconductors in the decades to come.

It is our privilege, as the chair of ENIAC "MtM" technology domain team and the chair of ENIAC/AENEAS support group, to present this book. From this place, we like to thank all authors who have worked on the various chapters and also all technology domain team members in the ENIAC, EPoSS, and MEDEA+/CATRENE communities who have contributed to this book in one way or another.

Eindhoven, The Netherlands G.Q. Zhang and A.J. van Roosmalen

Contents

Contributors

Rolf Aschenbrenner Fraunhofer IZM, Berlin, Germany

Mario Baum Fraunhofer ENAS, Group Technologies/Waferbonding, Chemnitz, Germany

E. Beyne IMEC, Leuven, Belgium

Joel Björk Technikon Forschungs - und Planungsgesellschaft mbH, Villach, Austria

N. Blanc CSEM SA, Photonics Division, Zurich, Switzerland

P. Buchschacher Faculty of Electrical Engineering and Information Technology STU, Bratislava, Slovakia

Peter Caldera Infineon Technologies, Austria AG, Villach, Austria

G. Carchon IMEC, Leuven, Belgium

Mario Cortese STMicroelectronics S.r.l., Milan, Italy

W. De Raedt IMEC, Leuven, Belgium

Michel Despont IBM Zurich Research Laboratory, Rüschlikon, Switzerland

Daniel Donoval Faculty of Electrical Engineering and Information Technology STU, Bratislava, Slovakia

Karsten Einwich Fraunhofer Institute for Integrated Circuits, Dresden, Germany

Paul Fugger Infineon Technologies, Austria AG, Villach, Austria

Thomas Gessner Fraunhofer ENAS, Chemnitz, Germany

Wolfgang Gessner VDI/VDE Innovation + Technik, Berlin, Germany

P. Giffard CEA-LETI-Minatec, Grenoble, France

Christoph Hagleitner IBM Zurich Research Laboratory, Rüschlikon, Switzerland

M. Hoheisel Siemens AG, Forchheim, Germany

Karl Hollaus Institute for Fundamentals and Theory in Electrical Engineering, Graz University of Technology, Graz, Austria

Jaroslav Kováč Faculty of Electrical Engineering and Information Technology STU, Bratislava, Slovakia
International Laser Center, Ilkovičova 3, 81219, Bratislava, Slovakia

Jaroslav Kováč, Jr. Faculty of Electrical Engineering and Information Technology STU, Bratislava, Slovakia
International Laser Center, Bratislava, Slovakia

Mark Lantz IBM Zurich Research Laboratory, Rüschlikon, Switzerland

Günter Lugert Sensor & Actuator Systems, Siemens AG, Munich, Germany

G. Maggioni STMicroelectronics S.r.l., Milan, Italy

V. Nguyen CEA-LETI-Minatec, Grenoble, France

Harald Pötter Fraunhofer IZM, Berlin, Germany

Wolfgan Pribyl Institute for Electronics, Graz University of Technology, Graz, Austria

P. Puget CEA-LETI-Minatec, Grenoble, France

Herbert Reichl Technische Universität, Berlin, Germany

Jochen Reisinger Infineon Technologies, Austria AG, Villach, Austria

G. Ricotti STMicroelectronics S.r.l., Milan, Italy

Willy Sansen Department of Electrical Engineering, Katholieke Universiteit Leuven, Leuven, Belgium

P. Seitz CSEM SA, Research Center for Nanomedicine, Landquart, Switzerland

H.A.C. Tilmans IMEC, Leuven, Belgium

Michael Topper Fraunhofer IZM, Berlin, Germany

František Uherek Faculty of Electrical Engineering and Information Technology STU, Bratislava, Slovakia
International Laser Center, Bratislava, Slovakia

A.J. van Roosmalen Delft University of Technology, NXP Semiconductors, Delft, Eindhoven, The Netherlands

C. Vauchier CEA-LETI-Minatec, Grenoble, France

Peter Vettiger IBM Zurich Research Laboratory, Rüschlikon, Switzerland

Benedetto Vigna STMicroelectronics S.r.l., Milan, Italy

Andreas Wiesbauer Infineon Technologies, Austria AG, Villach, Austria

G.Q. Zhang Delft University of Technology, NXP Semiconductors, Delft, Eindhoven, The Netherlands

Horst Zimmerman Institute of Electrical Measurements and Circuit Design, Vienna University of Technology, Vienna, Austria

Chapter 1
The Changing Landscape of Micro/Nanoelectronics

G.Q. Zhang and A.J. van Roosmalen

Abstract In the past decades, the progresses of semiconductors are mainly powered by Moore's law focusing on IC miniaturization down to nanoscale, resulting in the transition from microelectronics into nanoelectronics. Recently, we have witnessed the quick development of a new area of Micro/nanoelectronics beyond the boundaries of Moore's law, called "More than Moore" (MtM). MtM creates and adds various nondigital functionalities to semiconductor products and focuses on creating high value micro/nanoelectronics systems, leading to virtually unlimited technology possibilities and application potentials. This chapter presents the changing global landscape of micro/nanoelectronics by summarizing the major ongoing technology and business development trends, especially the vision and strategy of MtM, by highlighting some potential applications, and by providing a systematic overview for the major MtM technologies.

Keywords Moore's s law • More than Moore • Beyond CMOS • Heterogeneous integration

1.1 Introduction

The first transistor was invented at Bell Laboratories on December 16, 1947, by William Shockley, John Bardeen, and Walter Brattain. This was perhaps the most important electronics event of the twentieth century, as it later made possible the integrated circuit and microprocessor that are the basis of modern electronics. Since then, semiconductors rapidly evolved into a key enabler for providing solutions to societal, business, and consumer needs for more than half century.

G.Q. Zhang (✉) and A.J. van Roosmalen
Delft University of Technology,
NXP Semiconductors, Delft, Eindhoven, The Netherlands

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As of today, the semiconductor market has become the cornerstone of global high-tech economy. The worldwide market for electronic products in 2007 is estimated at $1,105 billion, and the related electronics services market at around $6,500 billion [1]. These product and service markets are enabled by a $280 billion market for semiconductor components and an associated $80 billion market for semiconductor equipment and materials. By comparison, the 2007 GWP (Gross World Product) is expected to reach $48,900 billion, implying that more than 16% of the world economy today is built on semiconductors (Fig. 1.1). In addition to its immediate economic value, the semiconductor industry is one of the biggest investors in R&D for the knowledge society, with typical annual R&D budgets in the industry ranging from 15 to 20% of revenue.

At the same time, semiconductors have become the cornerstone of modern society, and pervaded human lives in the past 50 years. Without them, the rich multimedia experience that we enjoy in today's world of CD, MP3, DVD, and the Internet would not have been possible. Without them, we would not be able to talk to people around the world, exchange messages, or share photographs and video clips via a personal portable device that fits into our pocket. Without them, our cars would do far fewer kilometers per liter of fuel, heavily pollute the environment, and cause more accidents. Gordon Moore estimated in 2003 that the number of transistors shipped in a year had reached about 10^{18}. That is about 100 times the number of ants estimated to be in the world. Semiconductors are with us everywhere and anytime.

The shift from the past era of microelectronics, where semiconductor devices were measured in microns (1 millionth of a meter) to the new era of nanoelectronics where they shrink to dimensions measured in nanometers (1 billionth of a meter) will make the semiconductor industry even more pervasive than it is today. It will allow much more intelligence and far greater interactivity to be built into many more everyday items around us, with the result that silicon chip technology will play a part in virtually every aspect of our lives, from personal health and traffic control to public security.

However, in the future, the semiconductor industry cannot be exclusively based on the same "business as usual" strategy. This is due to the facts that many aspects of the business, technology, design, and system level requirements are now

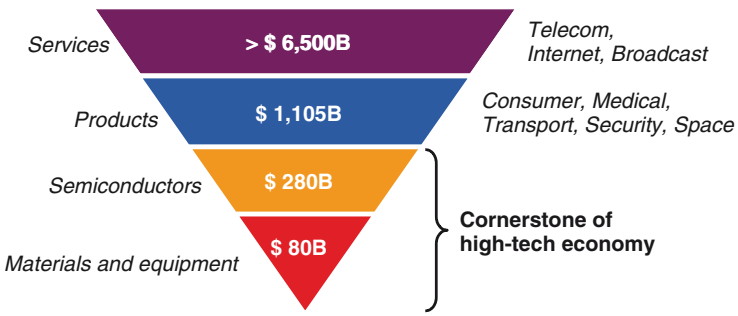

Fig. 1.1 Semiconductors underpin over 16% of the global economy

simultaneously changing when approaching fundamental limits at the nanoscale. The introduction of new materials and technology steps, increased process variability, tough reliability need, are all impacting system level design at the same time, confronted with extremely large and complex architectures and quasi-impossible-to-solve power density issues. On the other hand, the applications will also be different. Consumers and society at large demand new types of electronics products with more than digital function, short-time-to-market for new product creation, and continuous cost reduction. This chapter intends to draw an overview picture of the changing global landscape of semiconductors by highlighting some of the major development trends, covering both technology and business.

1.2 Technology Evolution

Since the invention of transistor in 1947, semiconductors have been undergoing many rapid changes empowered by numerous innovations and technology breakthroughs. In the following some of the major technology advances, both existing and emerging, will be discussed.

1.2.1 More Moore (MM)

On April 19, 1965, the Electronics Magazine published a paper by Gordon E. Moore in which he made a prediction that the number of transistors on a chip roughly doubles every 2 years. Known as Moore's law, his prediction has enabled widespread proliferation of technology worldwide, and today has become shorthand for rapid technological change.

Moore's law is about miniaturization, and about extreme miniaturization. As one example, the Intel® 45-nm high-*k* metal gate silicon technology packs more than 400 million transistors for dual-core processors and more than 800 million for quad-core. Intel demonstrated first 32-nm logic process with functional SRAM packing more than 1.9 billion transistors [2]. The total length of the interconnect lines connecting different transistors of a single IC can be as long as several kilometers.

Moore's law is about cost reduction, and about extreme cost reduction. The price per transistor on a chip has dropped dramatically since 1968 [3, 4]. Some people estimate that the price of a transistor is now about the same as that of one printed newspaper character. In 1978, a commercial flight between New York and Paris cost around $900 and took 7 hours. If the principles of Moore's law had been applied to the airline industry the way they have applied to the semiconductor industry since 1978, then that flight would now cost about a cent and take less than 1 s. It is this economic aspect of Moore's law that has made electronics so pervasive.

Moore's law characterized by extreme miniaturization and extreme cost reduction is not only valid for ICs; for backend technology, i.e., packaging and assembly, similar trends have also been observed. Taking some feature sizes of packaging and assembly as examples, one can see that wire diameters for bonding can be smaller than 10 μm; the interconnect pitch of wafer level packaging can be smaller than 20 μm; the thickness of copper film/trace in PCB can be smaller than 5 μm; the microvia diameters can be smaller than 20 μm; and the wafer thickness can be thinner than 20 μm. Clearly, Moore's law has not only driven the extreme miniaturization of the IC technology, but also pushed the packaging, assembly, and system level miniaturization, going beyond the visualization with our bare eyes.

Currently almost 70% of the total semiconductor components market is directly impacted by advanced CMOS miniaturization achieved by following Moore's law. This 70% comprises three component groups of similar size, namely microprocessors, mass memories, and digital logic. The analog/mixed-signal market largely relies on variants of CMOS technology that are less affected by the miniaturization race due to other constraints, such as the need to handle power and/or high voltage.

The "MM" development is defined as a relentless scaling of digital functions, and an attempt to further develop advanced CMOS technologies and reduce the associated cost per function along two axes. The first axis is a geometrical (constant field) scaling, which refers to the continued shrinking of horizontal and vertical physical feature sizes of on-chip logic and memory storage functions in order to improve integration density (reduced cost per function), performance (higher speed, lower power), and reliability values. The second axis of scaling relates to three-dimensional device structure improvements plus other nongeometrical process techniques and new materials that affect the electrical performance of the chip. This axis of "equivalent" scaling occurs in conjunction with, and also enables, continued geometrical scaling.

However, reaching this ultimate CMOS node at the deca-nanometer level around 2015 will not be business as usual [5]. It will require much more innovation in the coming decade than in the past ones. Indeed, today we have reached the end of classical Dennard scaling and we are confronted with a set of cumulative interrelated challenges at all levels of the value chain from system down to atomic level, requiring enormously innovative processing steps and new materials in contrast with the Dennard scaling of the past. The art will be to manage these processes such that 10 billion of these devices can be interconnected to create reliable architectures for applications. To summarize, the main challenges for "MM" technology are as follows [5]:

- In the process technology domain: massive introduction of new materials, introduction of new device architectures (FD mugfets), moving to EUV litho or nanoimprint litho, the increase of random device and interconnect variability especially in memories, reaching the limit of Cu interconnects (e-migration, cross-talk, etc.), and conflicting between dynamic and static power density.

- In the design domain: Ultimately, NRE cost may reach 1 billion € per platform if no drastic changes in design technology occur due to increased hardware-software interaction on multicore platforms. Furthermore, the design metrics have changed from maximizing raw performance (servers, microprocessors) to maximizing throughput (B/s)/W cm^2.
- The problem of ultimate scaling is shifting to both extremes of the value chain, i.e., coping with gigascale system-level design cost (hardware and software) on one hand and multiscale (from nano to macro) physical effects on the other hand. Most importantly, the challenges in the above-mentioned two domains are strongly inter-related, i.e., changing in process will affect the whole design process, from atomic to system level. To name a few they are as follows [5].
- Achieving the above power efficiency requires a joint optimization of concurrent hardware-dependent low-power software; heterogeneous multicore architectures; and sub-1 Volt digital, RF, and analog IP libraries using novel device architectures.
- Reaching lithographic limits will require the development of highly regular yet layout-efficient computing, storage, and communication structures amenable to automated design methodologies. Otherwise, IP development costs will become unacceptable.
- Random variability will affect parametric yield and will require, besides DFM techniques, novel ways to avoid corner-based design to cope with device uncertainty, and amenable to design automation. Designers need to be trained in their applications. This will require the development of self-healing, defect, and error-tolerant, yet testable design styles based on low-cost on-chip adaptive control systems.
- Reliable local and global on-chip communication in 22 nm and beyond technology will be a much more limiting factor than transistor scaling and will require, besides the investigation of optical-, wireless-, or CNT-based technologies, investigation of architectural solutions such as tile-based GALS architectures exploiting networks-on-chip. Three-dimensional integration and System-in-Package (SiP) should be studied as strong contenders to ultimate scaling for true system design, which is the ultimate goal of electronics.
- Analog and RF design will have to cope with ultimate digital scaling and further sub-1 Volt scaling. This will require extreme creativity in analog and RF system design by compensating analog deficiencies using digital techniques.

It is important to note that the "living apart together" relationship among system, platform, IP creators, and process development is no longer possible or appropriate. Currently only limited research activities are devoted to the link between the two extremes (gigascale system design and multiscale physical performance), without which the commercial exploitation of ultimate CMOS will fail. There is an urgent need for an interdisciplinary dialog and interdisciplinary teams of industry, research institutes, and academia to establish a common systemability view, roadmap, and joint effort, in order to cope with the hardware and software codesign gap (see Fig. 1.2).

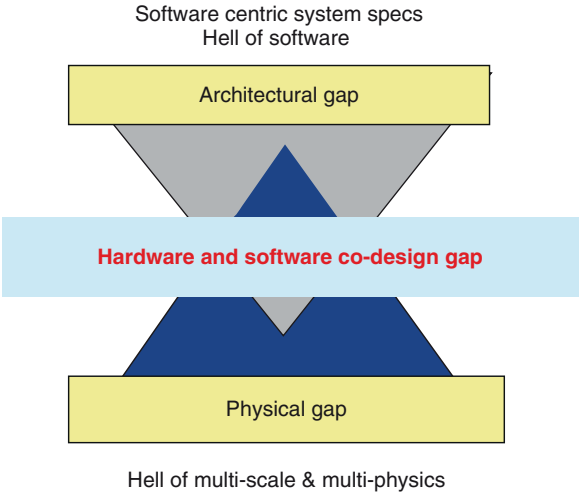

Fig. 1.2 Hardware and software codesign gap

1.2.2 More than Moore (MtM)

In recent years, we have witnessed the emergence of an increasingly diverse area of micro/nanoelectronics that goes beyond the boundaries of Moore's law into the area of "More than Moore" (MtM) [1, 6–10]. From the technology perspective, "MtM" refers to all technologies enabling nondigital functions. They are based on or derived from silicon technology, but do not simply scale with Moore's law. From the application perspective, "MtM" enables functions equivalent with the eyes, ears, noses, arms, and legs of human beings, working together with the brain provided by microprocessor and memory subsystems. Figure 1.3 shows some typical "MtM" products, such as a mobile phone with nondigital functions (such as audio/video player, camera, Personal Health Monitor, GPS, Identification, Compass, etc.) and a great variety and quantity of sensors and actuators required in today's cars to monitor and control engine functions, safety, navigation, and comfort support. There are many other "MtM" products being able to realize a wide range of nonelectronic functions, such as mechanical, thermal, acoustical, chemical, optical, and biomedical. These nondigital functions provide means to sense, to interact with people, to interact with environment, and to power advanced semiconductor systems (see Fig. 1.4).

Generally speaking, "MtM" adds value to conventional semiconductors products via three routes [5]:

- *Interfacing (sensing and interacting) to the real world*. If the interaction is based on a nonelectrical phenomenon, then specific transducers are required. Sensors, actuators, displays, imagers, fluidic or biointerfaces (DNA, protein, lab-on-chip, neuron interfaces, etc.) are in this category.

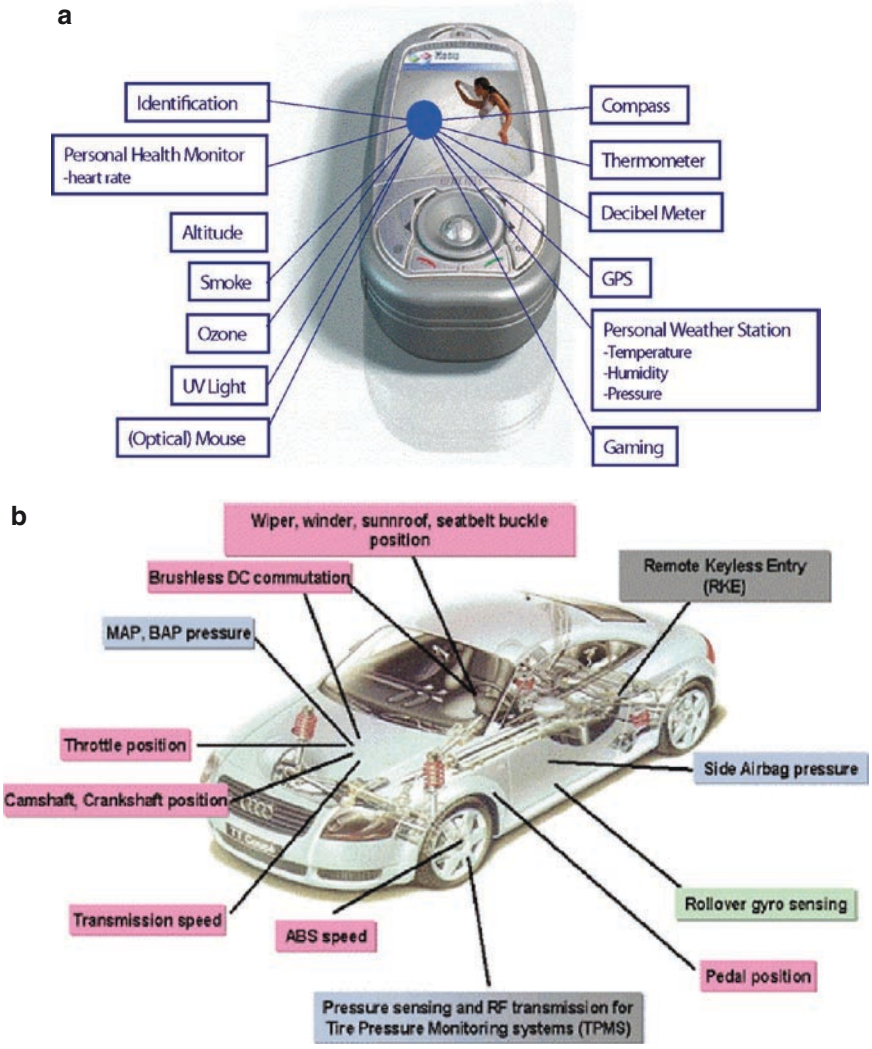

Fig. 1.3 Some "MtM" product examples

- *Enhancing* electronics *with nonpure electrical devices*. New devices can be used in RF or analog circuits and signal processing. Thanks to electrical characteristics or transfer functions that are unachievable by regular CMOS circuits, it is possible to reach better system performances. RF MEMS electroacoustic high Q resonators are a good example of this category.
- *Embedding power sources with the electronics*. Several new applications will require on-chip or in-package micro power sources (autonomous sensors or circuits with permanent active security monitoring for instance). Energy scavenging microsources and microbatteries are examples of this category.

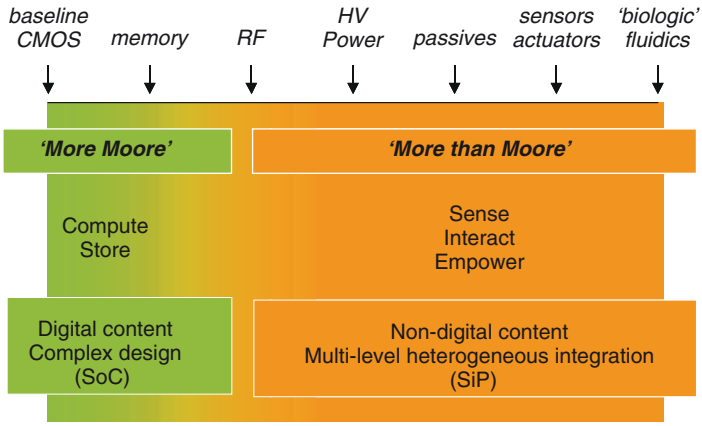

Fig. 1.4 Functions of "MtM" products

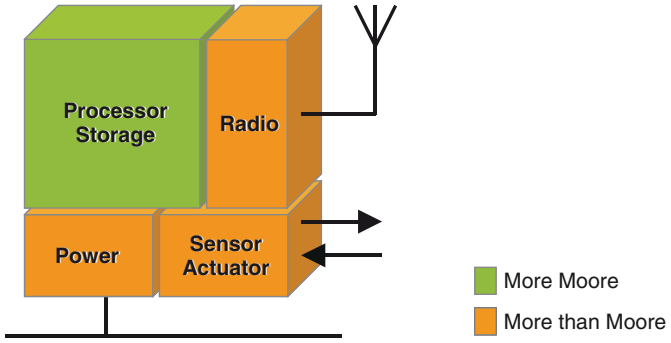

Fig. 1.5 Intelligent systems need "MM" and "MtM"

Clearly "MtM" technologies and products provide essential functional enrichment to the digital CMOS-based mainstream semiconductors. Along with IC technology, "MtM" becomes one of the key innovation drivers to meet current and future society needs with unlimited application potentials.

The emerging and rapid developments of "MtM" technologies and products are mainly driven by three factors given as follows [6].

First, the increasing social need for high-level system integration including non-digital functionalities, in order to interface to the real world in a wide range of societal relevant applications. The real world and the consumers are all analog, and digital functions alone are far from sufficient to meet the needs of human being. With industry entering into the nanoelectronics era, more and more consumers desire more functionalities beside the digital one. Figure 1.5 shows that intelligent system needs not only memory and processor, but also power, RF interfaces, and sensor and actuator functions.

Second, the need to create innovative products and broaden the product portfolio using less advanced wafer technology and production lines. Due to fierce competition and high investment costs of wafer fab, it is difficult to ensure business profitability by producing commodity ICs using less advanced wafer fab. However, for many applications, "MtM" products which are less geometric size dominant and allow a time-delay for miniaturization can still add value on top of the less advanced IC technology (see Fig. 1.6). It is worth to emphasize that although many novel "MtM" technologies and applications may not be size dependent as "MM," novel nanotechnologies will for sure provide important opportunities for the future development and success of "MtM" technologies. Besides, "MtM" technology will not only help to enlarge existing markets, but also drive the development of emerging ones – for example, Ambient Intelligence, Domotica, Lifestyle, Heath Care, Security, Food, Environment, and Energy. "MtM" is a unique opportunity for creativity, innovation, and new business creation for both small and large companies.

Finally, the need to overcome the cost and time-to-market limitations of System-on-Chip (SoC) development. Although many nondigital functions can theoretically be integrated onto these chips, doing so would involve prohibitive development time and cost. In addition, there is little prospect of a single practical IC technology that would allow integration with large number of diverse applications in the near future. It is therefore of paramount importance to balance the benefits of integrating some "MtM" functions on a chip, while integrating other functions in the same package to create SiP solutions.

It should be emphasized that "MM" and "MtM" are not competing with each others, but rather complimentary. To drive the future success of semiconductors, it is essential to integrate "MM" technology focusing mainly on digital functions with "MtM" technology focusing mainly on nondigital functions via heterogeneous system integration (see Fig. 1.7).

The technology challenges for "MtM" are application and product specific. Each type of technology, such as RF, sensors/actuators, biofluidics, HV and power,

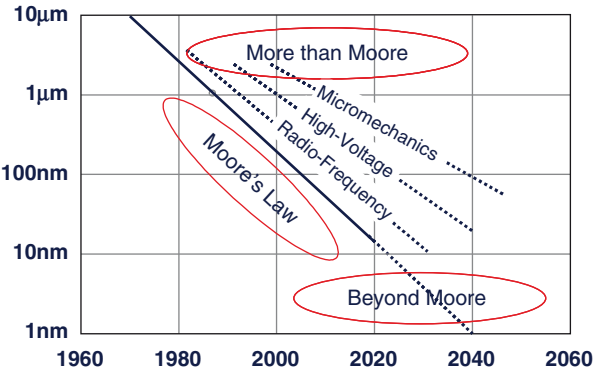

Fig. 1.6 Dimension delay of "MtM" products

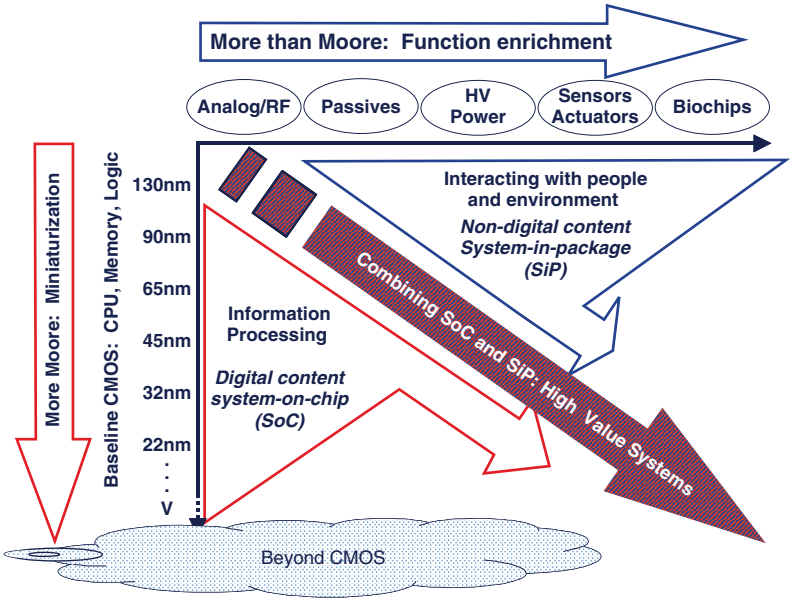

Fig. 1.7 ITRS nanoelectronics technology roadmap

Solid-State Lighting, MEMS/NEMS, has their own issues. Examples of some generic challenges are given below [11]:

- The introduction of new nanomaterials and nanotechnologies: To some extend, the success of nanoelectronics depends on the profound understanding of the properties and behavior of materials and their interfaces under manufacturing, qualification testing, and use conditions; and the capability to tailor the material design for the requirements of specific applications. This issue is already acute in the design of microelectronics. It is even more so for nanoelectronics and "MtM" technologies, wherein both multiscale size effect and multimaterial compatibility, stability, and reliability will be key to success. Among many challenges, characterization and modeling of material and their interface behavior need more attention, especially for multiscale, multiphysics, and time-dependent situations.
- Integrated process development via mastering the requirements and interaction among IC, package, and multifunctional systems.
- Establishing reusable design platform, process, and assembly environment for cost-effective mass implementation of a wide range CMOS compatible "MtM" devices, such as sensor, actuator, MEMS, and NEMS.
- Multiscale and multiphysical simulation, modeling, and characterization for "MtM" processes and products.
- Novel multifunctional system architecture and design.
- Designing for reliability, testability, compatibility, and manufacturability.

1.2.3 Beyond CMOS

"Beyond CMOS" covers the most advanced research activities to allow scaling of logic and memory functions to continue beyond the physical limits of Silicon-based CMOS technology [1, 5].

After more than 40 years of scaling according to Moore's law, we are rapidly approaching the CMOS scaling limit because we are reaching a point where an increase in power consumption coincides with an insufficient increase in operating speed. These highly undesirable effects are caused by a decrease in channel mobility and an increase in the interconnection resistance for smaller process geometries. The power consumption is largely due to increased leakage currents, short channel effects, source-drain tunneling, and p/n junction tunneling. Moreover, interconnections are increasingly becoming a limiting factor: the decrease in the pitch of interconnections and in the size of contacts and vias is causing an increase in overall resistance, while the reduced spacing is increasing propagation capacitances. The consequence is an increase in propagation delays and in the power consumption related to charging and discharging of interconnects to a point that already in today's 90-nm logic devices, a significant portion of transistors is dedicated only to driving interconnection lines, without playing any computational role. Physical limits of existing materials have been reached, and no significant progress can be expected in this area.

On top of that, the increasing impact of defects and the high level of complexity in both lithography and design have resulted in manufacturing costs rising dramatically. At the same time, the variability induced by the process variation at this nanoscale impacts also the yield and thus the cost. Even without taking into account the physical limits, all these combined effects push us closer to a point of reaching the limit of CMOS scaling.

There are a large numbers of different "beyond CMOS" options – but most are in an embryonic preindustrial phase. They can be realized via two different approaches. One is a gradual and evolutionary approach, by introducing new concepts and structures into the conventional CMOS technology. Another is the disruptive technology for replacing CMOS for some specific applications.

The evolutionary approach is based on the introduction of a new device, architecture, material, or process step inside the conventional CMOS technology, to solve one specific issue. It imposes the important constraint of CMOS compatibility, but has the advantage of reusing the huge amount of know-how developed till now. Examples are carbon nanotube transistor, nanowires, single electron devices, Resistance Change Memory, Ferroelectric FET Memory, defect and variation tolerant architectures, optical interconnect, RF interconnect, III-V compounds, magnetic materials, etc.

For disruptive approach, one can take the future computation scaling as one example, which requires capability using new state variables, efficient information transfer, and managing the heat transfer more efficiently.

New State Variables Many different information carriers need to be explored in addition to charge and none of them currently stands out as a clear winner. Examples include spin, molecular state, photons, phonons, nanostructures, mechanical state, resistance, quantum state (including phase), and magnetic flux.

Spintronics (spin-based electronics) has many potential advantages, including low power operation, nonvolatility, and co-localization of data processing and storage. Metal-based spintronics is likely to be first introduced for data storage applications using either spin torque switching or domain wall effects. Semiconductor-based spintronics could find application in data processing, though major breakthroughs are needed in materials (e.g., semiconductors with a higher critical temperature), devices (e.g., injection/detection trade-off), cointegration with CMOS, or in exploring promising physical phenomena (e.g., "dissipationless" spin current). Spintronics using half-metals and molecules also need to be explored. It should be stressed that no clear information processing device has so far emerged as a promising candidate to replace or supplement CMOS logic.

Molecular electronics is targeted at creating functional blocks at the molecular or supramolecular level that could be assembled in more complex functions. Fully molecular-based complex systems including interconnected molecular logic and molecular memory devices have still to be demonstrated. Limited molecular logic, memory, and interconnect functions have been shown, based on different types of molecules, but their integration into a single chip is still an issue. The first potential application is using the bistable behavior of certain molecules to produce memories with an extremely high density. We are still at a very early stage, where the reproducibility of reported results is not always evident. Specific issues, such as contacting the molecule, carrying enough current to provide noise immunity and a reasonable fan-out, and the addressing and read out of specific blocks remain to be solved.

Information Transfer Although significant research is carried out worldwide on "alternative" devices, no significant technological breakthrough has been achieved so far on information transfer in an integrated circuit. One of the more likely contenders to replace electromagnetic communication (i.e., information transfer through charge current in a metallic wire) is photon communication (i.e., light in the visible or IR range). More specifically, the very dynamic fields of nanophotonics, including plasmonics, allow the confinement and interaction of photons and electrons in a small volume, opening up the possibility of processing data at high frequency without compromising integration density.

It should be stressed that significant progress will come not only from breakthroughs in materials and device research, but also more significantly from the creative interaction of technology progress with progress in layout, design, software, and system research. For example, an optimized architecture through a better coding and localization of data is likely to bring significant improvement in information transfer techniques. Finally, more disruptive approaches such as stochastic resonance need to be explored.

Heat Transfer Management The emerging field of phononics aims to control phonon movement by using engineered nanostructures. It brings new opportunities in the interaction between quasiparticles (electrons, photons, spins, etc.) and phonons, potentially allowing better heat removal, isolation from thermal noise, and better carrier mobility.

Beside the computation scaling, the following issues are also important for the successful implementation of disruptive "beyond CMOS" technologies.

System Architecture At the device level, it is important to pay attention to the "systemability" of emerging devices, i.e., the capacity of a device to be integrated into a complex system. Moving up to functional block level, some emerging devices may offer new information processing paradigm by performing "dissipationless" computation in limited domains where information carriers will not encounter scattering (in a "ballistic" regime) or where phase information is maintained (as in quantum computing before decoherence occurs).

Emerging devices are expected to be more defective, less reliable, and less controlled in both their position and physical properties. It is therefore important to go beyond simply developing fault-tolerant systems that monitor the device at runtime and react to error detection. It will be necessary to consider error as a specific design constraint and to develop methodologies for error resiliency, accepting that error is inevitable, and trading off error rate against performance (speed, power consumption, etc.) in an application-dependent manner.

Using a similar approach, analog blocks of low complexity built with emerging devices may eventually find more extended use in balancing power consumption, in analog-digital partitioning and in signal restoration.

Von Neumann architectures – or more generally, programmable digital systems – will have to be reconsidered, especially with respect to optimizing the localization of data processing and storage and in coengineering the software and the architecture (e.g., parallel processing), without underestimating the legacy of more than 40 years of continuous development in classical electronic systems.

Open issues such as giving up deterministic computation (e.g., in neural networks or DNA computing) or addressing emergent behavior in complex systems are new research fields where multidisciplinarity is the key.

Physicists, designers, and system researchers cannot afford to work in isolated mode any more, focusing on their own field and having well-defined interfaces and handover mechanisms to other areas. The main challenge is to close the triangle between applications, emerging devices, and design resource constraints in order to manage complex interaction between the different levels of system development. It is therefore essential to develop real multidisciplinary cooperation between all those stakeholders who play a part in optimizing the overall performance of a system.

Manufacturing Opportunities As we enter into the nm scale, the ability to manufacture billions of devices on a chip while maintaining full control over their properties is an overwhelming challenge that will probably lead to unbearable development

and production costs. While it is difficult to predict which new processes will make their way into future manufacturing lines, there may be a comeback for chemistry, especially as development of the so-called "supramolecular toolbox" progresses and selective processes (e.g., surface functionalization) become more commonly used. Directed self-assembly (a "bottom-up approach") and possibly bioinspired and templated assembly are attractive concepts for low-cost manufacturing that need further investigation, although the fabrication of complex nonregular integrated systems has still to be demonstrated. Bioinspired manufacturing processes may be useful to address defect-resiliency and the self-repair of defective systems.

Future successful technologies may have to combine novel bottom-up and more traditional top-down manufacturing to achieve increased performance and cost effectiveness. Finally, as discussed in the previous paragraphs, research into new architectures may also help to relax the need for a deterministic approach to controlling the properties of the elementary devices.

Enabling "MtM" While a longer time frame is expected to implement disruptive "beyond CMOS" technology for IC, a significant achievement can be realized in a short or middle term, by developing "beyond CMOS" technology for novel "MtM" applications. At the moment, one can actually buy a handful of electronic products made with carbon nanotubes (CNT). Examples are CNT sensors (see Fig. 1.8), probe tips, and transparent conductive films. As one of the novel solid materials, nanowires have also received much attention from the R&D community as components for electrical circuits, sensors, or light emitting sources based on CMOS compatible processes. Although the R&D activities for CNT and nanowires were initiated to address the future need of IC technologies beyond the physical limits of CMOS, more and more R&D activity nowadays is devoted to using CNT and

Fig. 1.8 Cell interacting with nanotube structure

nanowires to create "MtM" products. Other examples are using spin-torque for RF detection, plasmonics for more sensitive optical sensors, nanodevices for molecular recognition, or nanostructured materials for enhanced energy efficiency. It is expected that increased effort in developing disruptive "beyond CMOS' technology for "MtM" applications will eventually speed up the development and implementation to replace CMOS.

Today there is no acceptable candidate to replace CMOS devices in terms of the four essential metrics needed for successful applications: dimension (scalability), switching speed, energy consumption, and throughput. Moreover, when adding reliability, design-ability, and mixed-signal capability as other key metrics, CMOS dominance is even more obvious. ITRS Emerging Research Devices [12] proposes criteria to evaluate the potential of emerging devices and circuits, wherein continuity is largely dominant, and these criteria are to evaluate the potential of emerging technologies in terms of their added value compared to scaled CMOS, and clearly oriented toward dense computing and memory applications. The analysis presented in the ITRS-ERD document is based on defining a set of criteria for logic and another for memories, and applying them to potential technologies such as given below.

- *Logic*. Scalability, performance, energy dissipation, gain, operational reliability, operating temperature, CMOS technological and architectural compatibility
- *Memories*. Scalability, performance, energy dissipation, OFF/ON ratio, operational reliability, operating temperature, CMOS technological and architectural compatibility

The metrics above primarily address the CMOS and thus concern the pursuit of the "MM" approach and target a "beyond CMOS" technology corresponding to "an information processing technology that enhances the scaling of functional density and performances while simultaneously reducing the energy dissipated per functional operation and that could be realized using a highly manufacturable fabrication process."

However, it is also essential to consider complementary criteria that take into account the system-related issues, such as, system-ability; ability to co-host memory, logic, and communication; handling of device variability; existence of an appropriate architecture; handling of analog and mixed signals; and potentials for combining "MM" and "MtM."

Finally, attention is needed to the timeline of "beyond CMOS" development. Emerging devices are likely to be introduced initially in the form of low complexity blocks integrated into complex systems, before moving to more complex regular structures and, at a later stage, to complex random logic computing blocks. After the basic functionality of an emerging device ("proof of concept") has been demonstrated, it is expected that a few optimized components integrated into a system would be the next logical step. At this point, major issues will still need to be resolved regarding manufacturing techniques and the reproducibility of performance, as well as in terms of design methodologies and system architectures.

1.2.4 Systems Architecture and Design

System architecture and design are increasingly important for semiconductor solutions [5]. The increasing complexity of solutions driven by the creation in many areas of new industrial and consumer applications requires an increasingly modular design approach, developing more innovative building blocks and flexible system architectures with higher integration capabilities. The semiconductor value chain is becoming more differentiated and traditional players are moving forward along the entire value chain to provide systems solutions as required by the market. The trend includes moving from components to solutions, e.g., in radio frequency (RF), from modules to fully integrated solutions and from components business to systems business (e.g., camera systems with sensors, mechanics, lenses; telecom systems; and architectural systems).

The increasing gap between nanoelectronics hardware technology and complex system design is an urgent problem to be solved yet. As a consequence, we are now facing the reality of being able to develop new technology nodes every 2–3 years while the time frame for new design tools is in the order of 10 years. This discrepancy is unacceptable in the future and a profound change in people's mindset and substantially increased effort in development are needed.

Moving to nanoelectronics and emerging of "MtM" technologies enable a tremendous increase in the functionality of electronics systems and in the applications of SoC and SiP products. The demanding solutions must be capable of capturing formal design specifications provided by system houses, allowing high-level system and architecture exploration within the underlying constraints of available implementation technologies. All aspects of product development must be embraced, including digital, analog/mixed signal, power electronics, and embedded software in conjunction with nonelectrical components like MEMS and NEMS. This will require expertise drawn from the many different disciplines involved in product design (system level design, HW and SW co-design, IC-packaging-system co-design, product/process and equipment co-design, verification, and physical implementation with constraints for test, reliability, and manufacturability). Several challenges should be solved with respect to design [1, 11]:

Design for Heterogeneous System The complex and heterogeneous system assemblies will increasingly be interconnected three-dimensionally (wafer level packaging, TSV), and controlled by an ever increasing amount of software. The design of these smart and heterogeneous systems will require new methods and approaches to compose these compact systems. Interfaces linking digital/analog, hardware/software, electrical/mechanical, etc. need to be handled at different abstraction levels. Another important issue is the design platform and reuse technology. The current trend toward compact and heterogeneous systems such as SiP requires extension of the classical SoC-centric design flow to efficiently support the "MtM" needs, which is, by definition, extremely diverse. To design compact sys-

tems in the "MtM" domain, an "MtM" integration platform will be required, which can serve as a "virtual prototyping" environment. It is economically not sustainable without developing a design platform and reuse technology to account for the needs of very diverse "MtM" product characteristics.

Design for Manufacturability Design for manufacturability (D4M) is aimed to accelerate process ramp-up and to enhance process yield, robustness, and reliability. To be able to do so, effort is needed to develop and enable random and systematic yield loss estimations from design through yield models and process-aware design flows, enabling yield optimization early in the design flow and reducing costly iterations. In future, estimation of the effect of systematic yield hazards on the final yield of a complex SoC or SiP will become extremely difficult. Given the very large expected increase in NRE and development costs, this will have to be done at an early stage of the design cycle and will be an indispensable step.

Design for Reliability Design for reliability (D4R) is aimed to predict, optimize, and design upfront the reliability of products and processes. It is also called virtual prototyping method. D4R requires a range of research activities including gaining a basic understanding of material behavior, degradation and failure mechanisms under multiloading conditions, by accelerated reliability qualification tests and advanced failure analysis, in combination with various accurate and efficient multiphysical and multiscale simulation models in order to predict the failure evolution. Other issues are increasing occurrence of soft errors, variability, and soft failure mechanisms beyond 90-nm technology, which demand research into self-repairing circuits and self-modifying architectures. The issues that need special attention are as follows:

- Integrated multiscale (from atomistic to macro, considering the strong size and surface effect), multiphysics (electrical, mechanical, thermal, physics, chemical, etc.), multidamage (cracks, delamination, fatigues, electromigration, voids, creep, degradations, etc.), and multiprocess (wafer, micromachining, packaging, assembly, qualification and application profile) modeling incorporating the important loading history in order to understand and predict the performance and reliability. Herein, new algorithms and simulation tools have to be developed.
- Advanced failure analysis techniques and correlation methods to localize the multiphysics-based failure modes and the associated process for multifunctional SiP, and to understand the failure mechanisms and their interaction.
- Novel experimental methods and techniques to extract material/interface and total system behavior, in order to provide inputs for modeling and simulation on one hand, and to verify the modeling results and design rules on the other hand, covering both nano- and macroscales.
- Reliable and efficient reliability qualification methods and physics of failure-based correlation models to accelerate reliability qualification tests.

Design for Testability Design for testability (D4T) is to secure functionality, quality, and reliability before release. It is a challenging issue especially for "MtM" applications with multifunction products, wherein test strategy, methodology, and equipment need to be further developed. Other reasons of D4T concern are the growing costs for Automatic Testing Equipment systems and test programming that are needed for testing high-volume, high-speed, and high-quality products. According to the ITRS roadmap, testing's share of the total manufacturing cost tends to approach 50% if no effective counteractions are taken. Besides the cost issue, the increasingly tightening time-to-market windows, the multifunction design targets, and the growing customers' expectations for further improvement of product quality cause equally serious problems. Key test development activities include test specifications/test bench conception and diagnostic; test program development (test vector conversion/test program synthesis); test program debug and optimization (test characterization/optimization); and test pattern generation. Several challenges associated with the testability of compact "MtM" systems are identified as follows:

- Testers are typically specialized to different functions. With compact "MtM" system, all technologies can be present in the package which makes conventional testing with just one tester type a big challenge. Multiple insertion testing is an option.
- A compact "MtM" system is truly a system and it is easy to put components into such a system in a way that is inaccessible from the outside pins, which means that testing of a chip may have to be done through another device, most likely in a "functional" way instead of a "structural" way. Thus test time and test completeness are big challenges.
- For the multifunctional SiP, the test problems potentially get more difficult, depending on the test requirements of the MEMS. Some types of MEMS may require a physical stimulus as part of the test process (pressure, acceleration, etc.), which can lead to test fixturing difficulties.
- For software testability means that configurable functions exist that can perform self-tests. In addition, functions should have clear semantics and results that do not depend too much on the order of calling. Separation of concerns in the software is crucial. Advanced component- and aspect-oriented development methods will aid to this.
- Testing strategies become increasingly platform based. Driven by the specific application market, they are becoming more local and more supported by dedicated application engineers. As a consequence, the development and implementation of such test platform systems require increased flexibility and ease of access globally. The flexibility of platforms will allow their being more widely used in probe, final test, or engineering environments.

1.2.5 Software

Software is playing more and more important role in semiconductors. The know-how of dedicated semiconductor applications is increasingly implemented in software. Despite the portable nature of software, the close interaction between

software and hardware in embedded control is still essential for effective implementation. The functionality and market appeal of "MM," "MtM," and their integrations strongly depend on the contribution of the software that is embedded in it. Superior hardware technology alone cannot guarantee business success of future semiconductors. As a well-known example, huge effort is made to lower dielectric constant k in the IC backend stacks from 2.3 to 2.0, which is a 15% improvement, but this effort so far leads to serious yield issues while better software optimization can improve power efficiency and performance by factors between 2 and 10 [5]. It becomes obvious that simultaneous changes are needed in process technology, materials, device architectures, and design technologies coping with the need to create software-dominated platforms for future applications.

There is a clear trend for more and more software with greater functional diversity and architectural complexity. Taking the automotive industry as an example, it is estimated that 70% of future innovations will be software related and most other sectors are moving in a similar direction. The growing need for embedded software is fuelled by a need for additional and heterogeneous functionality, real-time performance, distribution across subsystems, reuse for multiple systems or in a platform, and long life time reliability needs. As systemability is becoming one of the key success criteria for future technology development, there is an urgent need to integrate nanoelectronics technology with embedded systems and system level design.

Another trigger for hardware and software codesign is due to the fact that the dramatically increased number of design tasks and their complexity are already leading to a phenomenon known as the "design gaps" - the difference between what should theoretically be integrated into systems and what can practically be designed into them, and what should be manufactured vs. what has been designed.

The main characteristics of this software trend are as follows [13]:

- Any complex semiconductor system embeds electronic parts and related software. There is a clear correlation between the attractiveness of the product and the total amount of electronics it embeds (hardware and software). The software controls the user-visible part and determines the price point and margin of the product. The software part is often used to create differentiation among products with similar dedicated hardware.
- The increasing complexity and focus of semiconductor applications on dedicated solutions and systems integration, implying sophisticated software and human interface functionalities, requires increasingly specialized software capabilities that only providers with a critical mass of skills and service resources are able to offer.
- Semiconductor vendors are required to provide the software ecosystem. Therefore, software providers increasingly offer full integration and services packages. Besides, the semiconductor industry is also required to provide more and more reference design and platforms. This means that the semiconductor industry provides not only ICs but also the systems software on top of which the OEMs can customize their products, including hardware and system software. The implementation of a complex platform already requires more software designers than hardware designers.

- As the variety of applications is broadening, the development of more advanced SW tools and packages is becoming increasingly sophisticated.
- In information processing, the trend is toward multiple cores. This will likely push design challenges even more toward SW. As a consequence of the increasing role of SW development by the semiconductor industry, design and embedded software R&D costs are rising faster than any other costs.

1.2.6 Heterogeneous Integration and Packaging

In the past several decades, semiconductors have been spending tremendous effort in developing and commercializing the Moore's law, leading to not only many breakthroughs and revolution in ICT, but also noticeable changes in the way of living of human being. While this trend will still be valid, reflected in the "MM" and "beyond CMOS," there are ever-increasing awareness, R&D effort, and business drivers to push the development and application of "MtM" enabling various nondigital functionalities. The future business opportunities and technology challenges will be the integration of Moore's law focusing mainly on digital functions with "MtM" focusing on mainly nondigital functions via heterogeneous integration and packaging.

Heterogeneous integration and packaging, at the center of any micro/nanoelectronics system creation, and the bridge between nano/micro semiconductor technology with macroscale applications, is the final manufacturing process transforming semiconductor devices into functional products for the end users. It provides electrical and multiphysical connections (e.g., bio connection for bio-SiP) for multisignal transmission, power input, and voltage control. It also provides for thermal dissipation, construction carrier, and the physical protection required for reliability. In the process of "MM" and "MtM" integration, heterogeneous integration and packaging play an essential role as the key enabler governing the multifunctional performance, size, weight, cost, and reliability of the final products. Heterogeneous integration will not only bring various multifunctional components together into one package but also provide an interface to the application environment. It therefore represents the glue between the world of micro/nanoelectronics devices and systems that humans can interact with. Heterogeneous integration has to ensure not only the integration of components based on different technologies and materials, but also the targets for miniaturization.

As one of the important packaging technologies, SiP refers to (multi-) functional systems built up using semiconductors and/or in combination with other technologies in an electronic package dimension. SiP focuses on achieving the highest value for a single system package, by extreme miniaturization, heterogeneous function (such as electrical, optical, mechanical, bio-, etc.) integration, short-time-to-market, and competitive function/cost ratio. Its concept applies to quite diverse technologies, such as semiconductors, sensors, actuators, power, RF modules, solid-state lighting, and various healthcare devices. To distinguish between

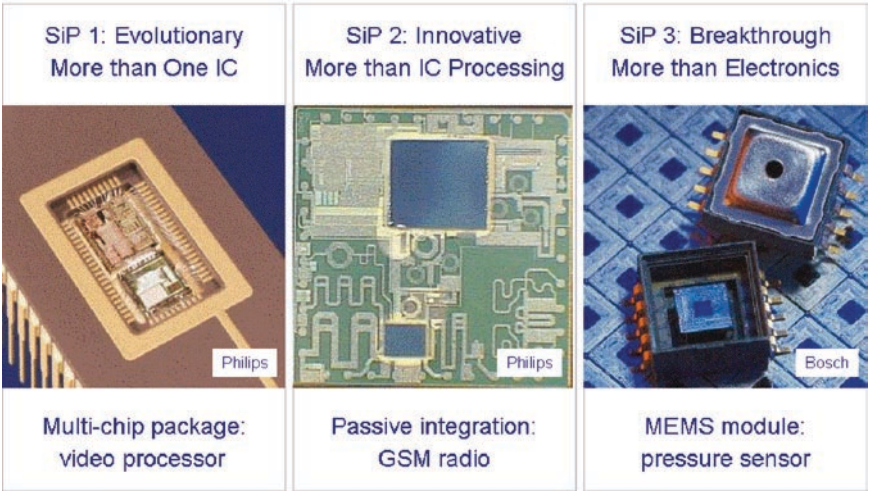

Fig. 1.9 Examples of three types of SiP

various SiPs, one can characterize SiPs into three categories (see Fig. 1.9). The first category refers to packages with multi-dies, such as McM, PiP, and PoP. The second category refers to subsystems built up using more than just IC process, such as passive integration. The last, the most challenging one, refers to compact system with more than electric functions, built up using multitechnologies and heterogeneous integration.

In the current semiconductor business, unfortunately heterogeneous integration and packaging are undervalued and underdeveloped. Many people consider packaging as low-tech and easy manageable process. There is a large gap between strong CMOS-based semiconductor device innovation capability and limited heterogeneous integration and packaging knowledge and know-how. It is also reflected by the fact that there are no industry-implementable roadmaps for nano-interconnect, nanopackaging, nanoassembly, and multifunction integration platform. For the coming decade, heterogeneous integration and packaging will be the bottleneck for the success of semiconductor industry, wherein packaging design concept, packaging architecture (often equivalent to system architecture), materials, manufacturing process, equipment, and system integration technology all need innovations and breakthroughs in an unprecedented speed.

On top of the above-mentioned roadmap issue, industries are confronted with ever-increased design complexity, dramatically decreased design margins, increased chances and consequences of failures, decreased product development and qualification times, and increased difficulties to meet quality, robustness, and reliability requirements. Other challenges for heterogeneous integration and packaging are given below: