

# CMOS Active Inductors and Transformers

Principle, Implementation, and Applications

Fei Yuan

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 Springer

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# Preface

CMOS spiral inductors have found a broad range of applications in high-speed analog signal processing and data communications. These applications include bandwidth enhancement, delay reduction, impedance matching, frequency selection, distributed amplifiers, RF phase shifters, low-noise amplifiers, and voltage-controlled oscillators, to name a few. The effectiveness of these inductors, however, is affected by a number of limitations intrinsic to the spiral layout of the inductors. These limitations include a low quality factor, a low self-resonant frequency, a small and non-tunable inductance, and the need for a prohibitively large silicon area. The use of CMOS spiral transformers in RF applications such as low-noise amplifiers, power amplifiers, and LC oscillators has emerged recently. These transformers are constructed by coupling two spiral inductors via a magnetic link. They offer the advantages of a reduced silicon consumption and increased inductances. The limitations of spiral inductors, however, are inherited by spiral transformers.

Inductors and transformers synthesized using active devices, known as active inductors and transformers, offer a number of unique advantages over their spiral counterparts including virtually no chip area requirement, large and tunable inductances with large inductance tuning ranges, large and tunable quality factors, high self-resonant frequencies, and full compatibility with digital oriented CMOS technologies. Active inductors and transformers have found increasing applications in high-speed analog signal processing and data communications where spiral inductors and transformers are usually employed. As compared with spiral inductors and transformers, the applications of CMOS active inductors and transformers are affected by a number of limitations intrinsic to synthesized devices. These limitations include a small dynamic range, poor noise performance, a high level of power consumption, and a high sensitivity to supply voltage fluctuation and process variation.

This book provides a comprehensive treatment of the principle, topologies, and characteristics of CMOS active inductors and transformers, and an in-depth

examination of their emerging applications in high-speed analog signal processing and data communications. The materials presented in the book are based on the work of many researchers who contributed to the theory and design of CMOS active inductors and transformers. In recognition of their contributions, the active inductors and transformers presented in this text are named in the names of the researchers. For active inductors and transformers developed by more than two researchers, although due to the space constraint, only the name of the first author of the work is used to name the active inductors and transformers, the contributions of all other authors are equally recognized. This is reflected by the presentation of the full authorship of the work in the *References* of the book. The same approach is followed in the presentation of CMOS active inductor/transformer bandpass filters, oscillators, and other sub-systems.

This book consists of two parts : Part I - *Principle and Implementation of CMOS Active Inductors and Transformers*, and Part II -*Applications of CMOS Active Inductors and Transformers*.

Part I of the book deals with the topologies, characteristics and implementation of CMOS active inductors and transformers. This part consists of three chapters.

Chapter 1 starts with a brief investigation into why inductive characteristics are critically needed in high-speed applications. This is demonstrated with the applications of inductors and transformers in LC oscillators, impedance matching networks, RF phase shifters, RF power dividers, frequency selection networks, in particular, RF bandpass filters, and low-noise amplifiers. A detailed examination of the design constraints of monolithic inductors and transformers is followed. The advantages and design challenges of CMOS active inductors and transformers are examined in detail.

Chapter 2 presents the principles of the synthesis of inductors using gyrator-C networks. Both lossless and lossy single-ended and fully differential gyrator-C active inductors are studied. The important figure-of-merits that quantify the performance of active inductors including frequency operation range, inductance tunability, quality factor, noise, linearity, stability, supply voltage sensitivity, parameter sensitivity, signal sensitivity, and power consumption are examined in detailed. The details of the CMOS implementation and analysis of single-ended and fully differential active inductors are presented. The circuit implementation and characteristics of published CMOS active inductors are examined in detail.

Chapter 3 focuses on the principles of the synthesis of CMOS active transformers. Both lossless and lossy gyrator-C active transformers are studied. The characterization of active transformers including stability, frequency operation range, the tunability of self and mutual inductances, turn ratios, coupling

factors, voltage and current transfer characteristics, impedance transformation, noise, quality factors, linearity, supply voltage sensitivity, parameter sensitivity, and power consumption is examined in detail. The CMOS implementation of several published CMOS active transformers is presented and their characteristics are analyzed.

Part II of the book focuses upon the emerging applications of CMOS active inductors and transformers in high-speed analog signal processing and data communications. This part consists of four chapters.

Chapter 4 investigates the implementation and characteristics of RF bandpass filters using CMOS active inductors. The chapter starts with a detailed investigation of the characterization of bandpass filters. Bandwidth, 1-dB compression points, third-order intercept points, noise figure, noise bandwidth, spurious-free-dynamic range, frequency selectivity, and passband center frequency tuning are examined. It is followed by a detailed examination of the configurations of RF bandpass filters with active inductors. Wu bandpass filters, Thanachayanont bandpass filters, Xiao-Schaumann bandpass filters, Thanachayanont-Payne bandpass filter, and Weng-Kuo bandpass filters are studied and their performance is compared.

Chapter 5 looks into the realization of the building blocks of high-speed transceivers using CMOS active inductors and transformers. The use of CMOS active inductors in low-noise amplifiers, optical front-ends, RF phase shifters, RF modulators, RF power dividers, and Gb/s serial-link transceivers is examined in detail.

Chapter 6 starts with a brief review of the fundamentals of electrical oscillators. Both ring and LC oscillators are investigated. The use of CMOS active inductors in improving the performance of ring oscillators is investigated. The presentation continues with a close examination of the use of CMOS active inductors in LC oscillators. A special attention is given to the comparison of the phase noise of these oscillators. LC oscillators and LC quadrature oscillators using CMOS active transformers are also studied.

Chapter 7 presents the theory of current-mode phase-locked loops (PLLs) and examines the intrinsic differences between voltage-mode and current-mode PLLs. The chapter starts with an in-depth study of the configurations and characteristics of voltage-mode PLLs. Both type I and type II voltage-mode PLLs are studied. It then moves on to investigate current-mode PLLs with CMOS active inductors and transformers. The loop dynamics of these PLLs are investigated in detailed. Three design examples are utilized to demonstrate the performance of current-mode PLLs with active inductors and active transformers.

The materials of the book are presented with an emphasis on both the evolution of each class of circuits and a close comparison of their advantages and limitations. The examples given in the book were implemented in TSMC-

0.18 $\mu\text{m}$  1.8V and UMC-0.13 $\mu\text{m}$  1.2V CMOS technologies, and analyzed using SpectreRF from Cadence Design Systems with BSIM3v3RF device models that account for both the parasitics and high-order effects of MOS devices at high frequencies. Readers are assumed to be familiar with the fundamentals of electrical networks, microelectronic devices and circuits, signals and systems, and basic RF circuits.

This book is the first text that provides a comprehensive treatment of the principle, implementation, and applications of CMOS active inductors and transformers. It is a valuable resource for senior undergraduate / graduate students and an important reference for IC design engineers.

Although an immense amount of effort has been made in preparation of the manuscript, flaws and errors will still exist due to erring human nature. Suggestions and corrections will be gratefully appreciated by the author.

FEI YUAN

DECEMBER 31, 2007

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PART I

PRINCIPLE AND IMPLEMENTATION OF  
CMOS ACTIVE INDUCTORS & TRANSFORMERS

# Chapter 1

## INTRODUCTION

CMOS spiral inductors and transformers have found a broad range of applications in high-speed analog signal processing including impedance matching and gain-boosting in wireless transceivers, bandwidth improvement in broadband data communications over wire and optical channels, oscillators and modulators, RF bandpass filters, RF phase shifters, RF power dividers, and coupling of high-frequency signals, to name a few. Traditionally, passive inductors and transformers are off-chip discrete components. The need for off-chip communications with these passive components severely limits the bandwidth, reduces the reliability, and increases the cost of systems. Since early 1990s, a significant effort has been made to fabricate inductors and transformers on a silicon substrate such that an entire wireless transceiver can be integrated on a single substrate monolithically. In the mean time, the need for a large silicon area to fabricate spiral inductors and transformers has also sparked a great interest in and an intensive research on the synthesis of inductors and transformers using active devices, aiming at minimizing the silicon consumption subsequently the fabrication cost and improving the performance.

This chapter looks into the characteristics of spiral and active inductors and transformers, both their advantages and limitations, and the impact of these characteristics on the applications of these devices. Section 1.1 demonstrates the critical need for an inductive characteristic in high-speed applications. The characteristics of spiral inductors and transformers are examined in Section 1.2. In Section 1.3, we investigate the pros and cons of active inductors and transformers. The chapter is summarized in Section 1.4.

### **1.1 Inductive Characteristics in High-Speed Applications**

Inductive characteristics are critically needed in high-speed applications to improve the performance of the systems, such as improving bandwidth and

boosting gain, and to perform specific tasks, such as impedance matching and frequency selection. These applications include LC tank oscillators, bandwidth enhancement in broadband communications, impedance matching in narrow-band communications, phase shifting for RF antennas and radars, RF power dividers, frequency selection, in particular, RF bandpass filters, RF power amplifiers, and gain boosting of RF low-noise amplifiers.

### 1.1.1 LC Oscillators

One of the key applications of inductors and transformers in wireless communications is the construction of LC oscillators. As compared with ring oscillators, LC oscillators with spiral inductors or transformers offer the key advantage of a low level of phase noise. They are widely used in wireless communication systems where a stringent constraint on the phase noise of oscillators exists. Frequency tuning of LC oscillators with spiral inductors or transformers is typically done by varying the capacitance of the LC tanks as the inductance tuning of spiral inductors or transformers in a monolithic integration is rather difficult. These variable capacitors are usually realized using MOS varactors and offer a relatively small capacitance tuning range, subsequently a small frequency tuning range of the oscillators. Because the need for the frequency tuning range in narrow-band wireless applications is much relaxed as compared with that for clock and data recovery in broadband data communications over wire lines or optical channels, the capacitance-based frequency tuning usually provides an adequate frequency tuning range. Table 1.1 compiles some of the recently published work on LC oscillators with either spiral inductors or spiral transformers.

### 1.1.2 Bandwidth Improvement

Bandwidth is of a critical concern in broadband communications, such as optical front-ends and data communications over wire links. The bandwidth of a circuit is set by the time constant of the critical node, i.e. the node that has the largest time constant, of the circuit. Three approaches, namely *inductive peaking*, *current-mode signaling*, and *distributed amplification*, are widely used to improve the bandwidth of circuits.

- *Inductive peaking* - The idea is to place an inductor at the node where a large nodal capacitance exists such that the first-order RC network associated with the node is replaced with a second-order RLC network. Because a RLC network has three different modes of operation, namely over damped, critically damped, and under damped. The bandwidth in these three cases differs with under-damped RLC systems exhibit the largest bandwidth. Both shunt peaking [11, 12] and series peaking [13], have been used, as shown

Table 1.1. Performance comparison of CMOS spiral inductor / transformer LC VCOs.

Reference	Tech.	$f_o$ [GHz]	Tuning range	Phase [dBc/Hz]	Power [mW]
Straayer <i>et al.</i> [1] (2002)	0.35 $\mu\text{m}$	1.7	6.3%	-138@0.6MHz	35*
Back <i>et al.</i> [2] (2003)	0.18 $\mu\text{m}$	8.08-7.83	3%	-108@1MHz	24*
Wang <i>et al.</i> [3] (2003)	0.18 $\mu\text{m}$	5.75-5.95	3.4%	-105@5MHz	18*
Gierkink <i>et al.</i> [4] (2003)	0.25 $\mu\text{m}$	4.57-5.21	13%	-124@1MHz	21.9*
Choi <i>et al.</i> [5] (2004)	0.25 $\mu\text{m}$	1.5	–	-100@1MHz	28.8*
Dehghani & Atarodi [6] (2004)	0.25 $\mu\text{m}$	5.8	4.4%	-134.6@3MHz	5.8
Kim <i>et al.</i> [7] (2004)	0.25 $\mu\text{m}$	2.27	–	-137@1MHz	30*
Chang & Kim [8] (2005)	0.18 $\mu\text{m}$	5.5-6.7	20%	-115@1MHz	5.76
Oh & Lee [9] (2005)	0.18 $\mu\text{m}$	11	2.73%	-109.4@1MHz	6.84
Soltanian & Kinget [10] (2006)	0.25 $\mu\text{m}$	1.755-2.123	19%	-120@0.6MHz	2.25

1. Legends : TVCO - Transformer VCO; QVCO - Quadrature VCO.
2. VCO proposed by Choi *et al.* is a source-injection quadrature VCO.
3. VCO proposed by Chang and Kim is a cascode-coupling quadrature VCO.
4. VCO proposed by Gierkink *et al.* is a super-harmonic coupled VCO.
5. VCO proposed by Oh and Lee is a back-gate transformer feedback VCO.
6. VCO proposed by Soltanian and Kinget is a tail-current shaped VCO.
7. \* Total power consumption including buffers. Otherwise, the power consumption of oscillator core only.

in Fig.1.1. It was demonstrated in [11, 12] that inductive shunt peaking can improve the bandwidth of a common-source amplifier by as much as 70%.

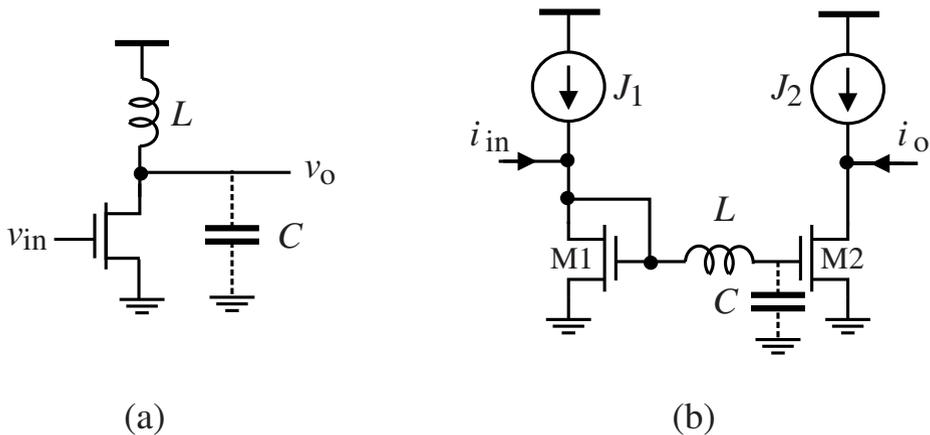


Figure 1.1. Inductive peaking. (a) Shunt peaking - The peaking inductor  $L$  is in parallel with the dominant capacitor  $C$ . (b) Series peaking - The peaking inductor  $L$  is in series with the dominant capacitor  $C$ .

- *Current-mode signaling* - A circuit is classified as current-mode if the information carriers of the circuit are the branch currents of the circuit. A key distinction between current-mode and voltage-mode circuits is that the nodal impedance of current-mode circuits is low whereas that of voltage-mode circuits is high. This distinct characteristic forms the foundation on which current-mode circuits are designed. Since the information processed by a current-mode circuit is represented by the branch currents rather than nodal voltages of the circuit, the swing of the nodal voltages of the circuit can be made small without sacrificing the fidelity of the signal. Current-mode circuits offer an improved bandwidth due to the following reasons : (i) Low nodal impedances - the low nodal impedances of current-mode circuits lower the nodal time constants of the circuits. (ii) Low voltage swing - the small swing of the nodal voltages of current-mode circuits reduces the amount of the time required to charge and discharge the nodes of the circuits [14]. It should be emphasized that the speed improvement using current-mode signaling is often moderate as lowering the nodal impedance of a nodal is often echoed with an increase in the capacitance of the node at the same time. Because each node is essentially a first-order RC network whose time constant is given by  $\tau_n = R_n C_n$ , where  $R_n$  and  $C_n$  denote the resistance and capacitance of the node, respectively, the net reduction in the nodal time constant is rather moderate.
  
- *Distributed amplification* - As pointed out earlier that the bandwidth or speed of a circuit is set by the time constant of the critical node of the circuit. An effective way to minimize the effect of the large shunt capacitance of the critical node is to break the large shunt capacitor into several smaller shunt capacitors and separate them with inductors such that the large shunt capacitor is replaced with a distributed LC network or a transmission line [15, 16]. Shown in Fig.1.2 is a common-source amplifier where an shunt-peaking inductor is employed at the drain of the transistor to offset the effect of the large output capacitance  $C$  arising from the large width of the transistor. Inductive shunt-peaking, though effective, can not deliver the needed bandwidth in this case. Notice that a transistor is typically laid out in a multi-finger fashion. This is equivalent to connecting  $N$  smaller transistors whose width is only  $1/N$  of that of the original transistor in parallel, as shown in the figure, where  $N$  is the number of the fingers of the transistor. Inductors can then be employed to separate these small transistors and form two transmission lines, one at the drain and the other at the source. Resistors  $R_{1-4}$  are for the purpose of impedance matching.

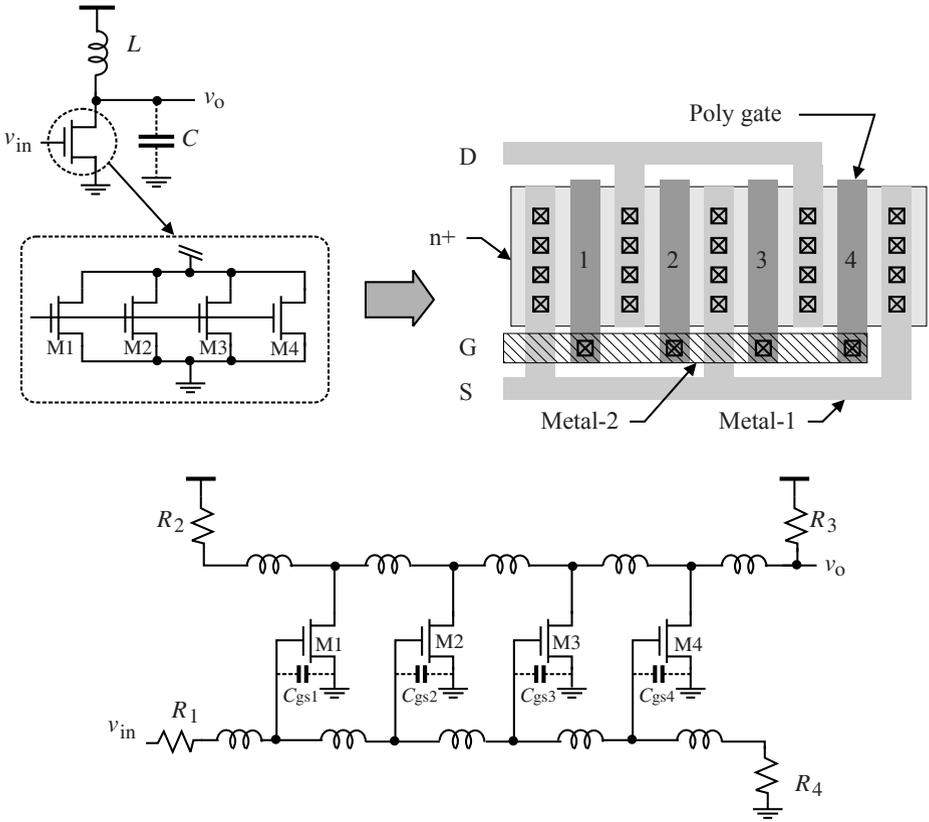


Figure 1.2. Distributed amplifiers.

### 1.1.3 Impedance Matching

Impedance matching is required between channels and high-speed circuits to minimize signal reflection at their interfaces. Resistors are usually used to provide a matching impedance in broadband communication systems as impedance matching is required over a broad frequency spectrum, as shown in Fig.1.3 where a shunt resistor termination at the far end of the channels is employed. Active termination where transistors are used as termination devices has also been used recently to take the advantage of the tunability of the termination resistance [14]. Frequency-dependent elements, such as capacitors and inductors, can not be used for impedance matching in broadband communication systems simply due to their frequency-dependent characteristics.

Most wireless communication systems operate in a narrow-band mode. A matching impedance in this case is only required over a very narrow frequency

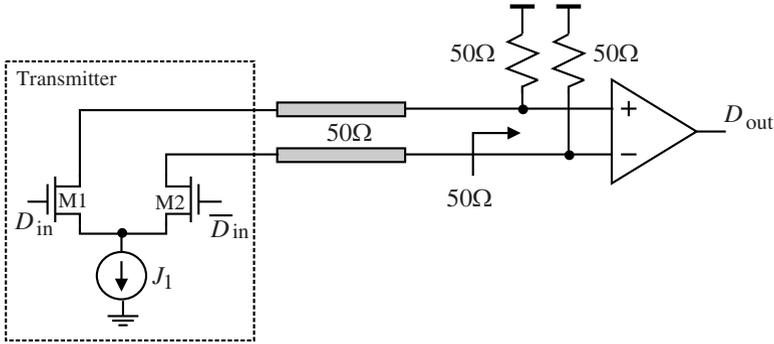


Figure 1.3. Impedance matching in high-speed current-mode serial links.

range. Although resistors can be used for these applications, the high level of the thermal noise of resistors disqualifies themselves from being used in wireless communications where a stringent constraint on the noise performance of the systems exists. Instead, noiseless elements such as capacitors and spiral inductors are widely used in narrow-band impedance matching because these frequency-dependent noiseless elements can provide the desired impedance in a narrow frequency band and at the same time keep the noise at the minimum [17, 18]. Shown in Fig.1.4 is a widely used termination scheme for narrow-band low-noise amplifiers. Neglecting  $C_{gd}$  and other parasitic capacitances, it is elementary to show that the input impedance of the LNA is given by

$$z_{in} = \left[ j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs1}} \right] + \frac{g_{m1}L_2}{C_{gs1}}, \quad (1.1)$$

where  $C_{gs1}$  and  $g_{m1}$  are the gate-source capacitance and transconductance of  $M_1$ , respectively. It is seen from (1.1) that the first term on the right hand side of (1.1) is reactive while the second term is resistive. The reactive term can be made zero by imposing

$$\omega(L_1 + L_2) - \frac{1}{\omega C_{gs1}} = 0. \quad (1.2)$$

The input impedance of the LNA in this case becomes purely resistive and is given by

$$z_{in} = \frac{g_{m1}L_2}{C_{gs1}}. \quad (1.3)$$

The need for two inductors  $L_1$  and  $L_2$  with  $L_1$  at the gate and  $L_2$  at the source is justified as the followings : Once the dimension of  $M_1$  is chosen,  $g_{m1}$  and

$C_{gs1}$  are determined. The desired input impedance of the LNA in this case can be obtained by adjusting  $L_2$ . Once  $L_2$  is chosen, the value of  $L_1$  can be tuned to ensure the total cancellation of the reactive part of the input impedance.

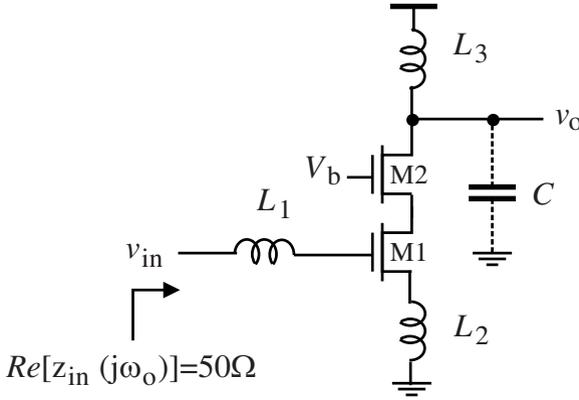


Figure 1.4. Impedance matching in narrow-band low-noise amplifiers.

### 1.1.4 Phase Shifting

A phase shifter is a uni-directional serial network inserted in a signal path so that the phase of the signal at the output of the signal path can be adjusted in a controlled manner [19, 20]. A well-designed phase shifter should possess the characteristics of a low insertion loss, a high return loss, and a large phase shift range. The common configuration of RF phase shifters is shown in Fig.1.5. The floating inductors are typically implemented using high-impedance metal lines. The tuning of the amount of the phase shift is carried out by varying the capacitance of the shunt varactors.

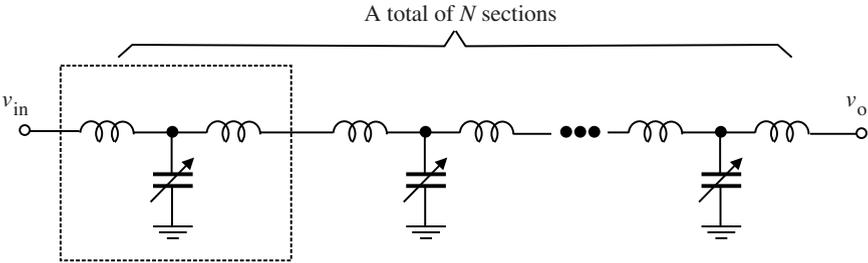


Figure 1.5. RF phase shifters with floating inductors and shunt varactors.

### 1.1.5 Frequency Selection

Bandpass filters with a high passband center frequency are used extensively in narrow-band wireless communications for RF band selection. These filters are traditionally implemented using lumped LC and surface acoustic wave (SAW) filters with SAW filters the most widely used. SAW filters, however, are not compatible with CMOS technologies. The recent effort on integrating RF bandpass filters on a silicon substrate is accelerated with the emergence of CMOS spiral inductors and transformers. A single-chip realization of RF transceivers with on-chip RF bandpass filters offers a number of critical advantages including a reduced assembly cost, increased system reliability, and improved performance. To compensate for the high insertion loss of spiral inductors at high frequencies, active negative resistors have been used to boost the quality factor of the spiral inductors. Table 1.2 tabulates some recently reported RF bandpass filters with spiral inductors and active Q-enhancement.

Table 1.2. Bandpass filter with Q-enhanced spiral inductors.

Reference	Year	Tech.	$f_o$	Tuning range
Kuhn <i>et al.</i> [21]	1997	$2\mu\text{m}$	0.2 GHz	4.5%
Duncan <i>et al.</i> [22]	1997	$0.8\mu\text{m}$	0.75 GHz	2.3%
Soorapanth-Wong [23]	2002	$0.25\mu\text{m}$	2.14 GHz	1.4%
Dulger <i>et al.</i> [24]	2003	$0.35\mu\text{m}$	2.1 GHz	13%
Kuhn <i>et al.</i> [25]	2003	-	0.9 GHz	2.2%
Bantas-Koutsoyannopoulos [26]	2004	$0.35\mu\text{m}$	1 GHz	11%
Kulyk-Haslett [27]	2006	$0.18\mu\text{m}$	2.368 GHz	1.3%

### 1.1.6 Gain Boosting

Traditional gain-boosting techniques such as cascodes and regulated cascodes lose their potency at high frequencies due to the increased gate-source and gate-drain couplings via the gate-source and gate-drain capacitors of MOSFETs. A technique that is widely used in boosting the voltage gain of narrow-band low-noise amplifiers (LNAs) is to use a LC tank as the load of the LNAs, utilizing the infinite impedance of ideal LC tanks at their self-resonant frequency. When a LC tank is used as the load of a common-source amplifier whose voltage gain is approximated by  $A_v \approx -g_m z_L$ , where  $g_m$  is the transconductance of the MOSFET and  $z_L$  is the load impedance, as shown in Fig.1.6, the large impedance of the LC tank at its self-resonant frequency  $\omega_o = \frac{1}{\sqrt{L_p C}}$

will significantly boost the gain of the amplifier at  $\omega_o$ . The resonant frequency of the tank is set to be the same as the frequency of the input of the LNA. Note that voltage gain of the amplifier at frequencies other than  $\omega_o$  is low.

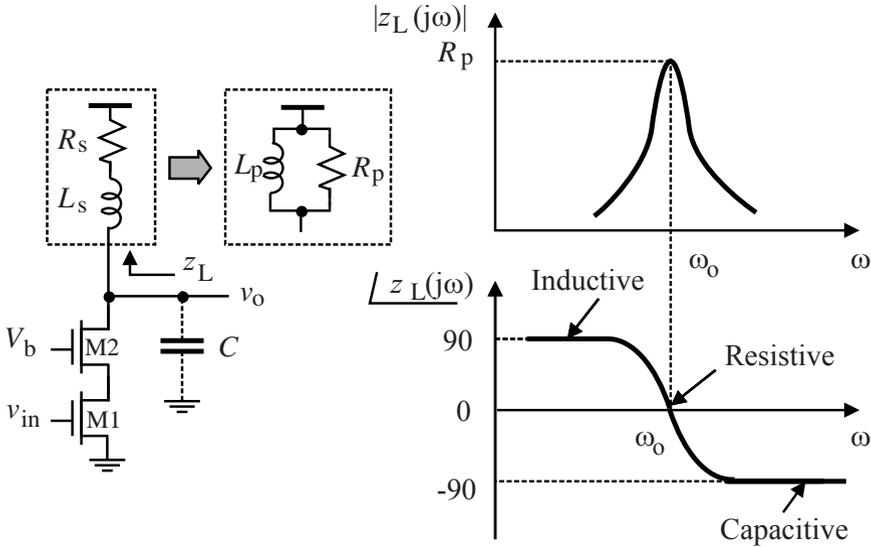


Figure 1.6. Gain boosting of low noise amplifiers using LC tank load.

### 1.1.7 Power Dividers

RF power dividers are traditionally realized using transmission lines. Lumped passive implementation of power dividers has also been used to reduce the size of the power dividers, however, at the cost of a high insertion loss and a limited bandwidth. Fig.1.7 shows the equivalent circuit of lumped Wilkinson power divider. The use of CMOS active inductors to replace passive spiral inductors of RF power dividers was proposed by Lu and Wu in [28] to take the advantages of the high quality factor, low silicon consumption, and high self-resonant frequency of CMOS active inductors.

## 1.2 Spiral Inductors and Transformers

Monolithic on-chip inductors and transformers are also known as spiral inductors and transformers due to the way in which these inductors and transformers are laid out. Both planar and stacked spiral inductors and transformers have been developed and the detailed characterization and modeling of these inductors and transformers are available. Modern CAD tools for IC design are equipped with spiral inductors as standard elements in their component libraries.

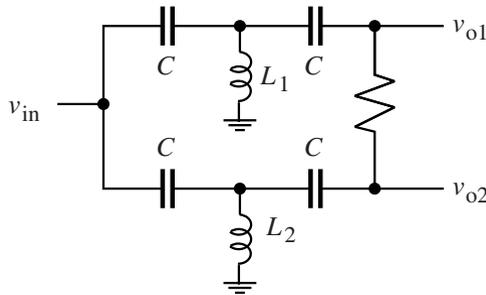


Figure 1.7. Equivalent circuit of lumped Wilkinson power divider.

### 1.2.1 Planar Spiral Inductors

Fig.1.8 is a sketch of square-shaped planar spiral inductors. The lumped equivalent circuit of spiral inductors is given in Fig.1.9, where  $L$  is the inductance of the spiral inductor,  $R_s$  represents the series resistance of the spiral caused by the skin-effect induced resistance in the spiral and the resistance induced by the eddy current in the substrate [29],  $C_s$  accounts for the capacitance due to the overlap of the spiral and the center-tap underpasses,  $C_{ox}$  denotes the capacitance between the spiral and the substrate,  $C_b$  and  $R_b$  quantify the capacitance and resistance of the substrate, respectively. Although modern CMOS technologies are equipped with multiple metal layers, typically only the top metal layer is used to construct planar spiral inductors and transformers such that the unwanted parasitic capacitance between the spiral and the substrate is minimized. As pointed out in [29], the substrate loss accounts for 10-30% reduction of the quality factor of the spiral inductors in low GHz ranges, mainly due to the penetration of the electric field generated by the spiral into the substrate. A main drawback of planar spiral inductors is their low inductance.

### 1.2.2 Stacked Spiral Inductors

The inductance of spiral inductors can be increased significantly using stacked configurations, as shown in Fig.1.10, however, at the price of an increased spiral-substrate capacitance because the lower metal layers are also used in the construction of the inductors [30]. The total inductance of a stacked inductor with two spiral layers is given by

$$L_{total} = L_1 + L_2 + 2M, \quad (1.4)$$

where  $L_1$  and  $L_2$  are the self-inductances of spirals 1 and 2, respectively, and  $M$  is the mutual inductance between the two spirals. Note the direction of the routing of the spirals in differential metal layers must be carefully

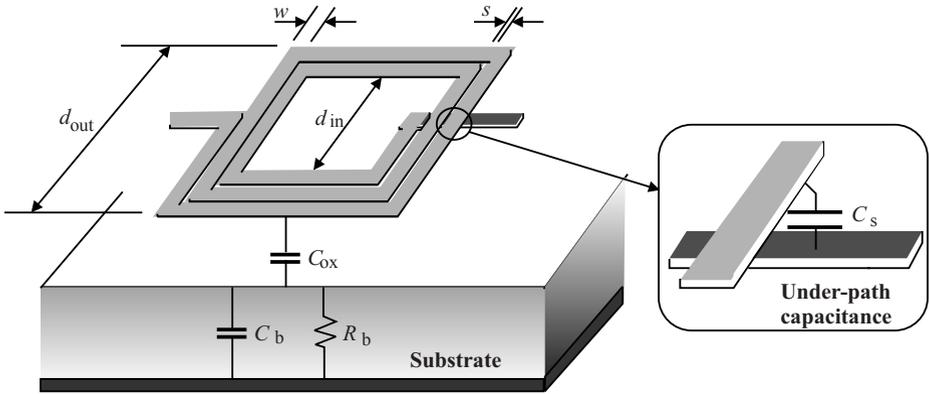


Figure 1.8. Square-shaped planar spiral inductors.  $w$  is the width of the spiral and  $s$  is the spacing between the turns of the spiral.

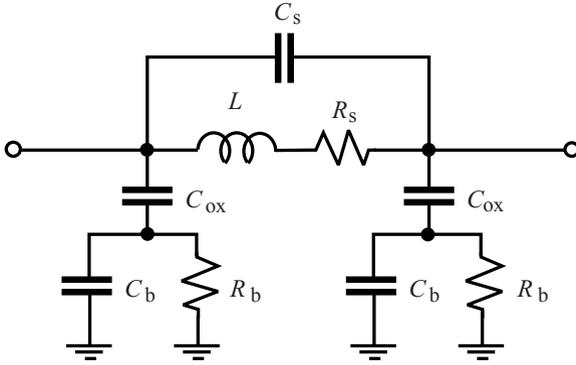


Figure 1.9. Lumped circuit model of planar spiral inductors.

chosen such that the total inductance increases. Figs.1.11 and 1.12 show the dependence of the measured inductance and self-resonant frequency of stacked inductors on the number of spiral layers [30]. It is seen that the inductance of stacked spiral inductors increases approximately linearly with the increase in the number of the spiral layers of the inductors. The self-resonant frequency of stacked inductors decreases with the increase in the number of spiral layers in a nonlinear fashion.

### 1.2.3 Spiral Transformers

To increase the inductance without significantly increasing silicon consumption, stacked spiral transformers and bilifar spiral transformers emerged. Transformers are essentially two spiral inductors coupled via a magnetic link.

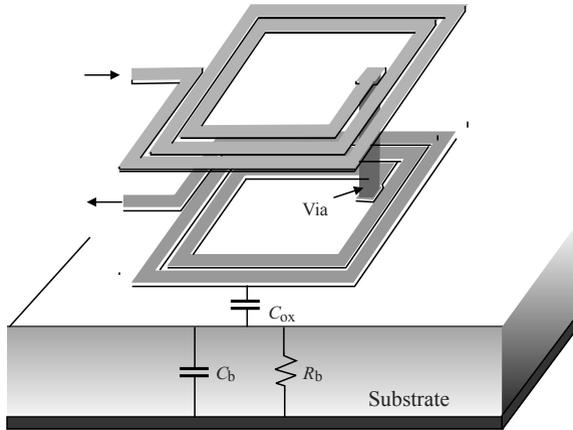


Figure 1.10. Square-shaped stacked spiral inductors.

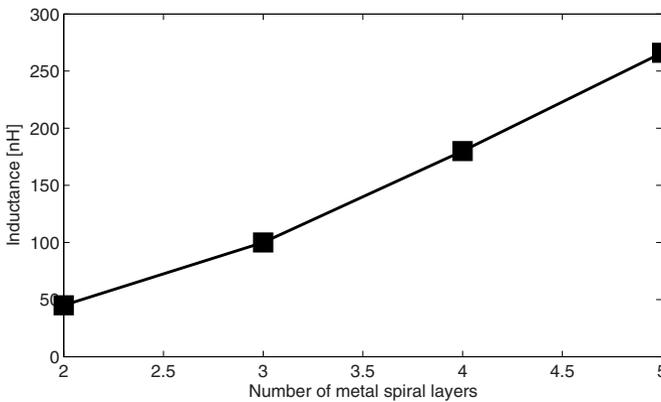


Figure 1.11. Dependence of the inductance of stacked spiral inductors on the number of spiral layers.

Fig.1.13 shows the lumped circuit model of bifilar spiral transformers [31], where  $C_{12}$  is the mutual capacitance between the primary and secondary windings, and  $k_{12}$ ,  $k_{21}$  are the coupling coefficients. All other parameters are the same as those in Fig.1.9.

## 1.2.4 Characteristics of Spiral Inductors and Transformers

Spiral inductors and transformers offer the key advantages of superior linearity and a low level of noise. The performance and applications of spiral inductors and transformers are affected by a number of drawbacks that are intrinsic to the physical geometry of these passive devices and CMOS tech-

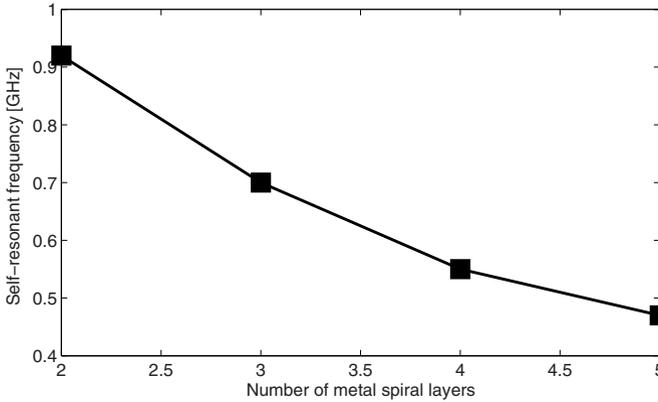


Figure 1.12. Dependence of the self-resonant frequency of stacked spiral inductors on the number of spiral layers.

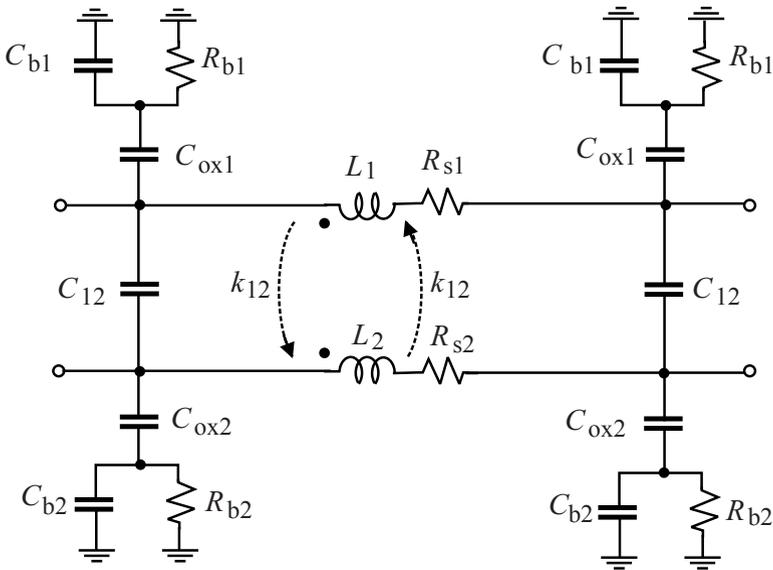


Figure 1.13. Lumped circuit model of spiral transformer.

nologies in which spiral inductors and transformers are implemented. These drawbacks include :

- *Low quality factor* - The quality factor of spiral inductors and transformers is limited by the ohmic loss of the spiral at high frequencies. Two sources that contribute to the ohmic loss of the spiral inductors and transformers exist : the skin-effect induced resistance of the spiral and the resistance

induced by the eddy currents in the substrate. The former is proportional to the square-root of the frequency of the signal flowing in the spiral whereas the latter is proportional to the square of the frequency of the signal flowing in the spiral. Because the resistance of the substrate in the lateral direction is much larger as compared with that in the vertical direction [32], the eddy currents in the lateral direction in the substrate are small. The substrate eddy-current induced resistance of the spiral is often negligible as compared with the resistance caused by the skin-effect [23]. The quality factor of spiral inductors in standard CMOS is typically below 20, as is evident in Table 1.3 where the parameters of some recently reported CMOS spiral inductors are tabulated.

- *Low self-resonant frequency* - The self-resonance of a spiral inductor is the resonance of the LC tank formed by the series inductance of the spiral inductor and the shunt capacitance between the spiral of the inductor and the substrate, as well as its underpass capacitance. The low self-resonant frequency of spiral inductors is mainly due to the large spiral-substrate capacitance, arising from the large metal area occupied by the spiral. The typical self-resonant frequency of spiral inductors is in the low GHz range, as is evident in Table 1.3.
- *Low and fixed inductance* - As pointed out earlier that the inductance of a planar spiral inductor is low and fixed once the number of the turns of the spiral is set. The only way to increase the inductance of the spiral inductor is to either increase the number of the turns of the spiral or use a stacked configuration where spirals on multiple metal layers are connected using vias. The former is at the expense of a large silicon area while the latter increases the spiral-substrate capacitance.
- *Large silicon area* - Due to the low inductance of spiral inductors, especially planar spiral inductors, and the fact that the inductance of these inductors is directly proportional to the number of the turns of the spiral of the inductors, the silicon area required for routing the spiral of the inductors is large. As an example, it was shown in [11] that a square-shaped spiral inductor of an inductance 8 nH will require 6 turns with  $d_{out} = 400\mu m$ . The actual silicon consumption of the inductor is larger than  $400 \times 400\mu m^2$  when design rules on the minimum spacings are followed. Moreover, the design rules of most IC foundries prohibit the placement of either active or passive devices in the region between the spiral of the inductors and the substrate, making spiral inductors the most silicon-consuming components.