Electrical Conductive Adhesives with Nanotechnologies

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Electrical Conductive Adhesives with Nanotechnologies

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Preface

With the phasing out of lead-bearing solders, electrically conductive adhesives (ECAs) have been identified as one of the environmentally friendly alternatives to tin/lead (Sn/Pb) solders in electronics packaging applications. In particular, with the requirements for fine-pitch and high-performance interconnects in advanced packaging, ECAs with nano-materials or other nano-technology are becoming more and more important due to the special electrical, mechanical, optical, magnetic, and chemical properties that nano-sized materials can possess. There has been extensive research for the last few years on materials and process improvement of ECAs, as well as on the advances of nanoconductive adhesives that contain nano-filler, such as nano-particles, nanowires, or carbon nanotubes and nano monolayer graphenes.

The objective of this book is to review the most recent advances of various types of electrically conductive adhesives with the particular emphasis on the emerging nanotechnology, including materials development and characterizations, processing optimization, reliability improvement, and future challenges/opportunities identification.

This book consists of nine Chapters, each representing a specific field of interest. Chapter 1 discusses an overview of electronic packaging and the evolvement of different types of conductive adhesives. Chapter 2 describes the latest development of nano-materials, nanotechnology and their applications in microelectronics packaging. Chapter 3 reviews the key polymeric materials used in conductive adhesives and the analytic approaches for ECA characterizations. Chapter 4 deals with the recent advances in materials, processes, and applications of isotropically conductive adhesives (ICAs), particularly focusing on the fundamental understanding and improvement of materials properties for ICAs and nano-ICAs. Chapter 5 discusses the recent development and applications of anisotropically conductive adhesives (ACA) with the emphasis on the nano-materials implementation for improved performance. Chapter 6 describes the latest materials and processing development of non-conductive adhesives (NCA). Chapter 7 discusses the details of conductive nano-inks and their applications in transparent electrodes, printed electronics, and other packaging areas. Chapter 8 focuses on the recent research and development of materials and applications of intrinsically conducting polymers. And finally, Chapter 9 summarizes the recent advances of conductive adhesives with nanotechnology and discusses the challenges and opportunities for continuing the work on nanoconductive adhesives.

The field of electrically conductive adhesives and nanotechnology is quite broad and their development is dynamic, so it is impossible to cover every aspect of them. We have attempted to include most major areas with the latest references which should be useful to our audience who work in this vast growing discipline. With the advances of microelectronics packaging and nanotechnology, there is always a constant need of improved materials and technology. This is a challenge that requires the continuous and active collaborative efforts between materials scientists, chemists, physicists, device and package design engineers.

We express our gratitude to many of our colleagues and friends in the field of microelectronics packaging, conductive adhesives and nanoscience and nanotechnology. Many of their published works have been cited in this book, including work published by many other experts in the fields. We would also like to thank Owen Hildreth and Angela Duan for proofreading some chapters and Steven Elliot and Andrew Leigh for editorial suggestions.

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Chapter 1
Introduction

1.1 Electronics Packaging and Interconnect

Integrated circuits (ICs) form the bases of all modern electronic products. However, an IC alone does not form a complete system and it must be integrated with other components into a system-level board. "Electronic Packaging" is defined as the bridge that interconnects the integrated circuits (ICs) and other components into a system-level board to form electronic products [1]. The packaging has four main functions: (1) signal distribution, mainly involving topological and electromagnetic considerations; (2) power distribution, involving electromagnetic, structural, and material aspects; (3) heat dissipation (thermal management), involving structural and material considerations; (4) and protection (mechanical, chemical, electromagnetic) of components and interconnections. Furthermore, design for x (where x stands for performance, environment, manufacturability, and reliability) at the front end and system test at the final stage prior to the system shipment are also important functions for electronic packaging. The challenge for the package is to provide all crucial functions required by the microelectronic system without limiting the performance of the individual part.

From the bare chip fabricated from the silicon wafer to the final product ready for use, the whole system can be divided into various levels of the packaging. The first-level packaging provides the interconnection between an IC and the package. At this level, the packaging acts as an IC "carrier." The IC carrier allows IC to be shipped after "burn-in" (an accelerated test with high bias, temperature, and other accelerated factors designed to wipe out those inferior components to reduce the infant mortality of the IC) and electrical test to be ready for assembly onto a system-level board by end product or contract manufacturers.

Due to the complexity of modern electronics packaging, there are many levels of interconnects with first-level interconnects defined as the connections between the IC and the IC carrier. Currently, two types of first-level interconnection dominate the industry: (1) wire bonding and (2) flip chip attachment.

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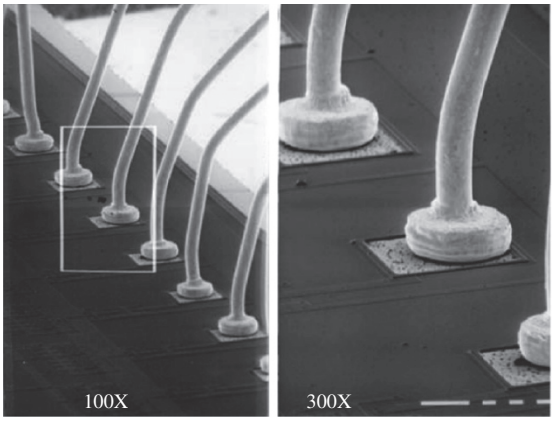
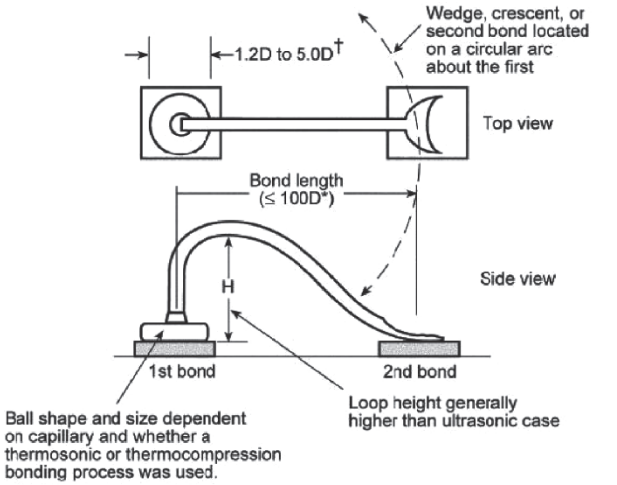
Many other interconnection methods exist to meet special needs or performance requirements. These range from tape automated bonding (TAB) which, at times, has seen significant usage within certain product lines to novel interconnection schemes, involving deposited thin films [2], compliant G-shaped springs [3], laser-deposited (written) conductors [4–6], copper pillar with solder cap [7–9], pure copper interconnect [10], and carbon nanotube (CNT)-based interconnect [11]. Pressure contacts using de-formable conducting polymers or elastomers have been used where the need to easily remove and replace the IC is a primary concern.

Wire bonding is the process of providing electrical connection between the silicon chip and the external leads of the semiconductor device using very fine bonding wires. The wire used in wire bonding is usually made either of gold (Au) or aluminum (Al). However, copper (Cu) wire bonding is starting to gain a foothold in the semiconductor manufacturing industry because Cu wire has a cost saving of more than 80% as compared to Au wire, higher thermal and electrical conductivity with lower power loss, and higher current flow as compared to Au wire which are important for enhanced device performance and reliability. There are two common wire bonding processes: Au ball bonding (Fig.1.1) and Al wedge bonding (Fig. 1.2) [12].



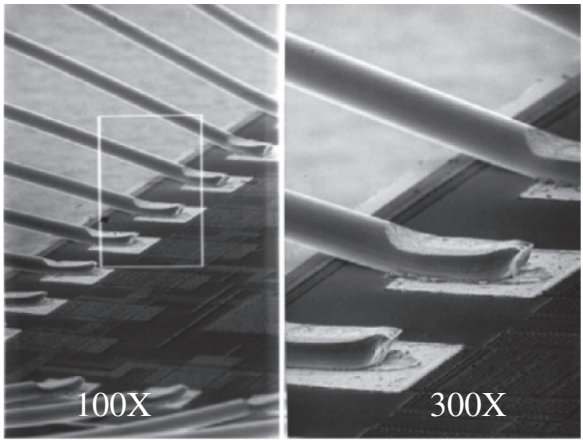
(a)

Fig. 1.1. Ball bonds (thermo-compression or thermosonic). (**a**) Scanning electron microscope photo micrograph of typical ball bonds and (**b**) schematic representation of ball bonds with important parameters indicated



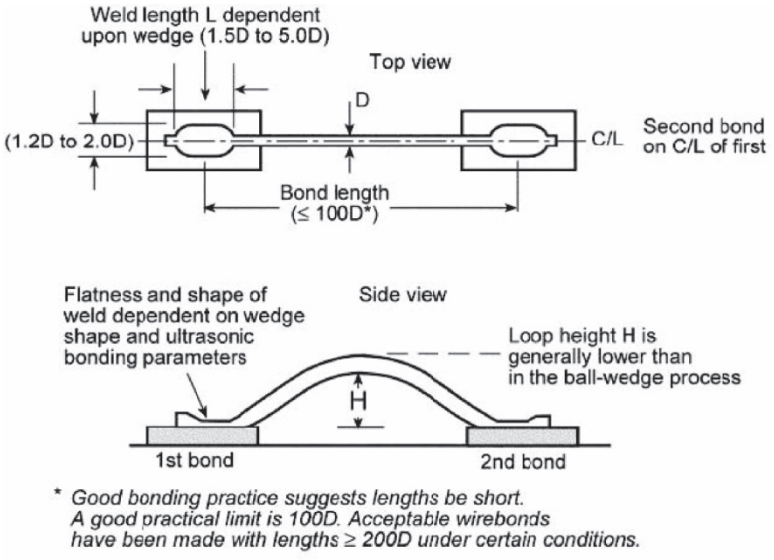
(b)

Fig. 1.1. (Continued)



(a)

Fig. 1.2. Ultrasonic bonds (wedge bonds). (**a**) Scanning electron microscope photo micrographs of typical ultrasonic wedge bonds and (**b**) schematic representation of ultrasonic bonds with important parameters indicated



(b)

Fig. 1.2. (Continued)

Gold ball bonding starts when a gold wire is fed through what is called a capillary. The capillary holds the gold wire as an electronic flame-off (EFO) is used to melt the end of the wire, forming a gold ball with a free-air ball diameter ranging from 1.5 to 2.5 times the wire diameter, with a typical wire diameter ~25–30 µm. Free air ball size consistency, controlled by the EFO and the tail length, is critical in good bonding. The free- air ball is then brought into contact with the bond pad. Adequate amounts of pressure, heat, and ultrasonic forces are then applied to the ball for a specific amount of time, forming the initial metallurgical weld between the ball and the bond pad as well as deforming the ball bond itself into its final shape. The wire is then run to the corresponding finger of the leadframe, forming a gradual arc or "loop" between the bond pad and the leadfinger. Pressure and ultrasonic forces are applied to the wire to form the second bond (known as a wedge bond, stitch bond, or fishtail bond), with the leadfinger. The wire bonding machine or wire bonder breaks the wire in preparation for the next wire bond cycle by clamping the wire and raising the capillary.

During aluminum wedge bonding, a clamped aluminum wire is brought in contact with the aluminum bond pad. Ultrasonic energy is then applied

to the wire for a specific duration while being held down by a specific amount of force, forming the first wedge bond between the wire and the bond pad. The wire is then run to the corresponding lead finger, against which it is again pressed, and a second bond formed by applying ultrasonic energy to the wire. The wire is then broken off by clamping and movement of the wire.

The gold ball bonding is non-directional and, as a result, is much faster than aluminum wedge bonding, which is why it is extensively used in plastic packaging. Unfortunately, gold ball bonding on Al bond pads cannot be used in hermetic packages, primarily because the high sealing temperatures (400–450° C) used for these packages tremendously accelerate the formation of Au–Al intermetallics, which can lead to early life failures. Gold ball bonding on gold bond pads, however, may be employed in hermetic packages.

Unlike Al–Al ultrasonic wedge bonding, Au–Al thermosonic ball bonding requires heat to facilitate the bonding process. The Al bond pad is harder than the Au ball bond, and it is impossible to make good bonding between them through purely ultrasonic without causing wire, bond pad, or silicon substrate damage. The application of thermal energy to the Al bond pads "softens" them, promoting the inter-diffusion of Au and Al atoms that ultimately form the Au–Al bond. Heat application also improves bonding by removing organic contaminants on the bond pad surface.

The tape automated bonding (TAB) technology is a usual microelectronic industrial process. TAB involves bonding a gold-bumped die to a leadframe circuit built on a flexible tape material, such as polyimide or polyester (Fig. 1.3). The TAB is used primarily in the flat panel display industry to mount driver chips between the glass of the display and the input circuitry behind the display, because of its low dimension interconnection. The flexible circuit using in TAB allows the package to be bent upward of 180°, allowing the circuit to be routed within the small confines of a flat panel display. It is also used in optical applications such as the sensors of stepper motors.

TAB is also utilized as a package format for Multi Chip Modules (MCM). In this format, the die and some of the leads are punched from the tape, the leads are formed, and then the package is mounted in a method similar to a J-Lead package. In some cases, the leads are not formed, but are soldered directly to the board.

TAB is typically a single-sided polyimide-based circuit, although a more expensive two-metal or four-metal tape is available. A copper metallization layer is bonded to the polyimide in one of two ways, either the copper is electrodeposited to the tape or an adhesive is used to bond rolled copper to the tape. Once the copper has been bonded to the polyimide the circuitry is imaged using a photolithography process, which allows for a

tight line pitch of up to 45 μm with a 22.5 μm lines and space widths. The tight pitch of TAB is very advantageous and allows for high-density circuits for high pin count devices.

There are two methods to achieve the connection between the die and the circuit. The first one is a single-point thermosonic bond. Single-point bonding requires each bond pad position to be individually bonded using heat, time, pressure, and ultrasonic applied to the TAB lead which is directly over its unique gold-bumped bond pad. This process does not require specific tools but on the other hand, it takes several times. The second one, the "Gang bonding," uses thermo-compression bonding to create a diffusion bond between all leads and bumps at the same time, all interconnections are performed in a one-step process-gang bonding. A specially designed tool bonds all the leads to the die using force, temperature, and time. It has the highest throughput. Then, the devices can be encapsulated, delivered in a reel-to-reel or singular format. Another advantage of this process is the minimized size of the circuits: the resulting height is the sum thickness of the die, the bumps, and the copper track.

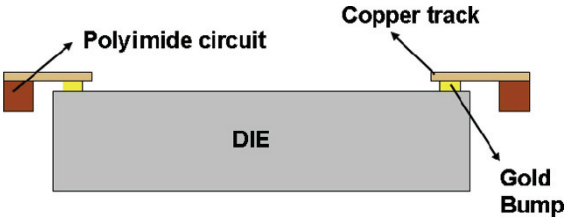


Fig. 1.3. A schematic of TAB interconnect

In contrast to wire bonding, in which the active silicon is "face-up," flip chip microelectronics assembly utilizes a different assembly method in which active silicon is flipped "face-down." With the active silicon face-down, electrical connections between the silicon and the substrate, circuit board, or carrier are made using conducive bumps on chip bond pads (Fig. 1.4) [12]. In contrast, wire bonding uses face-up chips with a wire connection to each pad. A comparison of wire bonding and flip chip is shown in Table 1.1. Flip chip components are predominantly semiconductor devices; however, components such as passive filters, detector arrays, and microelectromechanical system (MEMs) devices are also beginning to use flip chip bonding technologies.

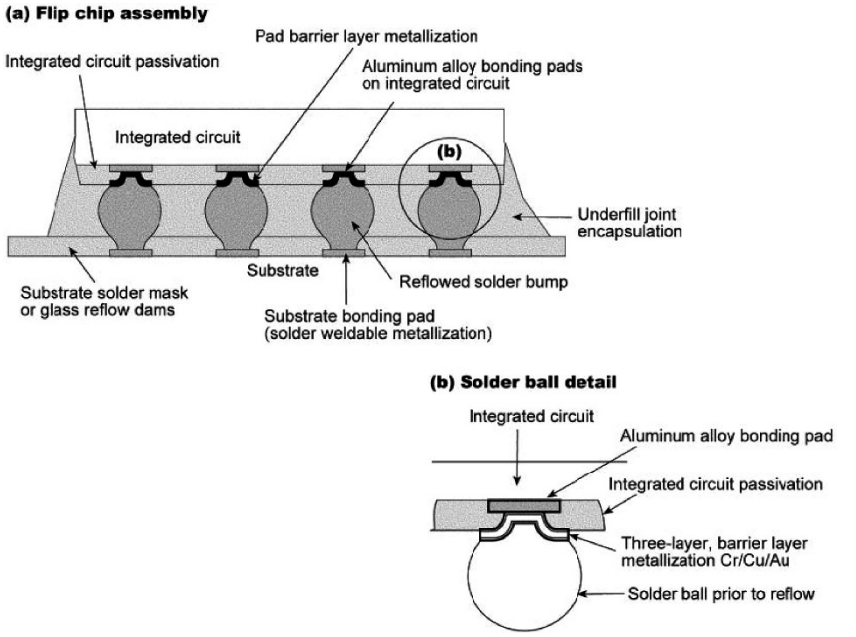


Fig. 1.4. Schematic representation of the flip chip bonding process. (**a**) Cross-section of a flip chip assembly and (**b**) detail of the solder ball and barrier layer metallization prior to reflow

Flip chip packaging has been widely adopted by the industry due to the technology's advantages in size, performance, flexibility, reliability, and cost over other packaging methods:

- *Smallest size* Eliminating packages and bond wires reduces the required board area by up to 95% and requires far less weight. Weight can be less than 5% of packaged device weight. Flip chip is the simplest minimal package, smaller than chip-scale packages (CSP) because of its chip size.
- *Highest performance* Flip chip offers the highest speed electrical performance of any assembly method. Eliminating bond wires reduces the delaying inductance and capacitance of the connection by a factor of 10 and shortens the path by a factor of 25–100. The result is high-speed off-chip interconnection.
- *Greatest I/O flexibility* Flip chip has the highest input/output connection flexibility of any interconnect technology. Wire bond connections are limited to the perimeter of the die, driving die sizes up as the number of connections increases, while flip chip connections can use the whole area of the die, accommodating many more connections on a smaller die. Area

connections also allow 3-D stacking of dies (via through silicon via [TSV], wire bonding, anisotropic conductive adhesive film (ACF) as well as flip chip interconnections) and other components.

- *Lowest cost* Flip chip can be the lowest cost interconnection for high-volume automated production as it can provide thousands of interconnection at once via a solder reflow process as such, costs below $0.01 per I/O connection. This explains flip chip's longevity in the cost-conscious automotive world, pervasiveness in low-cost consumer watches, and growing popularity in smart cards, RF-ID cards, cellular telephones, and other cost-dominated applications.

Early flip chip technologies used solder balls, or "bumps," to electrically connect the chip to the substrate. Even though materials other than solder balls have been developed, the term bump is still widely used by the industry; however, the primary functions of bumps remain the same. First, the bump provides the conductive path from chip to substrate. The bump also provides a thermally conductive path to carry heat from the chip to the substrate. In addition, the bump provides part of the mechanical mounting of the die to the substrate. Finally, the bump provides a spacer, preventing electrical contact between the chip and the substrate conductors, and acting as a short lead to relieve mechanical strain between board and substrate.

Flip chip packages can be classified into the following categories based on the processes for forming the bump and the interconnection between the die and the chip carrier:

- *Solder bump flip chip* The solder bumping process requires that an under-bump metallization (UBM) be placed on the chip bond pads by sputtering, plating, or other means. This UBM layer replaces the insulating aluminum oxide layer and also defines and limits the solder-wetted area. Solder is deposited over the UBM by evaporation, electroplating, screen printing solder paste, or needle depositing. After solder bumping, the wafer is sawn into individual chips called "bumped die." The bumped die is placed on the substrate pads, and the assembly is heated to make a solder connection.
- *Plated bump flip chip* Plated bump flip chip uses wet chemical processes to remove the aluminum oxide and plate conductive metal bumps onto the wafer bond pads. Plated nickel-gold bumps are formed on the semiconductor wafer by electroless nickel plating of the aluminum bond pads of the chips. After plating with the desired thickness of nickel, an immersion gold layer is added for protection, and the wafer is diced into bumped die. Plating copper bumps (posts) on wafers have also been demonstrated [13].

Attachment generally is by solder or adhesive, which may be applied to the bumps or the substrate bond pads by various techniques.

- *Stud bump flip chip* The gold stud bump flip chip process bumps die by a modified standard wire bonding technique. This technique makes a gold ball for wire bonding by melting the end of a gold wire to form a sphere. The gold ball is attached to the chip bond pad as the first part of a wire bond. To form gold bumps instead of wire bonds, wire bonders are modified to break off the wire after attaching the ball to the chip bond pad. The gold ball, or "stud bump" remaining on the bond pad, provides a permanent connection through the aluminum oxide to the underlying metal. The gold stud bump process is unique in being readily applied to individual single die or to wafers. Gold stud bump flip chips may be attached to the substrate bond pads with adhesive [14] or by thermosonic gold-to-gold connection. Die bumping and assembly services are available from several suppliers such as PacTech in Germany, Flip Chip International in USA.

- *Polymer bump flip chip* This adhesive bump flip chip process stencils a conductive adhesive to form bumps onto an under-bump metal [15–18]. Once cured, the adhesive acts as bumps and an additional attachment of conductive adhesive bonds the bumps to the mating chip or substrate. There are three stages in making flip chip assemblies: bumping the die or wafer, attaching the bumped die to the board or substrate, and, in most cases, filling the remaining space under the die with an electrically non-conductive "underfill" material.

Table 1.1. Comparison of wire bonding and flip chip interconnection factors [12]

Factor	Wire bond	Flip chip
Area	Requires space outside of chip perimeter for second bond	Within chip perimeter
Number I/O	Limited: 1–4 perimeter rows (100s–1,000s possible)	Full area array. Outperforms wire bonding even with a larger pitch (1,000s–10,000s possible)
Flexibility	Very flexible. Ability to shift I/O. Accommodate different die orientations, die sizes, package layout, etc. (within reason, of course)	None. Substrate pattern must match I/O pattern on chip. (Some self-aligning force.)
Electrical performance	Long round wires limits low loss frequency response to between 5 and10 GHz	Short , fat solder joint pillars allow low loss frequency response above 100 GHz
Cost	Typically \$0.0005–\$0.001 per interconnect with full automation	Ranges from \$0.01 to \$0.05 per interconnect [a]
Bonding time	Sequential (10–20 bonds/second)	Gang (all bonding at one reflow)
Bond type	Weld: Au–Al, Au–Au, Al–Al, Au–Cu,Cu–Cu	Solder : Sn63, Sn5, Sn10, Lead free (SnAg, SnAgCu,…)

Reliability	Monometallic systems, extremely reliable, flexible lead, eliminates or reduces any CTE issues. Bimetallic system could be susceptible to intermetallic growth and voiding	Solder fatigue a concern due to CTE mismatches. Typically requires underfill. Intermetallic growth and voiding problems with Sn and Cu
Environmental	Au, Al, environmentally friendly	Pb an environmental concern, hence lead-free alloys are used

[a] Includes extra cost for custom under-bump metallurgy and a penalty for substrate repatterning if the die shrink or pin out changes could be accommodated by the wire bond technology without changing the substrate pattern

Second-level packaging provides the interconnection between the interposer and substrate to either a printed wiring board (PWB) or a card. This interconnection can be realized by through-hole (TH) technology, surface mount technology (SMT) including dual-in-line, quad-in-line, ball grid array (BGA), and chip-scale package (CSP). Traditional through-hole dual in-line package (DIP) assemblies reached their limits in terms of improvements in cost, weight, volume, and reliability at approximately 68 leads. SMT allows production of more reliable assemblies with higher I/O, increased board density, and reduced weight, volume, and cost.

Third-level packaging mainly is the process to put second-level packages (i.e., FR 4 motherboard) onto a backplane. With the requirements toward low cost, miniaturization, and high performance for the current semiconductor devices, the bare IC chips can also be connected to the integrated board using flip chip technology directly [19], which is called flip chip on board (FCOB) or direct chip attach (DCA). The advantage is to eliminate the first-level package (chip to package), reduce assembly cost, and enhance performance.

The packaging concepts and technologies at all packaging levels are under quick evolution because of the dramatic changes in the computer, telecommunications, automotive, and consumer electronics industries to low cost, portability, high performance, diverse functions, and environment- and user-friendliness. Figure 1.5 illustrates the historical evolution of packaging [20]. Packages have evolved from traditional DIP (dual-in-line packages), quad flat packages (QFP) to area array flip chip, and BGA (ball grid array) packages. The silicon efficiency in the package has increased to almost 100% with the following CSP (chip-scale packages) and now in excess of 100% silicon efficiency by stacking those thin dies in three-dimensional stacked packages. In order to increase the efficiency of packaging, there is a paradigm shift to wafer level packaging (WLP) and through silicon vias (TSVs). WLP is a packaging technology where most or all of the IC packaging process steps are carried out at the wafer level. TSV technology enables the chips (or wafers) to be stacked vertically, thus reducing the wiring length to the thickness of the die. Memory dies can be stacked right on top of the processor die to provide high-speed and

low-loss memory–processor interfaces due to the lower parasitics of the TSV vertical interconnections. TSVs can be developed in an area array format thereby increasing the vertical interconnection density. They can also be used for heterogeneous integration of different IC technologies.

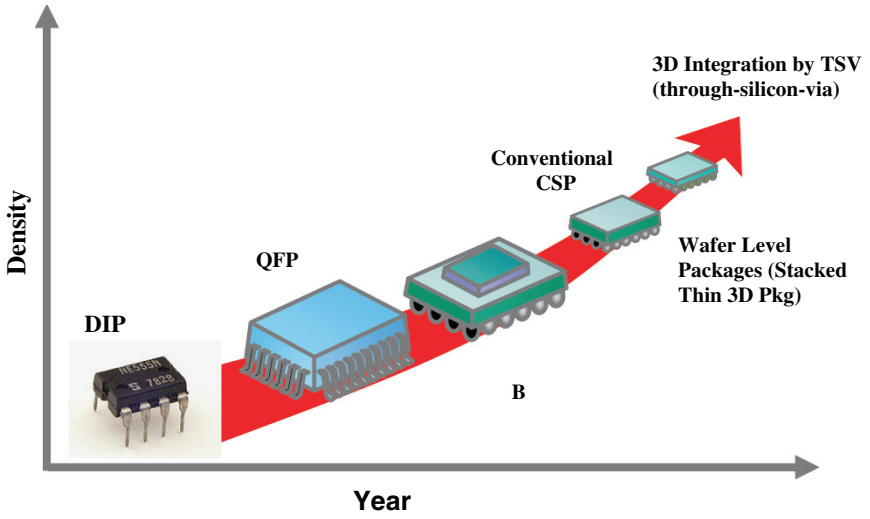


Fig. 1.5. Electronics packaging evolution

1.2 Interconnection Materials

Different levels of packaging are connected through interconnect materials. The primary purpose of interconnect materials is to electrically connect components for power, ground, and signal transmissions, with lead-containing solder alloys, especially eutectic tin/lead (Sn/Pb), has been the de facto interconnect material in most areas of electronic packaging. Such interconnection technologies include pin through hole (PTH), surface mount technology (SMT), ball grid array (BGA) package, chip-scale package (CSP), and flip chip technology [21]. Figure 1.6 shows an example of a functional surface mount component attached to a substrate via interconnect materials.

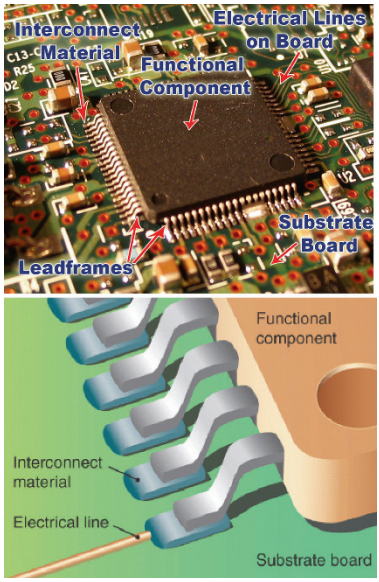


Fig. 1.6. (*Top*) Photo of a functional component that is assembled on the board substrate via interconnects. (*Bottom*) side view of the bonding between the component and the substrate via the interconnect material

1.2.1 Lead-Free Interconnect Materials

There are increasing concerns with the use of tin–lead alloy solders because the lead contained in these solders is a material hazardous to both humans and environment. Each year, thousands of tons of lead are incorporated into thousands of products with consumer products consuming the bulk of the lead. Many of these products such as cell phones, pagers, electronic toys, personal digital assistants tend to have a short life cycle on the order of 2–3 years and millions of lead-containing products simply end up in landfills. According to 2001 US Geological Survey, the total lead consumption by the US industries in 2000 was 52,400 metric tons. More than 10% of the lead, 5,430 metric tons, was used to produce alloy solders. Recycling of lead-containing consumer electronic products has proven to be very difficult, although in Japan, legislation prohibiting lead disposal in landfills and other waste disposal sites is already in place. The electronic industry is moving toward green manufacturing as a global trend. In the area of soldering, mainly driven by European RoHS (Reduction of Hazardous Substances), lead was banned effective July 1,

2006, except in some exempt items. This European legislation is followed by China RoHS which has similar list of banned materials, and its phase 1 implementation was effective March 1, 2007. In Japan, the legislative activities deal with the reclamation and recycling of electronics. The Home Electronics recycling law came into force on April 1, 2001, and applied only to TVs, refrigerators, and similar items. Although not specifically aiming at lead, this legislation effectively drove Japanese industry toward lead-free soldering process. Those legislation activities lead the trend which effectively drives the rest of the world toward lead-free soldering (see Fig. 1.7).

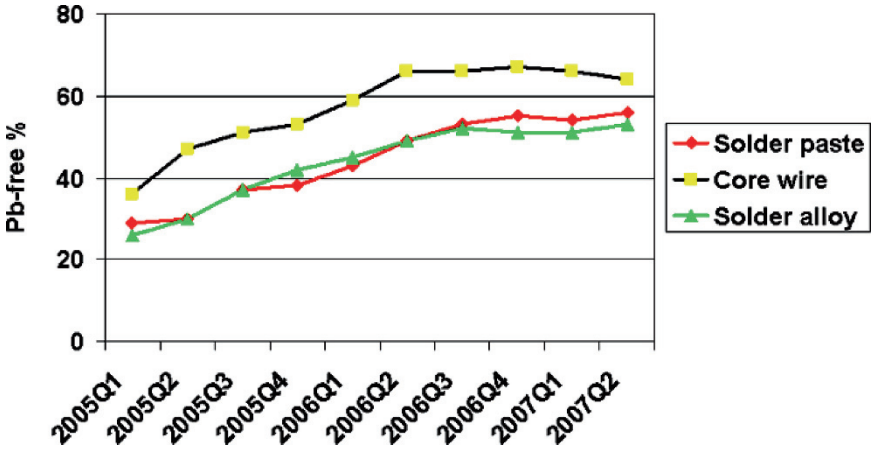


Fig. 1.7. Lead-free soldering implementation status reported by IPC [22]

The main requirements for an alternative solder alloy are the following:

1. Low melting point: The melting point should be low enough to avoid thermal damage to the assembly and high enough for the solder joint to bear the operating temperatures. The solder should retain adequate mechanical properties at these temperatures.
2. Wettability: The bond between the solder and the base metal is formed only when the solder wets the base metal properly. A high Sn content ensures this and thus forms a strong bond.
3. Availability: There should be adequate supplies or reserves available of candidate metals. Tin (Sn), zinc (Zn), copper (Cu), and antimony (Sb) are available whereas there is limited supply of indium (In).
4. Cost: Manufacturers of electronic systems are unlikely to change to an alternative solder with an increased cost unless it has demonstrated better properties or there is legislative pressure to do so.

There are strict performance requirements for solder alloys used in microelectronics. In general, the solder alloy must meet the expected levels of reliability, as well as electrical and mechanical performance [23–27].

Ever since the commencement of the research and development of Pb-free solder alloys, a large number of Pb-free solder alloys have been proposed and studied. Among the numerous lead-free solder options available, Fig. 1.8 shows the families which are of particular interest and the prevailing choices of industry: eutectic SnAg, eutectic SnCu, eutectic SnAgCu, eutectic SnZn, eutectic BiSn, along with their modifications. Also shown in Fig. 1.8 are the related applications including reflow soldering, wave soldering, and hand soldering. SnAgCu alloys are the prevailing choices, with SnCu(+Y), SnAg(+Y), and BiSn(+Y) families, where Y represents minor additive elements, also being adopted. The soldering processing window is narrower than that of eutectic tin–lead, also called Sn63 mainly due to the elevated melting temperature of SnAgCu solder and the limited high-temperature tolerance of components and board. The high surface tension of Sn aggravates the difficulty in wetting, while the high reactivity of Sn adds additional constraints to control the contact time between molten solder and base metal or solder container. Compared to Sn63, the creep rate of SnAgCu is slower at low stress, but faster at high stress. This results in a longer temperature cycling life at low joint strain applications, but a shorter cycling life at high joint strain applications. Higher Cu content stabilizes intermetallic compound (IMC) structure at interface between SnAgCu solder and NiAu bond pads. The high rigidity of SnAgCu solders enhances the fragility of joints, although significant improvement has been accomplished via low Ag or high Cu content or doping approaches [10].

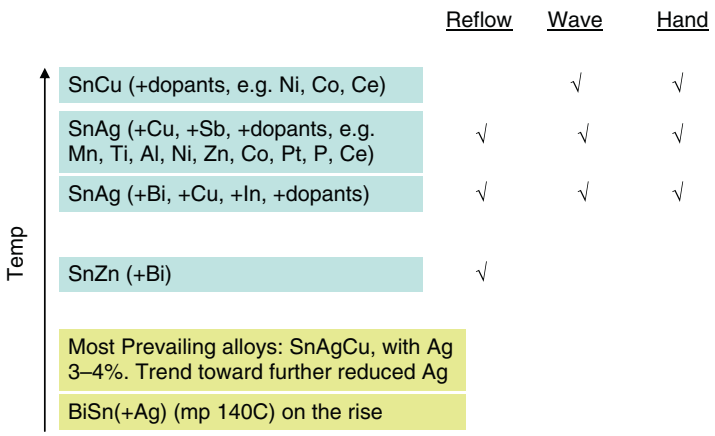


Fig. 1.8. Prevailing lead-free solder alloys and their applications [10]

Electronic devices such as notebook computers and cellular phones are required to be thin and small with complicated functions. The electronic industry has been coping with these changes, providing the necessary miniaturization of these electronic devices, and has been able to meet the required reliability. To support these changes, the interconnections provided by solder joints have become finer and finer in pitch size, and yet the reliability is maintained.

To meet the present and future strength requirements, higher strength solder alloys may be required. It is believed that composite solders would provide reinforcements to the otherwise weak solder, and researchers have been working on their development, beginning with the SnPb alloys [28–34]. These composite solders have been found to have good reliability because the reinforcing particles can suppress grain-boundary sliding, intermetallic compound (IMC) formation, grain growth, and furthermore, redistribute stress uniformly. In Pb-free composite solders, the reinforcements can be intermetallic powders of Cu_5Sn_5, Ag_3Sn or NiTi, carbon fibers, or fine oxide particles of metals such as Ni, Cu, and Ag [35–40]. Composite solder alloy development activities so far have mainly been aiming to achieve suitable physical properties and better service performance.

1.2.2 Electrically Conductive Adhesives

Other than lead-free solders, another lead-free interconnect material is electrically conductive adhesives (ECAs). ECAs mainly consist of an organic/polymeric binder matrices and conductive metal fillers. The conductive fillers provide the electrical properties and the polymeric matrices provide the physical and mechanical properties. Compared to the solder technology, ECAs offer numerous advantages such as environmental friendliness from the elimination of lead usage and flux cleaning, mild processing conditions, fewer processing steps which reduce processing cost, and finally, an increase in fine-pitch capability due to the availability of small-sized conductive fillers. There are two types of ECAs: isotropically conductive adhesives (ICAs) which are conductive equally in all directions and anisotropically conductive adhesives (ACAs) which are only conductive in one direction, typically along the *z*-axis. Figure 1.9 compares chip-to-substrate interconnects with solder joints and different ECA joints. However, like all lead-free materials, currently commercialized ECAs still have some material property limitations and challenges, including lower electrical and thermal conductivity compared to solder interconnects materials, contact resistance fatigue in reliability tests, limited current-carrying capability, metal migration fatigue in reliability and high voltage tests, and poor impact strength [40–42].

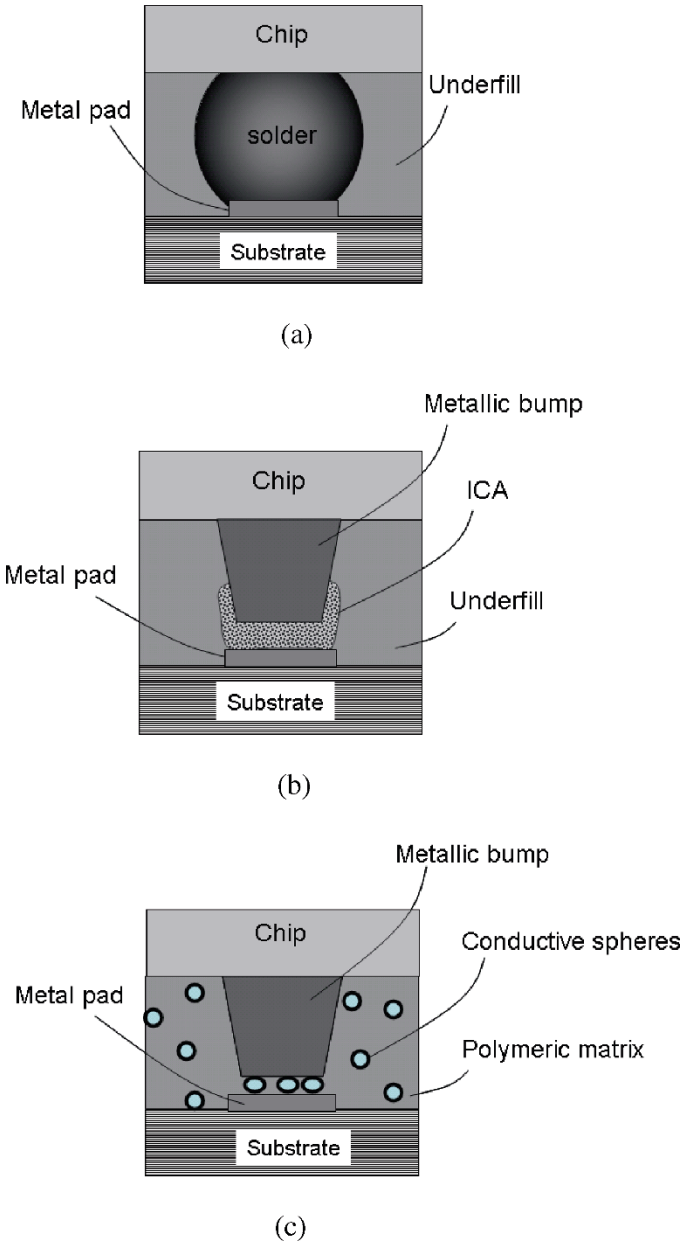


Fig. 1.9. Comparison of various types of interconnect approaches. (**a**) Solder interconnect, (**b**) isotropically conductive adhesive (ICA) interconnect, and (**c**) anisotropically conductive adhesive (ACA) interconnect

1.2.2.1 Electrically Conductive Adhesives (ECA) categories

ICAs and ACAs generally contain different types of conductive fillers and filler loadings are different too. ICAs typically are filled with 1–10 μm-sized Ag flakes and ACAs typically contain 3–5 μm-sized conductive fillers which usually are spherical in shape. Non-conductive adhesives (NCAs, typically without conductive fillers) have also become quite popular for some applications. The difference between ICA and ACA/NCA is based on the percolation theory as shown in Fig. 1.10. The percolation threshold (Pc) depends on the shape and size of the fillers, but typically in the order of 15–25% volume fraction. For ICA, the loading level of conductive fillers exceeds the percolation threshold, providing electrical conductivity in all *x*, *y*, and *z* directions. For ACAs or NCAs, the electrical conductivity is provided only in *z*-direction between the electrodes of the assembly. Figure 1.11 shows the schematics of the interconnect structures and typical cross-sectional images of flip chip joints by ICA, ACA, and NCA materials illustrating the bonding mechanism for all three adhesives.

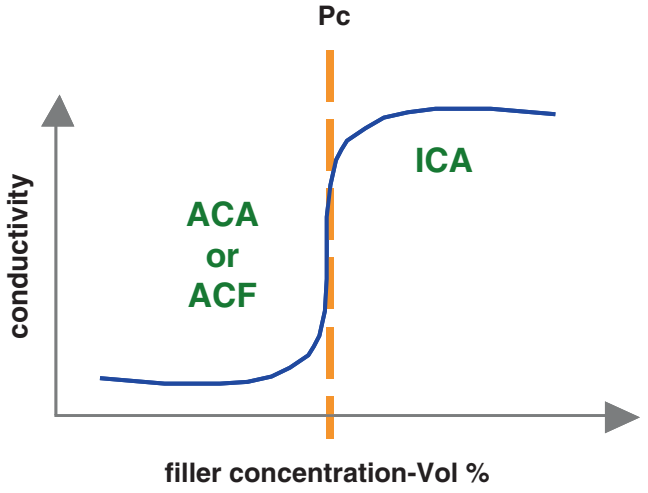


Fig. 1.10. Typical percolation curve of conductive adhesives (*P*c is the percolation threshold)

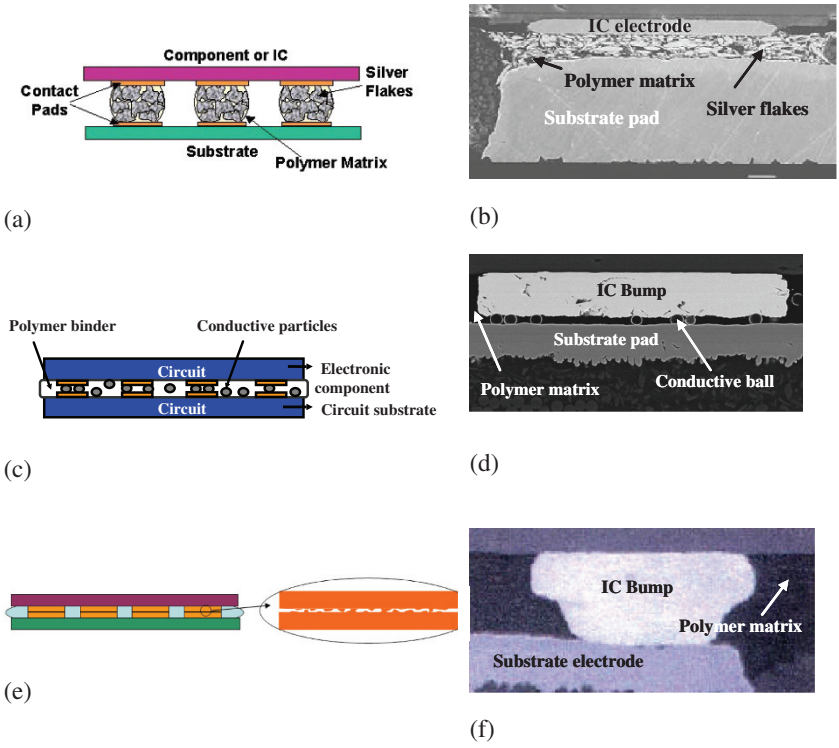


Fig. 1.11. Schematic illustrations and cross-sectional views of (**a**), (**b**) ICA, (**c**), (**d**) ACA, and (**e**), (**f**) NCA flip chip bonding

Isotropic conductive adhesives are composites of polymer resin and conductive fillers. The adhesive matrix is used to form an electrical and mechanical bond at the interconnects. With increasing filler concentrations, the electrical properties of an ICA transform it from an insulator to a conductor. ICAs have been used in the electronic packaging industry primarily as die attach adhesives [43–45]. Recently, ICAs have been proposed as an alternative to tin/lead solders in surface mount technology (SMT) [46], flip chip, and other applications.

Anisotropic conductive adhesives (ACAs) or anisotropic conductive films (ACFs) provide unidirectional electrical conductivity in the vertical or *Z*-axis. This directional conductivity is achieved by using a relatively low volume loading of conductive filler (5–20 volume percent). The low volume loading is insufficient for inter-particle contact and prevents conductivity in the *X*–*Y* plane of the adhesive. The *Z*-axis adhesive, in film or paste form, is interposed

between the surfaces to be connected. Heat and pressure are applied simultaneously to this stack-up until the particles bridge the two conductor surfaces. Recently, anisotropic conductive adhesives/films (ACAs/ACFs) are becoming popular as one of promising candidates for lead-free interconnection solutions in microelectronic packaging application due to their technical advantages such as fine-pitch capability below 40 μm, low-temperature processing ability, low cost, and environmentally friendly materials and processing. ACAs/ACFs consist of conducting particles (typically 5 ~ 10 μm in diameter) and polymer matrix that provides both attachment and electrical interconnection between electrodes [47–49]. In particular, ACFs are widely used for high-density interconnection between liquid- crystal display (LCD) panels and tape carrier packages (TCPs) to replace the traditional soldering or rubber connectors. In LCD applications, traditional soldering may not be as effective as ACFs in interconnecting materials between indium tin oxide (ITO) electrodes and TCP. ACFs have also been used as an alternative to soldering for interconnecting TCP input lead bonding to printed- circuit boards (PCBs).

1.2.2.2 Nanoelectrically Conductive Adhesives

To meet the requirements for future fine pitch and high-performance interconnects in advanced packaging, ECAs with nanomaterials or other nano-technologies are attracting more and more interest due to the special electrical, mechanical, optical, magnetic, and chemical properties that nano-sized materials can possess. There has been extensive research on nanoconductive adhesives that contain nano-filles, such as nanoparticles, nanowires, or carbon nanotubes, and nano monolayer graphenes.

A detailed review of ICAs, ACAs/ACFs, and nano-ECA will be covered in other chapters in this book.

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