METHODOLOGY FOR THE DIGITAL CALIBRATION OF ANALOG CIRCUITS AND SYSTEMS

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with Case Studies

by

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Introduction

1 CONTEXT

Ever since the invention of the transistor in the late 50's, its fabrication technology has been evolving, allowing the device integration in a continuously shrinking area. High-performance integrated analog systems have always been difficult to design. Sometimes, calibration is used to gather the extra performance that the analog devices cannot provide intrinsically. But the evolution of the manufacturing technology renders even basic analog systems difficult to design today. With the size reduction, the intrinsic precision of the components degrades. In parallel, the supply voltage decreases, limiting the topologies which can be used. Many modern technologies are specifically suited for pure digital circuits, and some analog devices, like capacitors, are not available. In these conditions, analog design is a challenge even for experienced designers.

To relieve the extreme design constraints in analog circuits, digital calibration becomes a must. It allows a low-precision component to be used in high-performance systems. If the calibration is repeated, it can even cancel the effect of temperature drift and ageing.

The digital calibration is compatible with the evolution of fabrication technologies, which ever more facilitates the integration of digital solutions at the cost of a dramatic reduction of analog performances. Thanks to the reduction of the size of digital devices, even complex digital calibration solutions can be integrated and become a viable alternative to intrinsically precise analog designs.

Digital calibration allows to realize high-performance analog systems with modern technologies. This enables pure analog designs to be implemented even in fully digital processes. In existing mixed-signal designs, the full system realization also becomes possible with technologies providing higher integration density. Finally, because circuit performances rely on digital calibration, retargeting is simplified. The digital blocks can be synthesized automatically, whereas only a limited design effort is invested in the analog circuit.

2 OBJECTIVES

The first objective of this book is to provide a general methodology for the digital calibration of analog circuits. It ranges from the analog circuit analysis (to identify how imperfections are detected) to the implementation of the compensation. It presents systematic means for performing the compensation based on general correction blocks and algorithms. The opportunity of performing regular calibration is also analyzed, and a classification of analog systems allowing or disallowing this feature is developed. Finally, simulation tools permitting the verification of the efficiency of the calibration are presented.

The second objective is to use the defined methodology for correcting the imperfections of existing circuits. In this book, the application of the compensation technique and circuits to three different systems is proposed: a high-precision digital-to-analog converter, a SOI (silicon on insulator) 1T DRAM (single-transistor dynamic random access memory), and a Hall sensor-based microsystem for current measurement.

3 COMPENSATION METHODOLOGY

The compensation methodology is based on current-mode sub-binary radix converters used in conjunction with successive approximations algorithms. A complete analysis of an efficient implementation of sub-binary converters using MOS transistors is performed. In particular, it is demonstrated that these very low-area $M/2^{+}M$ converters can achieve arbitrarily high resolutions, which is advantageous to perform high-precision calibrations.

An adaptation of the compensation methodology to continuous-time processing systems is also studied. In particular, a way of using an adapted successive approximations algorithm and compensation converter which produce unity up and down compensation steps is presented.

4 APPLICATIONS OF THE COMPENSATION METHODOLOGY

The sub-binary converters are intrinsically non-linear and their direct use as conventional digital-to-analog converters is impossible. However, using two special calibration and radix conversion algorithms, this limitation is

removed and the realization of high-precision DACs becomes possible, even with very low-precision components used in sub-binary converters.

The second application is a SOI 1T DRAM, for which an automatic reference calibration technique is proposed. Using the proposed compensation methodology, a sub-binary DAC controlled by a successive approximations algorithm generates the current reference necessary to read the memory. The reference compensates various circuit imperfections together, from the sense amplifier offset to the statistical dispersion of the memory cell currents.

The most important application of the digital compensation methodology is a current measurement microsystem based on a Hall sensor. Until now, the performances of current measurement ASICs have been highly limited by the sensitivity drift of integrated Hall sensors. A novel continuous sensitivity calibration technique is proposed, based on the digital compensation methodology. It combines chopper and autozero techniques, along with all the circuits and algorithms proposed in the first part for the general correction methodology.

5 BOOK ORGANIZATION

Chapter 2 is an introduction to common compensation techniques. The chopper and autozero techniques are presented, and the conditions of their use in continuous and sampled systems is discussed. Finally, both techniques are compared and a classification is performed.

Chapter 3 presents the digital compensation algorithm (successive approximations), and the current-mode sub-binary $M/2^{+}M$ digital-to-analog converters which are especially well-suited for digital compensation by current injection. Other sub-binary structures are also presented and compared. Finally, the special calibration and radix conversion algorithms, allowing the use of sub-binary converters as conventional DACs, are presented.

Chapter 4 proposes a complete digital compensation methology which allows the correction of circuit imperfections using the circuits and algorithms of chapter 2. The presentation includes specific simulation tools for automatic digital compensation. The application of the methodology to the SOI 1T DRAM reference calibration is presented.

Chapter 5 introduces a new sensitivity calibration technique for Hall microsystems, based on the methodology and circuits of chapters 3 and 4. After an introduction to Hall sensors and the state of the art in Hall sensor-based microsystems, the principle of the calibration technique is explained. The system-level issues are presented and the solutions explained.

Chapter 6 details the implementation of a complete Hall microsystem for current measurement using the sensitivity calibration technique proposed in chapter 5. Each block is presented, and the simulated and measured performances discussed.

Chapter 7 concludes this book by highlighting the most important results and proposing future improvement possibilities.

Chapter 2

Autocalibration and compensation techniques

This chapter presents techniques which are commonly used to compensate or hide imperfections of analog circuits. Some of them, like chopper modulation, use mostly analog circuitry to remove a disturbing effect. Others, like successive approximations, extensively use digital correction algorithms to trim analog components or circuits. First, the mostly used techniques are presented. Then, their performances are examined and a classification is made.

1 INTRODUCTION

The design of analog circuits is rendered difficult by the imperfections imparted by the manufacturing process to the component values. Physical parameters (e.g. oxide thickness, physical dimensions, doping profile) are subject to variations due to instabilities of the fabrication technology, and they reflect on component parameters. The best achievable tolerance of individual component values thus depends on the accuracy of the manufacturing process, and cannot be reduced below a minimum level.

Fortunately, analog design rarely relies on the *absolute value* of single components, but rather on *relative values* of several components. The relative values can be made arbitrarily close, i.e. with small tolerances, by using appropriate design techniques like matching. Thus, high-precision circuits can be realized even with poor manufacturing processes.

2 MATCHING

The most common technique for improving the precision of analog blocks is matching. If the layout of pairs/sets of components is performed carefully following the rules presented below, the statistical dispersion of their values can be reduced.

2.1 Matching rules

The following rules should be applied for optimum matching of integrated components [1]:

1. Same structure
2. Same temperature
3. Same shape, same size
4. Minimum distance
5. Common-centroid geometries
6. Same orientation
7. Same surroundings
8. Non minimum size

When designing pairs/sets of components using these rules, one makes them all as similar as possible. Furthermore, as the components are split and mixed appropriately (common-centroid), they are statistically affected in a similar manner by external (e.g. temperature) and intrinsic (e.g. doping) parameter variations.

2.2 Matching parameters

If the rules presented in section 2.1 are correctly applied, the dispersion of the component values becomes an inverse function of the *area* occupied by the devices [2][3][4]. This means that by increasing the size of the features and by applying rigorously the matching rules, the relative mismatch of the device pairs/sets is reduced. The general model that describes the dependence of the matching of a parameter P on the area of two devices with area $W \cdot L$ is:

$$\sigma^2(P) = \frac{A_P^2}{W \cdot L} \tag{2.1}$$

where A_P is the process-dependent matching parameter describing the area dependence. This model is applicable to capacitors, resistors, MOS transistors, etc.

The statistical dispersion is inversely proportional to the area of the device. Consequently, in order to achieve a given matching precision, one has to design components larger than the limit that is calculated using equation 2.1. Obviously, the designer faces an important trade-off between precision and circuit area when using only matching properties. But there are also other

techniques that allow for increasing the precision of poor circuit elements. Instead of focusing on building high-precision devices, one can build low-precision components and try to *adjust* them or *compensate* for their imperfections later on. There are wide varieties of such techniques, each one having its specific application fields. The new trade-off is then between the matching effort and the use of one or a combination of these compensation techniques. This chapter presents some of them, focusing on the additional circuitry needed to implement them and on the alternative design choices.

3 CHOPPER STABILIZATION

Many imperfections of operational amplifiers, e.g. 1/f noise and offset, are low-frequency or even DC. The idea of chopper stabilization [5][6] is to transpose the signal to a higher frequency where the effect of 1/f noise (and offset) is negligible, to amplify the modulated signal, and finally to demodulate the amplified signal back to the baseband.

3.1 Principle

Figure 1 presents a functional schematic of a chopper amplifier.

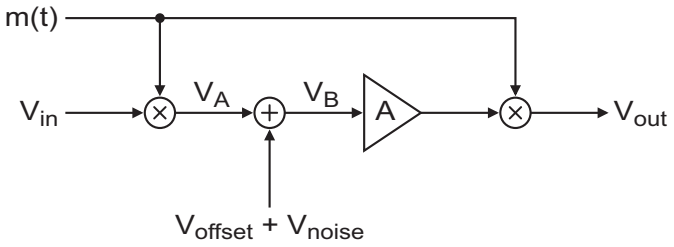

Figure 1. Functional chopper amplifier

A modulation signal m(t) periodically changes the polarity of the input signal V_{in}. The amplifier block A is ideal, having an infinite bandwidth and neither offset nor noise. However, an equivalent input offset V_{offset} and noise V_{noise} are added to the input V_A of the amplifier, generating an equivalent imperfect input signal V_B for the ideal amplifier. The amplified signal is demodulated by sign changes using the same signal as for input modulation, resulting in the system output V_{out}.

3.2 Analysis

Figure 2 presents an analysis of this chopper amplifier in the time domain, whereas figure 3 displays the frequency analysis.

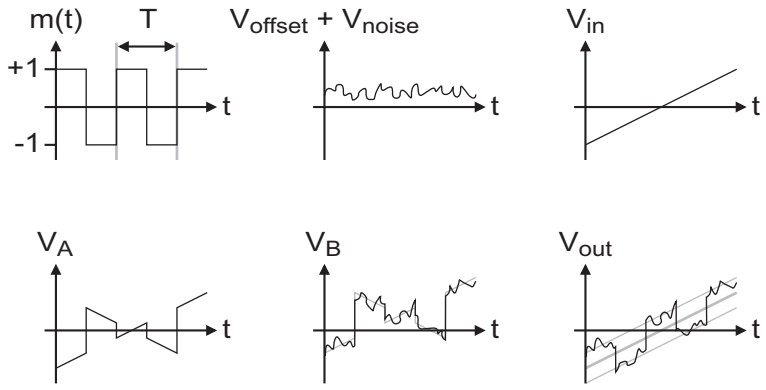

Figure 2. Temporal analysis of a chopper amplifier

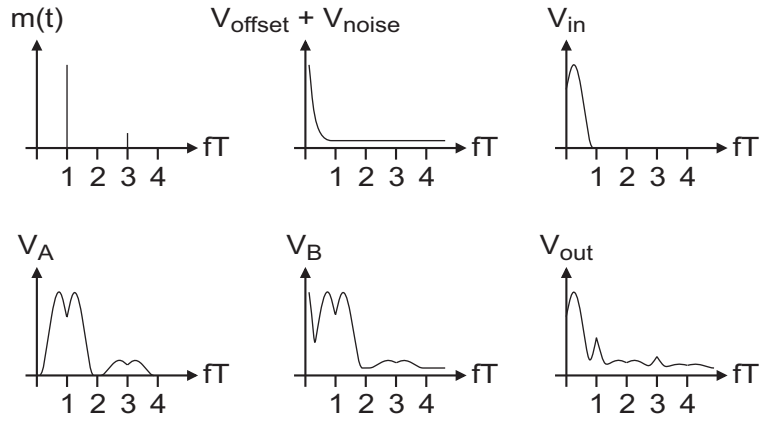

Figure 3. Frequency analysis of a chopper amplifier

In this functional system, the modulation signal m(t) is a square wave with a period T that is applied to both the modulator and demodulator. V_{in} is a band limited signal with frequency components up to at maximum 1/T. If this is not the case, the higher frequencies are aliased in the baseband, which is undesirable.

The modulation changes the sign of the amplifier input periodically, which corresponds in the frequency domain to a shift of the spectrum to the odd har-

monics of the modulation signal. This point is the key of the performances of a chopper amplifier. Indeed, the imperfections that are added to the shifted spectrum have important low-frequency components (offset and 1/f noise), whereas they are significantly lower at the frequencies where the signal is shifted. Ideally, the chopper frequency is chosen to be higher than the corner frequency of the 1/f noise in order to add only white noise to the signal.

Once the signal V_B is amplified, it is brought back to the baseband by the demodulator, which effectuates exactly the same operation as the input modulator. The effect is to shift the signal back around DC and even multiples of the chopper frequency, whereas the 1/f noise and offset are located at the odd harmonics. In the time domain, this signifies that the mean value is the amplified signal, whereas the modulated component is the offset.

Obviously, the output signal V_{out} cannot be exploited as is. The signal is correctly present in the baseband, but the higher frequency components should be removed. For this reason, the output of chopper amplifiers is usually low-pass filtered by an additional stage.

3.3 Implementation

To simplify the realization of a chopper amplifier, it is advantageous to use differential inputs and outputs for the amplifier. Indeed, since the inputs and the outputs of the amplifier are differential, changing their polarity is done simply by crossing the positive and negative lines. Such a fully-differential system is presented in figure 4.

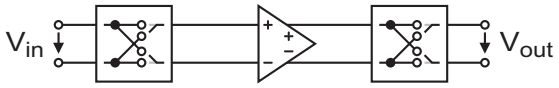

Figure 4. Fully differential chopper amplifier

A schematic of a practical implementation of the modulator and demodulator is the circuit presented in figure 5. Four cross-coupled switches, connected to the modulation signal and its complement, are used for this purpose. When ϕ is active, the input signals are straightly transmitted to the output. When ϕ is inactive, the signals are crossed.

The switches in figure 5 can be realized as CMOS transmission gates, as presented in figure 6. The transmission gate consists of two complementary NMOS and PMOS transistors, which are controlled by complementary signals ϕ and $\bar{\phi}$. The circuit acts as a switch driven by ϕ. It has the advantage over the single-transistor switch of presenting a low-impedance between its terminals A and B, whatever the voltages in both these nodes are.

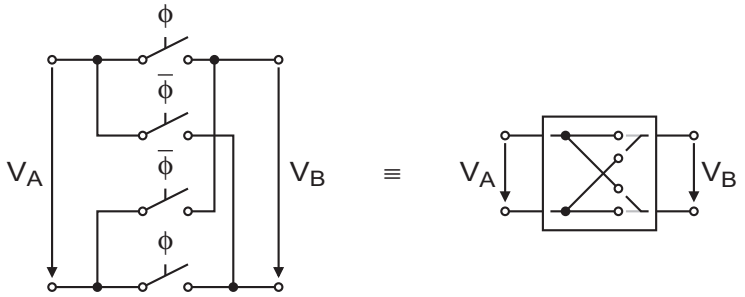

Figure 5. Implementation of a modulator/demodulator using cross-coupled switches

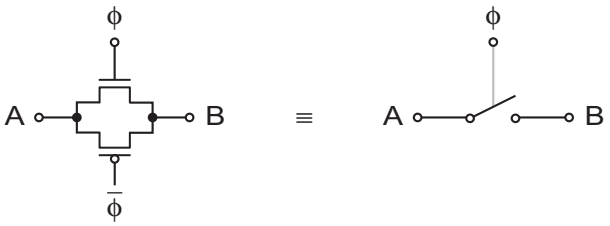

Figure 6. CMOS transmission gate

Using this approach, the implementation of the modulator and demodulator is simple. However, it implies the use of differential inputs and outputs for the amplifier, which is neither practical nor desirable always. Differential inputs are usually available, since most amplifier implementations rely on a differential pair as first stage.

If the amplifier has only one single output, the sign change in the demodulator is more difficult to realize. Figure 7 presents an example of circuit implementing the required function. When ϕ is active, the input signal is directly fed to the output. When ϕ is inactive, the amplifier changes the sign of the input since its gain is designed to be -1.

The main drawback of this solution is the difficulty to obtain precisely the -1 gain, because it depends on the quality of the matching of the two resistors. A second problem arises from the delay introduced by the additional amplifier, making the circuit asymmetrical for both phases. Finally, the imperfections of the additional amplifier, such as offset and noise, degrade the overall system performance. In this example, this is not problematic if the chopper amplifier gain A is high, because the input-referred offset and noise of the amplifier in the demodulator are divided by A.

As one can see, single input and/or output chopper amplifiers are less straightforward to design. In some specific applications however, these circuits are more suitable than differential topologies.

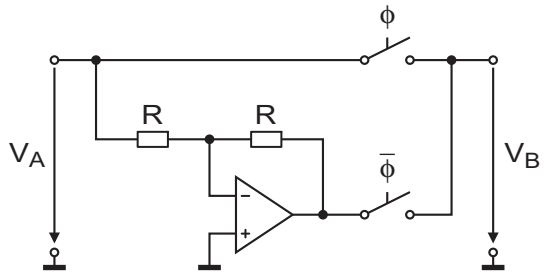

Figure 7. Demodulator for single output chopper amplifier

4 AUTOZERO

Autozero is another common technique used to minimize offset and 1/f noise in amplifiers. The main idea [7] is to first sample the undesired effect and then to subtract it during the second phase when the input signal is processed by the imperfect amplifier.

4.1 Principle

Figure 8 presents the principle of an autozero amplifier [6], which is also applicable to comparators. The amplifier A is ideal, the real amplifier noise and offset being represented by the voltage source connected to the positive input.

During the first phase, the amplifier is disconnected from the input signal by switch S_{in} and the offset V_O and noise V_N voltages are sampled[1] on capacitor C_{AZ} across switch S_{FB}:

$$V_C = \frac{A}{1+A} \cdot (V_O + V_N) \cong (V_O + V_N) \tag{2.2}$$

1. The assumption is made that the open-loop gain A of the amplifier is much larger than 1, which is correct in most cases.