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PRECISION TEMPERATURE SENSORS IN CMOS TECHNOLOGY

by

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Michiel Pertijs
Delft, May 2006

Chapter 1

INTRODUCTION

The low cost and direct digital output of CMOS smart temperature sensors are important advantages compared to conventional temperature sensors. This book addresses the main problem that nevertheless prevents widespread application of CMOS smart temperature sensors: their relatively poor absolute accuracy. Several new techniques are introduced to improve this accuracy. The effectiveness of these techniques is demonstrated using three prototypes. The final prototype achieves an inaccuracy of $\pm 0.1\,^{\circ}\mathrm{C}$ over the military temperature range, which is a significant improvement in the state of the art. Since smart temperature sensors have been the subject of academic and industrial research for more than two decades, an overview of existing knowledge and techniques is also provided throughout the book.

In this introductory chapter, the motivation and objectives of this work are described. This is followed by a review of the basic operating principles of CMOS smart temperature sensors, and a brief overview of previous work. The challenges are then described that need to be met in order to improve the accuracy of CMOS smart temperature sensors while maintaining their cost advantage. Finally, the structure of the rest of the book is introduced.

1.1 Motivation and Objectives

Temperature sensors are widely applied in measurement, instrumentation and control systems. In an average household, at least a dozen temperature sensors can be found in various places, ranging from the coffee machine, to the heating system, to the car. Given this large market, it makes sense to try to fabricate temperature sensors in integrated circuit (IC) technology, as this is ideally suited for the volume production of low-cost products. Moreover, a temperature sensor fabricated in IC technology can be combined with interface electronics on a single chip. Such ‘smart’ sensors have distinct

advantages compared to conventional sensors: they can directly communicate with a microcomputer in a standardized digital format, thus reducing the complexity and increasing the modularity of the system in which they are applied. In addition, the local processing of the sensor signal (amplification, analog-to-digital conversion) makes the measurement more robust to interference [1, 2].

In spite of these advantages, only a minority of the temperature sensors applied today are smart sensors. The semiconductor industry only became successful in marketing smart temperature sensors when an application 'close to home' presented itself: thermal management in personal computers and laptops [3]. Because of the steady increase in heat dissipation that has accompanied the increasing processing power of microprocessors, temperature sensors are needed to track the processor's temperature and regulate its cooling fan. During the last decade, this application has given an enormous boost to the development of smart temperature sensors.

The relatively limited use of smart temperature sensors in other applications can be partially attributed to the success of conventional sensors: platinum resistors, thermistors and thermopiles have been used successfully for decades, so designers are hesitant to adopt a new, 'unproven' technology, in spite of its possible advantages. Also, for some applications, the operating range of integrated temperature sensors (typically $-55\,°\mathrm{C}$ to $125\,°\mathrm{C}$) is too restricted. For many other applications, however, the limited accuracy of smart temperature sensors is the most important obstacle.

There are two main reasons for the limited accuracy of smart temperature sensors. To keep production costs low, smart temperature sensors are often produced in standard CMOS technology, which has been developed for mainstream digital products, not precision analog products. In addition, their temperature error is typically measured (calibrated) and corrected at not more than one temperature. Over their full operating range, the resulting inaccuracy is then typically not better than $\pm 2.0\,°\mathrm{C}$ [1]. For comparison, the inaccuracy that can be obtained with a class-A platinum resistor over that range is $\pm 0.5\,°\mathrm{C}$ [4]. Until recently, such inaccuracy could only be obtained from smart temperature sensors by calibrating them at several temperatures, which undoes much of their cost advantage.

As the use of standard CMOS technology and calibration at not more than one temperature are required to keep production costs low, improvements in the accuracy of smart temperature sensors should be sought in improvements in sensor design and in the calibration procedure. This book presents such improvements. Through a combination of existing precision interfacing techniques and several new techniques, a significant improvement in accuracy has been obtained. This has been demonstrated by the realization of several prototypes, which will be described at the end of the book. The most advanced

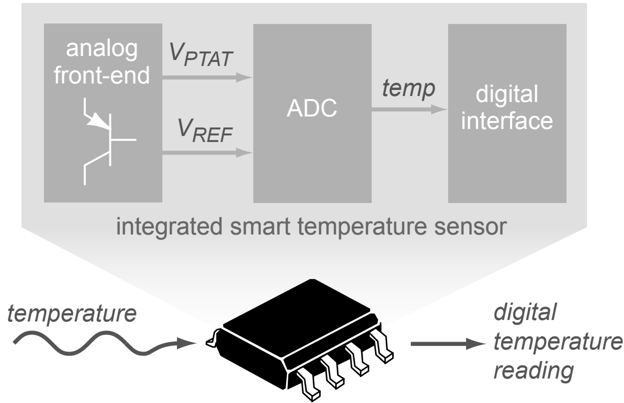


Figure 1.1. Block diagram of an integrated smart temperature sensor.

prototype has an inaccuracy of $\pm 0.1\,°\mathrm{C}$ over the temperature range of $-55\,°\mathrm{C}$ to $125\,°\mathrm{C}$ [5]. This is, to date, the best reported accuracy for this type of sensors.

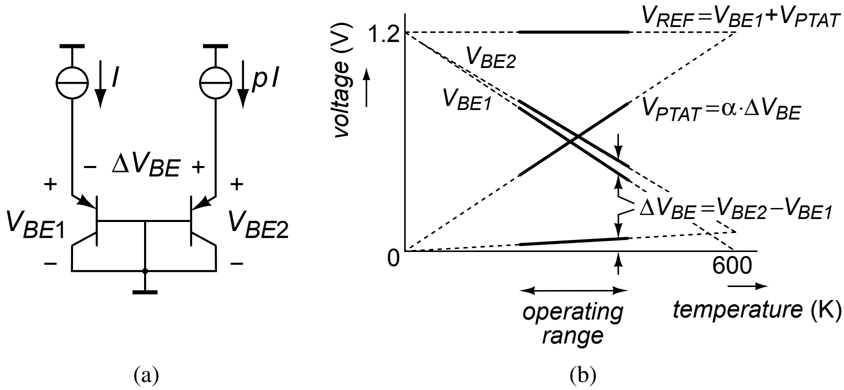
With such improved designs, smart temperature sensors can be produced that can compete with conventional temperature sensors in terms of both cost and accuracy. Thus, the mentioned advantages of smart sensors will become available to a wider range of applications.

1.2 Basic Principles

As virtually every device characteristic in an integrated circuit is temperature dependent, there are numerous ways of making integrated temperature sensors. Sensors have been reported that are based on the temperature dependency of resistors, MOS transistors [6], thermal delay-lines [7], tunneling diodes [8] and, predominantly, bipolar transistors [9]. The output of such sensors is typically an analog signal: a temperature-dependent voltage, current, period or frequency.

A single temperature-dependent analog signal alone, however, is not enough to realize a *smart* temperature sensor. This is because the output of a smart temperature sensor should be a digital representation of its temperature. To produce such a representation, a temperature-dependent signal needs to be compared with a reference signal, that is, a *ratiometric* measurement is needed.

Most smart temperature sensors make use of the characteristics of bipolar transistors. These characteristics are based on two voltages that can play the role of the signals required for ratiometric temperature measurement: the thermal voltage kT/q (where k is Boltzmann's constant, T is the absolute temperature, and q is the charge of an electron) and the silicon bandgap voltage V_{g0}. The thermal voltage can be used to generate a voltage V_{PTAT} that is proportional



(a) (b)

Figure 1.2. Operating principle of a CMOS smart temperature sensor: (a) two diode-connected pnp transistors are biased at a well-defined current density ratio $1 : p$; (b) their base-emitter voltages are used to generate a voltage proportional to absolute temperature V_{PTAT} and a bandgap reference V_{REF}, the ratio of which is a measure of temperature.

to absolute temperature (PTAT), while the bandgap voltage is the basis for generating a temperature-independent reference voltage V_{REF} [9].

In an integrated smart temperature sensor (see Figure 1.1), a number of bipolar transistors are combined with precision interface circuitry in an analog front-end to extract these voltages. A digital representation of their ratio is then determined by an analog-to-digital converter (ADC). This ratio is a measure of the chip's temperature and is communicated to the outside world (e.g. to a microcomputer) by means of a digital interface. This interface can be, for instance, a standardized serial interface, such as I^{2}C, that allows the sensor to communicate over a small number of wires, possibly shared by multiple sensors [2].

Figure 1.2 illustrates the operating principle of the analog front-end. In CMOS technology, the bipolar transistors are usually substrate pnp transistors, which are parasitic devices that are present as a side-effect of the MOS transistors for which the technology was designed. The PTAT voltage is generated from the difference in base-emitter voltage ΔV_{BE} between two such transistors biased at different current densities (Figure 1.2a). If the ratio p of the bias currents is well-defined, this difference is accurately PTAT. It is, however, quite small ($0.1 - 0.25\,\mathrm{mV}\,/\,\mathrm{K}$) and therefore needs to amplified to get a useful voltage V_{PTAT}.

The reference voltage is based on the absolute base-emitter voltage of a bipolar transistors, rather than on a difference. Extrapolated to $0\,\mathrm{K}$, this base-emitter voltage is equal to the silicon bandgap voltage of about $1.2\,\mathrm{V}$ (Figure 1.2b). From there, it decreases by about $2\,\mathrm{mV}\,/\,\mathrm{K}$. To compensate for this decrease, a voltage $\alpha \cdot \Delta V_{BE}$ is added to it, resulting in a voltage V_{REF} that is

essentially temperature-independent [9]. Since V_{REF} is nominally equal to the silicon bandgap voltage, such a reference is referred to as a 'bandgap reference'.

1.3 Context of the Research

General-purpose bandgap references were invented before temperature sensors based on the same principles came around. The first bandgap reference was introduced by Hilbiber in 1964 [10] and made practical in the seminal work of Widlar in 1971 [11]. The first analog sensor that used ΔV_{BE} as a measure of temperature was presented by Verster in 1968 [12], while the first integrated version of such a sensor was described by Dobkin [13]. A lot of pioneering work was done by Meijer [14]. The first *smart* temperature sensors (based on a ratiometric measurement and with a digital interface) were introduced around 1985 and targeted the relatively small temperature range required to measure human body temperature [15, 16]. They were fabricated in bipolar technology, which dominated the industry at the time. A more general-purpose smart sensor was introduced by Meijer in 1989 [17].

During the 1990's, CMOS technology became mainstream. Due to the ever-increasing demand for digital circuits, CMOS technology became available at much lower costs than bipolar technology. Though digital CMOS technology is typically not designed to include bipolar transistors, such transistors usually are available as parasitic devices. These devices come in two flavors, lateral and vertical, both of which have, for general purposes, a poorer performance than their counterparts in bipolar technology.

Already in 1983, Vittoz investigated the characteristics and application of lateral bipolar transistors and pointed out that they could be used in CMOS temperature sensors [18]. The first CMOS smart temperature sensor based on lateral bipolar transistors was published by Krummenacher in 1990 [19].

The temperature dependency of vertical bipolar transistors has been studied by Wang, who has shown that they are very suitable for making bandgap references and temperature sensors [20]. Moreover, Fruett [21] and Creemer [22] have shown in their study of the piezo-junction effect that vertical pnp transistors in CMOS are relatively insensitive to mechanical stress. This makes them the device of choice, especially for temperature sensors that are exposed to stress due to low-cost plastic packaging.

One of the first CMOS smart temperature sensors based on vertical bipolar transistors was presented by Bakker in 1996 [23]. His work focused on solving the problem that amplifiers in CMOS technology have a much larger offset than their counterparts in bipolar technology, which prevents accurate amplification of ΔV_{BE}. With his nested-chopper technique, he reduced the offset to the $100\,\mathrm{nV}$ level, which reduces the associated temperature errors to negligible levels [1]. The dynamic element matching technique, introduced by Klaassen [24] and Van der Plassche [25], can be employed to make amplifiers with an

accurate gain. Its applicability to temperature sensors has been demonstrated by Meijer *et al.* [26].

Most recent work on smart temperature sensors has been performed in industry, fueled by their above-mentioned application in PCs and laptops. The biggest players in this field are Analog Devices [27], National Semiconductor [28] and Maxim [29], who have all developed an extensive line of thermal management chips. For this application, an accuracy of $\pm 1.0\,^{\circ}\mathrm{C}$ is usually sufficient, although a higher accuracy for the same price is of course a competitive advantage. Developments have mainly focused, however, on incorporating extra functionality on the sensor chip, such as voltage monitoring and temperature measurement of a remote diode located on the microprocessor chip [3].

1.4 Challenges

The accuracy that can be reached with a smart temperature sensor is ultimately determined by the accuracy of the temperature characteristics of the bipolar transistors. How much trimming is needed depends on the reproducibility of these characteristics in production. The difference in base-emitter voltage ΔV_{BE} is very reproducible, because the components that depend on production parameters cancel when two base-emitter voltages are subtracted. As a result, as will be shown in this book, temperature errors as a result of inaccuracy of ΔV_{BE} can be made less than $\pm 0.1\,^{\circ}\mathrm{C}$ when transistor non-idealities are taken into account [30].

A single base-emitter voltage V_{BE} (and therefore also the reference voltage V_{REF} that is derived from it), in contrast, is much less reproducible. This is a result of production tolerances in the CMOS production process, and cannot be avoided by clever circuit design. It results in temperature errors in the order of at least $\pm 1\,^{\circ}\mathrm{C}$. Fortunately, because there is essentially only one degree of freedom in the production spread of V_{BE}, a calibration at a single temperature provides sufficient information to correct the resulting error over the full operating range [26].

There are therefore two main challenges in the design of a high-accuracy CMOS smart temperature sensor. First, the sensor's electronics have to be designed in such a way that the spread of V_{BE} is the only significant error source. Second, a cost-effective calibration technique has to be developed that can be used determine the temperature error resulting from the spread of V_{BE}.

The first challenge is one of precision analog circuit design, and can be broken down in two sub-challenges (see Figure 1.3). The first is the design of a circuit that generates well-defined bias currents for the bipolar transistors and operates them in a region most suited for accurate temperature sensing. This is the main topic of Chapter 3 of this book. The second is the design of an ADC that accurately processes the base-emitter voltages and generates the desired

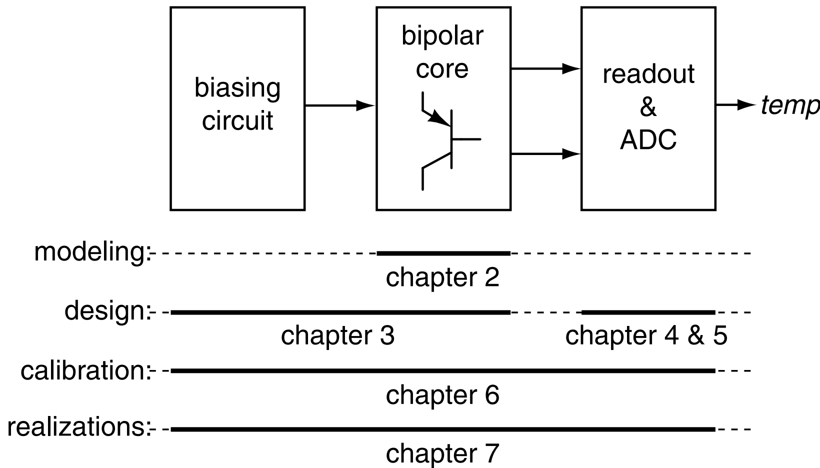


Figure 1.3. Sub-blocks of a smart temperature sensor, with an indication of where they are discussed in the book.

digital temperature reading. The system-level design of such an ADC will be discussed in Chapter 4, while the circuit-level design is described in Chapter 5.

The second challenge, the development of a cost-effective technique, is related to the design of the production line. Calibration of smart temperature sensors can either take place on wafer-level, i.e. before the sensors are diced and packaged, or after packaging. Calibration at wafer-level is typically cheaper, because a large number of sensors can be calibrated at the same time. The subsequent packaging, however, introduces additional errors due to mechanical stress, especially if a low-cost plastic package is used [31].

It will be shown that for inaccuracies below $\pm 0.5\,^{\circ}$C, it is required to calibrate the sensors individually after packaging. If this is done in a traditional way, by comparing a sensor's output with an accurate thermometer, a thermal stabilization time in the order of minutes is needed to guarantee a small enough temperature difference between the sensor and the thermometer. This is very long compared to the time typically spent on the electrical production tests performed after packaging, which is in the order of seconds. To keep production costs low, an alternative technique is needed that can be completed in the same time frame as the electrical tests. Such techniques are introduced in Chapter 6.

1.5 Organization of the Book

The organization of this book is as follows (see Figure 1.3). In order to improve the design of CMOS smart temperature sensors, a solid understanding of the characteristics of the sensor element, i.e. the bipolar core, is needed.

This is developed in Chapter 2, by reviewing the relevant physical backgrounds of bipolar transistors, and by modeling the non-idealities of V_{BE} and ΔV_{BE}. This establishes a lower bound on the overall accuracy that can be obtained. Trimming is shown to be indispensable for inaccuracy below $\pm 1.0\,^{\circ}\mathrm{C}$, but it is also shown that a calibration at a single temperature can be sufficient to achieve a high accuracy over a wide temperature range.

Given the models for the behavior of the bipolar core, design techniques for the other parts of the sensor are developed in Chapters 3, 4 and 5. In Chapter 3, the combination of the biasing circuit and the bipolar core is considered. This 'front-end' of the sensor generates the two voltages V_{BE} and ΔV_{BE}. The techniques discussed in Chapter 3 focus on reducing or compensating for the non-idealities of these voltages.

Chapter 4 discusses the system-level design of the ADC that processes V_{BE} and ΔV_{BE}. Sigma-delta ADCs are found to be best suited for precision smart temperature sensors. The principles of first- and second-order sigma-delta converters are described. Details of the design of a decimation filter that can directly provide an output in $^{\circ}\mathrm{C}$ are also included. Finally, the filtering properties of sigma-delta ADC are discussed, which are important if dynamic error correction techniques are applied in the front-end of the sensor, which generate modulated signals at the input of the ADC that need to be filtered out.

Sigma-delta ADCs can be realized using continuous-time or switched-capacitor circuits. In Chapter 5, these alternatives are analyzed and compared in terms of accuracy and noise. Offset cancellation and dynamic element matching techniques are discussed, which are needed for accurate conversion in the presence of mismatch.

In Chapter 6, three low-cost calibration techniques are described and compared with conventional techniques.

In Chapter 7, the techniques discussed in Chapter 3-6 are combined in three realizations, which achieve inaccuracies of $\pm 1.5\,^{\circ}\mathrm{C}$, $\pm 0.5\,^{\circ}\mathrm{C}$, and finally $\pm 0.1\,^{\circ}\mathrm{C}$. Details of these realizations are described and experimental results are presented. The results are compared with previous work, showing that the realized sensors have the highest reported accuracy to date.

The book ends with conclusions and a summary. Special sections have been devoted to other applications of the work and future work on smart temperature sensors.

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Chapter 2

CHARACTERISTICS OF BIPOLAR TRANSISTORS

Bipolar transistors form the core of most smart temperature sensors. This chapter reviews the physics of bipolar transistors and the various effects that determine the temperature dependency of their base-emitter voltage. The bipolar transistors available in standard CMOS processes are described and compared. Their most important non-idealities are discussed, including their sensitivity to processing spread and mechanical stress. The models introduced in this chapter will be used extensively in the rest of the book.

2.1 Introduction

As mentioned in Chapter 1, most smart temperature sensors essentially digitize the thermal voltage kT/q, using the bandgap voltage V_g as reference. To help understand where these voltages come from, the basics of bipolar transistors physics will be reviewed. First, the characteristics of junction diodes will be discussed, along with the non-idealities that prevent the use of such diodes in temperature sensors. Then, building on the same principles, the operation of bipolar transistors will be explained, and their relevant non-idealities will be reviewed.

2.1.1 The Ideal Diode Characteristic

Since the p-n junction diode forms the basic building block of a bipolar transistor, and shows an exponential current-voltage characteristic that is similar to that of a bipolar transistor, it is useful to briefly review its physical backgrounds [1,2].

When a piece of p-type material is joined together with a piece of n-type material, electrons will diffuse from the n-side to the p-side, and holes will diffuse in the opposite direction. Positive donor ions and negative acceptor ions

are left uncovered near the junction in the n-side and p-side respectively, forming a depletion region. The resulting electric field causes electrons and holes to drift in a direction opposite to the diffusion currents. In thermal equilibrium, there is no net current across the junction, and the drift and diffusions currents balance each other out.

If an external voltage V is applied to a p-n junction, the balance between the drift and diffusion currents is disturbed. For a positive voltage (forward bias), the drift current is reduced in favour of the diffusion current, resulting in net current flowing from the p-side to the n-side and a decrease in the depletion region width. The concentration of minority electrons on the p-side of the depletion region is then given by

$$n_{p-side} = n_{p0} \exp\left(\frac{qV}{kT}\right), \tag{2.1}$$

where n_{p0} is the equilibrium concentration of electrons. Similarly, the concentration of minority holes on the n-side of the depletion region is given by

$$p_{n-side} = p_{n0} \exp\left(\frac{qV}{kT}\right), \tag{2.2}$$

where p_{n0} is the equilibrium hole concentration. The exponential dependency in these equations results from the Maxwell-Boltzmann approximation to the Fermi-Dirac probability function. According to this approximation, the concentration of electrons in the conduction band and that of holes in the valence band depends exponentially on the position of the Fermi energy level. Since an external voltage V results in a Fermi level that changes throughout the diode (in contrast with the constant Fermi level of a diode in equilibrium), an exponential dependency on V appears [2].

Far away from the depletion region, the minority-carrier concentrations equal their equilibrium values. As a result, the electron concentration on the p-side decreases away from the depletion region, and the hole concentration on the n-side does the same. These concentration gradients give rise to diffusion currents. The total current flowing through the diode is the sum of these diffusion currents, and can be described by

$$I_D = \frac{qAD_n(n_{p-side} - n_{p0})}{L_n} + \frac{qAD_p(p_{n-side} - p_{n0})}{L_p}, \tag{2.3}$$

where D_n and L_n are the diffusion constant and the diffusion length of minority electrons on the p-side, D_p and L_p are the diffusion constant and the diffusion length of minority holes on the n-side, and A is the junction area. Substituting (2.1) and (2.2) in this equation gives the well-known ideal diode characteristic

$$I_D = I_S\left(\exp\left(\frac{qV}{kT}\right) - 1\right), \tag{2.4}$$

where the saturation current I_S is given by

$$I_S = \frac{qAD_n n_{p0}}{L_n} + \frac{qAD_p p_{n0}}{L_p}. \tag{2.5}$$

The equilibrium electron and hole concentrations n_{po} and p_{no} can be expressed in terms of the intrinsic carrier concentration n_i and the acceptor and donor concentrations N_a and N_d, respectively:

$$n_{po} = \frac{n_i^2}{N_a}, \quad p_{no} = \frac{n_i^2}{N_d}, \tag{2.6}$$

which leads to the following expression for the saturation current I_S:

$$I_S = qAn_i^2 \left(\frac{D_n}{L_n N_a} + \frac{D_p}{L_p N_d} \right). \tag{2.7}$$

For forward-bias voltages $V \gg kT/q$, the -1 term in (2.4) can be neglected. The voltage drop that develops across the diode when a given bias current I is applied is then

$$V = \frac{kT}{q} \ln \left(\frac{I}{I_S} \right). \tag{2.8}$$

If two bias currents I_1 and $I_2 = pI_1$ are successively applied to a diode, the difference in voltage drop is

$$V_2 - V_1 = \frac{kT}{q} \ln \left(\frac{pI_1}{I_S} \right) - \frac{kT}{q} \ln \left(\frac{I_1}{I_S} \right) = \frac{kT}{q} \ln p. \tag{2.9}$$

This difference is proportional to absolute temperature (PTAT) and, ideally, independent of any processing-related parameters. As such, it seems very useful for temperature sensing. However, as will be discussed in the next section, non-ideal effects that are not modelled in equation (2.4) make most diodes unsuitable for accurate temperature sensing [3].

2.1.2 Non-Idealities of Diodes

The ideal diode characteristic (2.4) is based on the assumption that no generation or recombination of electron-hole pairs takes place in the depletion region. In practice, however, some of the carriers injected across the depletion region will recombine. The resulting recombination current can be described by

$$I_{rec} = I_{r0} \exp \left(\frac{qV}{2kT} \right), \tag{2.10}$$

where I_{r0} depends on the width of the depletion region, the recombination lifetime, and the intrinsic carrier concentration [2].

The total diode current is the sum of (2.4) and (2.10). Because of the factor 2 in (2.10), the two exponential terms cannot be easily combined in a single exponential expression. In practice, the following empirical approximation is often used:

$$I = I_S \left(\exp\left(\frac{qV}{nkT} \right) - 1 \right), \tag{2.11}$$

where n is the so-called non-ideality factor [2]. This approximation is valid only for a limited range of voltages. For large forward-bias voltages, when diffusion dominates, $n \approx 1$, and for low forward-bias voltages, when recombination dominates, $n \approx 2$. In the intermediate region, $1 \leq n \leq 2$.

With this empirical approximation, the PTAT voltage given by equation (2.9) becomes proportional to the non-ideality factor n. Since n depends on I_{r0}, which in turn depends on processing parameters, the PTAT voltage becomes sensitive to processing spread. This prevents the use of practical silicon diodes for accurate temperature sensing [3]. Fortunately, as will be shown in the next section, bipolar transistors behave much more ideal, with a non-ideality factor very close to 1.

2.2 Bipolar Transistor Physics

The relation between the collector current I_C and the base-emitter voltage V_{BE} of a bipolar transistor in its forward-active region is similar to the current-voltage characteristic of a diode. The non-idealities that prevent the use of diodes for accurate temperature sensing, however, are not part of the collector current of a bipolar transistor, but give rise to a base current. The $I_C - V_{BE}$ characteristic therefore follows the ideal exponential behaviour much better than the $I - V$ characteristic of a diode.

In this section, first the ideal characteristic of a pnp transistor will be derived. The discussion is based on a pnp transistor rather than an npn transistor because the transistors available in most CMOS processes are pnp transistors. Then, non-idealities of the $I_C - V_{BE}$ characteristic will be discussed. Finally, it will be shown that in some cases the base current is sufficiently well-behaved for transistors to be used in a 'diode-connected' configuration, in which their $I_E - V_{BE}$ characteristic is used.

2.2.1 Sign Conventions

Figure 2.1 shows the sign conventions often used in literature for npn and pnp transistors [4]. The polarities of the voltages and currents are chosen such that positive values correspond to the forward-active region of the transistor. For a pnp transistor, the *emitter-base* voltage is positive in this region. Therefore, one should strictly speaking use 'V_{EB}' and 'ΔV_{EB}' when discussing temperature

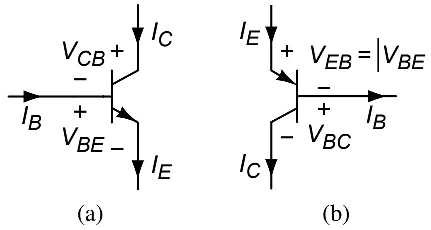

Figure 2.1. Sign conventions used for (a) npn transistors and (b) pnp transistors; positive voltages and currents correspond to the forward-active region.

sensors based on pnp transistors. However, in literature on CMOS temperature sensors and bandgap references (see for instance [5–7]), the symbols 'V_{BE}' and 'ΔV_{BE}' are often used instead, so as to be able to use the (more familiar) equations of an npn transistor. In this work, the same convention will be followed. In the equations in the following sections, the symbol 'V_{BE}' should therefore be strictly speaking be read as $|V_{BE}|$, or V_{EB}.

2.2.2 The Ideal $I_C - V_{BE}$ Characteristic

Consider a pnp transistor in its forward-active region, i.e. with a forward-biased base-emitter junction and a reverse-biased base-collector junction [8]. In this region, the current flow in the base-emitter junction is similar to that in the diode discussed in the previous section: holes are injected into the base region by the emitter, and electrons are injected into the emitter region by the base. The acceptor concentration in the emitter, however, is usually much larger than the donor concentration in base: the base-emitter junction is a so-called one-sided diode [2]. As a result, the diffusion current in the base due to the injection of holes will be much larger than that in the emitter due to the injection of electrons.

The injection of holes results in a minority-carrier concentration $p_{n,em}$ at the emitter-side of the base region that is larger than the equilibrium concentration p_{n0}, but still small compared to the majority-carrier concentration. It depends exponentially on the base-emitter voltage:

$$p_{n,em} = p_{n0} \exp\left(\frac{qV_{BE}}{kT}\right), \tag{2.12}$$

As for the diode discussed in the previous section, this exponential dependency comes from the Boltzmann approximation to the Fermi-Dirac distribution function. As before, the equilibrium concentration p_{n0} can be expressed in terms of the donor concentration N_d in the base and the intrinsic carrier concentration n_i:

$$p_{n0} = \frac{n_i^2}{N_d}. \tag{2.13}$$

Since holes are swept away across the reverse-biased base-collector junction, the minority-carrier concentration at the collector side of the base region is approximately zero. The resulting concentration gradient results in diffusion of minority carriers across the base region. In contrast with the diffusion of holes in the n-side of a diode, the diffusion of holes in the base-region takes place over the relatively short base width W_B. Since this is typically much smaller than the hole diffusion length L_p, the hole concentration decreases approximately linearly from $p_{n,em}$ at the emitter side to zero at the collector side. The corresponding collector current can therefore be described by

$$I_C = \frac{qA\overline{D_p}p_{n,em}}{W_B}, \tag{2.14}$$

where A is the emitter area, W_B is the base width, and $\overline{D_p}$ is the average diffusion constant of holes in the base. By combining (2.12)-(2.14), the collector current can be written as

$$I_C = I_S \exp\left(\frac{qV_{BE}}{kT}\right), \tag{2.15}$$

where the saturation current I_S is given by

$$I_S = \frac{qAn_i^2\overline{D_p}}{W_B N_d}, \tag{2.16}$$

The product $W_B N_d$ is the so-called Gummel number G_B, which expresses the number of impurities per unit area of the base. This Gummel number can also be evaluated as an integral of the doping concentration over the base width if non-uniform doping is used. The effective hole diffusion constant $\overline{D_p}$ is related to the effective hole mobility $\overline{\mu_p}$ via the Einstein relation [2]:

$$\overline{D_p} = \frac{kT}{q}\overline{\mu_p}. \tag{2.17}$$

The saturation current can thus also be expressed as

$$I_S = \frac{kTAn_i^2\overline{\mu_p}}{G_B}. \tag{2.18}$$

2.2.3 Non-Idealities of the $I_C - V_{BE}$ Characteristic

The ideal exponential characteristic described by (2.15) implies that a PTAT voltage can be obtained by biasing a transistor at two collector currents I_{C1} and $I_{C2} = pI_{C1}$, and taking the difference of the resulting base-emitter voltages:

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{kT}{q}\ln p. \tag{2.19}$$

As for a diode, non-ideal currents need to be accounted for to evaluate how accurate such a PTAT voltage will be in practice.

Two important mechanisms that affect the collector current are the generation of carriers in the base-collector junction, and the diffusion of minority electrons in the collector [2]. These mechanisms result in a leakage current in the base-collector junction that adds to the collector current and would disturb the current ratio p. Fortunately, these currents can be reduced to negligible levels by ensuring that the base-collector voltage is zero.

In that case, however, the assumption that the minority hole concentration at the collector side is zero is not valid anymore. Rather, it will be equal to the equilibrium hole concentration p_{n0}. The hole concentration $p_{n,em}$ at the emitter side due to injection will have to be significantly larger than p_{n0} for (2.15) to be accurate. Replacing $p_{n,em}$ in the diffusion-current equation (2.14) by $(p_{n,em} - p_{n0})$ leads to a more accurate equation for the collector current:

$$I_C = I_S \left(\exp\left(\frac{qV_{BE}}{kT} \right) - 1 \right). \tag{2.20}$$

This equation is identical to the ideal diode equation (2.4). It results in a modification of ΔV_{BE}:

$$\Delta V_{BE} = \frac{kT}{q} \ln \left(\frac{pI_{C1} + I_S}{I_{C1} + I_S} \right) \tag{2.21}$$

$$\simeq \frac{kT}{q} \ln \left(p - \frac{I_S}{I_{C1}}(p-1) \right), \tag{2.22}$$

which shows that the collector currents I_{C1} and pI_{C1} have to be significantly larger than I_S to obtain an accurate PTAT voltage. Since I_S increases rapidly with temperature (as will be explained later), this requirement is especially relevant at the high end of the operating temperature range.

The collector current cannot be chosen arbitrarily high. A collector current that is too high results in significant self-heating and/or a significant voltage drop across series resistances. Moreover, at a high collector current, the assumption that the minority carrier concentration in the base is low compared to the majority carrier concentration, is not valid anymore. The transistor is then operated in its high-injection region, where $\ln(I_C)$ becomes proportional to $qV_{BE}/(2kT)$ [2]. This effect is illustrated in Figure 2.2a, which shows the logarithm of the collector current as a function of the base-emitter voltage (a so-called Gummel plot).

The reason that a diode can usually not be used to generate an accurate PTAT voltage is the presence of a recombination current with a different temperature dependency than the diffusion current. Recombination also takes place in the base-emitter junction of a bipolar transistor. The crucial difference between a

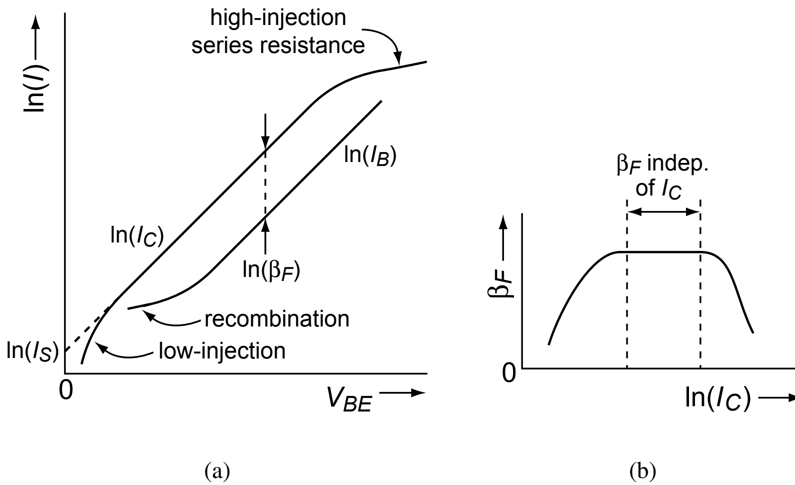

Figure 2.2. (a) The collector current I_C and the base current I_B as a function of the base-emitter voltage V_{BE}, for $V_{BC} = 0$; (b) the associated forward current-gain β_F as a function of the collector current.

diode and a transistor is that the resulting non-ideal components of the emitter current are mainly provided via the base of the transistor. As a result, at low current levels, $\ln(I_B)$ becomes proportional to $qV_{BE}/(2kT)$ (see Figure 2.2a; this effect will be discussed in more detail below). The collector current, in contrast, still follows (2.20) accurately.

In conclusion, in the region where I_C is much larger than I_S and small enough to avoid high injection, the $V_{BE} - I_C$ characteristic of a bipolar transistor is suitable for generating a voltage that is accurately proportional to absolute temperature.

2.2.4 Non-Idealities of the $I_E - V_{BE}$ Characteristic

If the emitter current of a bipolar transistor, rather than its collector current, is set by a current source, the base current has to be taken into account when determining the resulting base-emitter voltage. This is the case in the so-called diode-connected configuration shown in Figure 2.3 [8]. This configuration is especially important for substrate pnp transistors in CMOS technology. These transistors are often connected as a 'diode' by grounding their base. This is done because their collector is formed by the substrate, and is therefore not directly accessible. While this connection ensures that the base-collector voltage is zero, it also results in a collector current that is smaller than the applied emitter current:

$$I_C = I_E - I_B = \alpha_F I_E = \frac{\beta_F}{1 + \beta_F} I_E, \tag{2.23}$$