Essential Issues in SOC Design
Essential Issues in SOC Design
Designing Complex Systems-on-Chip

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Table of Contents

Contributing Authors vii

Chapter 1
   Essential Issues in System-on-a-Chip Design
   Youn-Long Lin 1

Chapter 2
   A SOC Controller for Digital Still Camera
   Jiing-Yuang Lin, Chien-Liang Chen and Youn-Long Lin 7

Chapter 3
   Multimedia IP Development – Image and Video Codecs
   Liang-Gee Chen, Chung-Jr Lian, Ching-Yeh Chen,
   and Tung-Chien Chen 19

Chapter 4
   SoC Memory System Design
   Kun-Bin Lee and Tian-Sheuan Chang 73

Chapter 5
   Embedded Software
   Tai-Yi Huang, Shiao-Li Tsao, Le-Chun Wu,
   Edward T.-H Chu, and Ko-Yun Liu 119

Chapter 6
   Energy Management Techniques for SOC Design
   Hiroto Yasuura, Tohru Ishihara and Masanori Muroyama 177

Chapter 7
   SoC Prototyping and Verification
   Moo-Kyoung Chung, Young-II Kim, Jae-Gon Lee,
   Wooseung Yang, Ando Ki, and Chong-Min Kyung 225

Chapter 8
   SoC Testing and Design for Testability
   Cheng-Wen Wu and Chih-Tsun Huang 265

Chapter 9
   Physical Design for System-on-a-Chip
   Yao-Wen Chang, Tung-Chieh Chen and Huang-Yu Chen 311
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Tian-Sheuan Chang, National Chiao-Tung University
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Chapter 1

ESSENTIAL ISSUES IN SYSTEM-ON-A-CHIP DESIGN

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Abstract: Due to advance in semiconductor manufacturing technology, integration of whole electronics system on a single chip is feasible. Starting with baseline CMOS logic, semiconductor wafer manufacturers have gradually added to their portfolio embedded memory (SRAM, OPT, Flash), mixed signal devices, RF devices, and even MEMS. Because it offers many advantages over traditional multiple-chip solutions, system-on-a-chip (SOC) has drawn great attention from both academia and industry. We expect an SOC solution to be smaller, less expensive, more energy efficient, more reliable, etc. However, designing an SOC for successful mass production is much more complicated than that of traditional simpler logic, memory, or analog chips. This chapter outlines some important issues that face an SOC design team and give brief introduction to each chapter of this book

Keywords: System-On-a-Chip, SOC Design Foundry, Multimedia SOC

1. INTRODUCTION

Since the integrated circuit was invented in 1958, the number of devices that can be massively-produced on a chip has been increased following the Moore’s Law, that is, the number of transistors on a chip doubles every 18 months or so. In the old days when a chip contains only smaller number of transistors, an electronics system consists of a large number of chips housed in many printed-circuit boards which in turn are put into a cabinet. Hence, we can call them system-on-boards. Nowadays, semiconductor
manufacturing process can give us a billion-transistor chip for a few US dollars. This makes possible applications that were previously either impossible or unaffordable.

Ever increasing computational demand from the application side and very deep submicron semiconductor processing from the technology side together make system-on-chip (SOC) reality and necessary.

To design an SOC for successful mass production, we have to cope with many technical and management issues. Here we focus on the technical aspect.

Let’s begin with what constitute an SOC. Like a typical electronics system, an SOC consists of processing elements, I/O devices, storage elements and interconnection structure linking all of them together.

Processing elements could be processors that run embedded software or functional-specific hardware accelerators. There are two popular processor categories: microprocessor for control and management function, and digital signal processor (DSP) for signal processing-specific function. Recently, there are academic and industrial efforts in the so called Application-Specific Instruction set Processor (ASIP), which allows instruction set extension by the users according to the target applications. It is quite common that multiple types and multiple instances of processors are used in a single SOC project. For example, in the TI-OMAP SOC, an ARM microprocessor and a TI DSP core co-exist.

When a software approach cannot deliver adequate performance for an application, we turn to dedicated hardware blocks. Typical accelerators include JPEG image Codec, MPEG-4 Video Codec, Viterbi Decoder, Turbo Code Decoder, AES Encryption/Decryption engines, etc.

To communicate with outside, an SOC usually consists of many types of standard I/O devices. Commonly found I/O IPs include Ethernet MAC and Phy, USB1.1/2.0 Device Controller and Phy, other high-speed serial links such as LVDS (Low Voltage Differential Signaling), Audio/Video Output, Memory Controller, etc.

Both internal and external memories are important to SOC. A typical SOC utilizes hundreds of internal memory blocks. They may be SRAM, ROM, Flash or OTP (One-Time Programmable). Their configurations in terms of number of words, word length, number of read/write access ports, and access speed are all tailor made to fit the applications.

When a memory block is too large to be effectively made on chip, we usually put it off-chip and integrate it with the SOC using a system-in-package (SiP) solution. Commonly used external memory includes DRAM and Non-Volatile Flash Memory. Very often we will find an SiP packed in an SDRAM or DDR-II die. Therefore, the SOC has to include memory controller for SDRAM, DDR, SD Card, MMC Card, Compact Flash, etc.
With all components available, we need a communication structure to put them all together. This is called on-chip-communication or on-chip-bus. Just like the PCI-bus of the PC system allows easy plug-and-play of memory cards, graphics cards, etc, the SOC community has proposed several on-chip-bus standards. One of the most popular bus architecture is the Advanced Microprocessor Bus Architecture (AMBA) by ARM.

As on-chip communication traffic exponentially increases and deep submicron effect makes transferring signals difficult in single cycle, researchers have proposed Network-on-Chip (NoC) communication architecture to cope with the problem. An NoC brings the computer networking technology (i.e., packet routing) to the SOC in order to simplify the design and management of communication among IPs in an SOC.

To design a complex SOC, we have to deal with the following essential issues: (1) Availability of components, (2) System integration and verification, and (3) Physical implementation.

Components used in an SOC are also called silicon intellectual property (IP). The SOC development team has to decide on which IP to use or design. There are many IP vendors each serving some segments of the IP market. For processor IP, software compatibility must be taken into account. For memory and I/O IPs, whether they have mass-production record is the main concern.

In case there are not suitable, ready to use IPs, we have to modify an existing one or develop a new one. Longer turn-around time, higher risk, and greater resource needs must be taken into account.

After we put all components together into a system, we have to verify its functional and timing correctness. In the old days when the chip was small, we usually relied on simulation tools for verification. However, for complex SOC which have high gate count and longer simulation pattern, simulation alone cannot give us sufficient confidence level. Moreover, as processors are integrated, we have to perform software/hardware co-verification down to cycle-accurate level. To cope with this challenge, emulation based prototyping is needed.

Physical implementation of SOC is also more difficult than that of traditional ASIC. Complex SOCs are usually targeted towards advanced nanometer technology (90nm and below). As feature size shrinks, process variation becomes relatively significant. Variation-aware analysis and optimization of timing and power consumption must be introduced into the implementation flow. Design for manufacturability consideration becomes a must.

In the case where system-in-package is chosen, chip and package co-design is inevitable.

After an SOC is tape-out, the design team should work closely with the testing team and the processing engineers to enhance the yield.
2. BOOK OVERVIEW

This book brings together experts from different research areas to present their knowledge in various topics related to SOC design. We hope that they have pointed to possible solutions and research directions for those who are either designing SOCs or are considering entering the field. 

Chapter 2 describes “An SOC Controller for Digital Still Camera.” This is a real industrial case. The authors present their experience in defining specification with system house, taking IP from third parties, integrating the SOC and, finally, ramping up for mass production of millions of units.

Chapter 3 presents “Multimedia IP Development – Image and Video Codec.” The authors describe their academic experience in developing JPEG, JPEG2000 and MPEG4 codec IPs that find their ways into industrial applications.

Chapter 4 deals with “SOC Memory System Design.” Memory will account for majority of silicon area in most SOCs. There is trade-off between memory usage and memory traffic. Careful algorithm and architecture designs will gain significantly in terms of area, performance and power consumption.

Chapter 5 describes “Embedded Software.” Contemporary SOCs all contain one or more microprocessors and DSPs. Both system software and application software are important. Unlike traditional PC-based software, embedded software must have small foot-print and consume less power. Moreover, their interaction with hardware devices and hardware accelerators is more closely coupled.

Chapter 6 presents “Energy Management Techniques for SOC Design.” Since most SOC solutions are for portable devices, which have limited battery life, power efficiency is a major concern. It is well known that the power of a circuit is linearly proportional to the frequency and quadratic proportional to the supply voltage. Depending on the characteristics of applications, we can run circuits at various clock rates to just meet the deadline. Consequently, slow circuit needs only small supply voltage. Dynamically scheduling the frequency and voltage will result in significant energy saving.

Chapter 7 describes “SOC Prototyping and Verification.” It takes a long time and huge costs to get a complex SOC manufactured. We cannot afford to make any mistakes during the design process. Complete verification of functionality and timing is a must for any SOC project. To speed up the verification process, prototyping is a popular approach. This chapter presents an industrial strength verification strategy.

Chapter 8 deals with “SOC Testing and Design for Testability.” Testing is the key to a high quality product. In a complex SOC, we should be able to
test every IP in the shortest possible test application time. Therefore, test integration and scheduling are important issues. Moreover, design for testability enhancement is also a common practice. For example, memory BIST has to be inserted into every memory macros.

Chapter 9 describes “Physical Design for SOC.” In the nanometer semiconductor manufacturing process, chip complexity and process variation together make physical implementation challenging. High complexity calls for hierarchical divide-and-conquer approach, while process variation calls for statistical-based analysis and optimization. A chip should be laid out such that it is manufacturable (i.e., high yield). Therefore, physical design should be aware of a mask making process and the manufacturing process.
Chapter 2

A SOC CONTROLLER FOR DIGITAL STILL CAMERA

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Abstract: We present our experience of designing a single-chip multimedia SOC for advanced digital still camera from specification all the way to mass production. The process involves collaboration with camera system designer, IP vendors, EDA vendors, silicon wafer foundry, package & testing houses, and camera maker. We also co-work with academic research groups to develop a JPEG codec IP and memory BIST and SOC testing methodology. In this presentation, we cover the problems encountered, our solutions, and lessons learned. This case study shows the feasibility of expanding semiconductor wafer foundry service to electronics manufacturing service (EMS) providers who in general have very limited IC design capability/experience. We also point out possible directions for future research.

Keywords: System-On-a-Chip, SOC Design Foundry, Multimedia SOC, Silicon Intellectual Property, Design for Manufacturability

1. INTRODUCTION

Ever increasing computational demand from the application side and very deep submicron semiconductor processing from the technology side together make system-on-chip (SOC) reality and necessary. Makers of such electronics systems as PDA, cellular phone handsets, digital still camera, portal music player, etc., need Application-Specific Integrated Circuits (ASIC) solutions in order to differentiate themselves from the competition,
to increase product value, and to reduce cost. On the other hand, semiconductor wafer foundry has to expand its service scope from wafer manufacturing to mask tooling, cell & I/O library, memory compiler, and up to silicon intellectual properties (IP) such as Phase-Lock Loop (PLL), Digital-to-Analog Converter (DAC), and Analog-to-Digital Converter (ADC). Therefore, there is a need to bridge the gap between electronic system houses and wafer foundry. We call such company SOC design service provider.

An SOC design service provider takes as its inputs from the electronics system house a specification or partially-designed prototype and delivers to its customer layout database in GDSII format ready for manufacturing as depicted in Figure 1. It is also called a fabless ASIC vendor if packaged and tested chips are delivered instead. Close collaboration is needed among all parties in order to successfully bring a competitive product to the market in time.

System houses are also called Electronics Manufacturing Service (EMS) as they do design and manufacture but they do not sell products under their own brands. Instead, their customers are those brand-name companies. Presently, almost all IT products including PC, Notebook, cellular phone, PDA, digital camera, music player, etc., are all operated under this business model. EMS usually does not have IC design capability. Instead, they buy chips from IC design houses and differentiate from one another in system board level design and software. As chip integration level increase, the room for differentiation in the board level shrinks. Therefore, it is natural for them to search for their own chip solutions (ASIC). As EMS usually command huge volume in the order of tens of millions units per year, it is reasonable...
and economically feasible for spinning their own chips. However, chip design is not their core business. Hence, partnership with a chip design service provider becomes essential to an EMS’s competitiveness.

In the semiconductor manufacturing side, the industry is divided into three segments: wafer foundry, packaging and testing houses. In the past, a semiconductor wafer foundry takes GDSII layout database from its customer and delivers manufactured wafers. As technology advances and design complexity grows, more and more customers cannot afford expensive infrastructure and investment required to produce GDSII in house. Wafer foundry can expand its reach of service to those who cannot submit GDSII by teaming up with an SOC design service provider.

For package and testing houses, it is beneficial to co-work with a design service provider too. It is already well known that design for testability is commonly accepted practice. Presently, heterogeneous integration of logic, memory, and radio frequency (RF) devices, makes testing and diagnosis more complicated. Therefore, it is essential to involve testing houses in an SOC design project. As package technology advances, substrate design, pin-to-pad routing, thermal aware package design, layout-package co-design all become very important. Moreover, system-in-a-package (SiP) is gaining momentum. It is very common to pack an SOC together with a DRAM and/or a Flash in a same package. Therefore, cooperation between SOC design service foundry and packaging service providers is also essential.

One of the promising approaches to cope with high design complexity is reusing existing design from previous projects or external sources. Such reusable object is called silicon intellectual property (IP). There are many IP vendors specializing in microprocessor (i.e., ARM, MIPS, Tensilica), digital signal processor (DSP), embedded memory (SRAM, 1T-RAM, ROM compilers), standard interface (USB, Ethernet), analog blocks (PLL, ADC, DAC), accelerators (JPEG, MPEG), etc. We have also seen organization that promotes inter-operability of IPs (e.g., OCP-IP). Usually, it is a tedious process for an SOC project manager to put together all appropriate IPs because there are many uncertainty and ambiguity in diverse IP from diverse sources. It is beneficial to have a one-stop-shopping service such as an SOC design service foundry, which has multiple experiences with various IP. Therefore, productivity is increased and risk reduced.

Digital still camera (DSC) is one of the fastest growing consumer electronics products over the past few years. Due to the success of the JPEG image compression standard, advance in CMOS image sensing and availability of high capacity yet low cost flash memory cards, DSC has virtually taken over the traditional film-based camera in just a few years. Moreover, DSC also penetrates quickly into cellular phone sets, which have become the convergent target of PDA, MP3 audio player, etc. Ever increasing picture resolution and advanced features such as video clip recording requires ultra low power and small form factor integration of all
needed functionality. Therefore, an SOC solution is very attractive to the camera makers.

We describe our experience with designing an SOC for DSC controller applications including IP preparation, system integration and verification, chip implementation, manufacturing, failure analysis and yield enhancement during million-units mass production. In Section 2, we first give the chip specification defined by the camera system maker. Then, we list all the intellectual properties (IP) used and difficulty encountered. The integration and verification of the whole system in a chip is then described. Section 3 presents our chip implementation flow from RTL synthesis down to GDSII layout ready for manufacturing. Then, we describe mass-production-related issues including yield ramp-up and failure analysis. Section 4 describes recent development based on the presented project. Finally, we summarize this chapter in Section 5.

2. A DIGITAL STILL CAMERA SOC

Our objective was to design a single chip controller for 2-million-pixel and 3-million-pixel grade DSC for mass production of 3.5 million units in a span of about 18 months in year 2002 and 2003. In order to satisfy required functionality at a very aggressive cost set to help proliferating the entry-level high-resolution camera, the SOC was specified to include the following IPs:

- A microprocessor capable of both traditional 32-bit RISC and DSP functionality
- A hardwired JPEG encoding and decoding accelerator
- A hardwired custom logic for color image processing
- A USB 1.1. device controller with min-host function and its transceiver PHY
- A dual mode SD/MMC flash memory card host interface
- An SDRAM controller interface
- An LCD interface controller for view-finder
- An NTSC/PAL TV signal encoder for viewing photos on TV
- A 10-bit Video DAC for TV
- An 8-bit LCD DAC
- Two PLLs for clock sources
- 30 SRAM macros for internal buffering

The IP cores come from multiple sources for different reasons. Each of them posts different challenges to the project team. To help their development, to verify the functionality of each individual IP as well as customize some of the IP for the project, we built an SOC platform as depicted in Figure 2. In the platform, some IPs are existing ICs, some are soft cores that can be configured and programmed into the FPGA. All IPs
are interconnected together with an AMBA-AHB/APB on-chip bus system. Because most of the IPs on the platform have been proven many times in previous projects, for each new SOC project we only have to concentrate on verifying newly added or customized IPs. Moreover, whole system verification is also easy due to the readiness of system-level verification bench. This platform approach greatly increase our productivity of IP development, IP qualification, and system verification.

The hybrid RISC/DSP implements both a typical 32-bit RISC instruction set and a DSP-specific instruction set in a unified instruction set architecture to simplify the programming interface. It was not an IP at all. Actually it was a stand alone processor chip used in the previous generations of cameras. For software compatibility concern, we have no option but to replace it with any other IP-style microprocessor such as ARM or MIPS cores. To meet high speed requirement (133MHz @ 0.25um), we have to make it a hard core before integration with other parts of the SOC. To integrate it into the SOC, we have to collaborate with the original vendor to create synthesis, simulation and test models in addition to hardening the processor into a high-speed hard macro.

The USB1.1 device controller and the SD card (secure digital flash memory card) controller are supplied by a third party vendor. They are in
VHDL RTL instead of more locally popular Verilog. Therefore, mixed-language simulation environment has to be set up. Only FPGA prototyping was performed at the time of SOC integration. Moreover, the synthesis scripts and testbenches were less than ideal. Therefore, close intensive co-work/co-debugging was carried remotely.

To meet processing speed requirement of 3M pixels @ 0.1Sec and long battery life, the JPEG codec function has been implemented in a hardware accelerator. We collaborated with a university research laboratory. The effort we spent was in bridging the gap between university prototype and industrial strength design. Also there was discrepancy among the interpretation of the JPEG standard by the system house and the IP developers. Therefore, we added a wrapper around it as depicted in Figure 3. Extensive regressive test of more than 1,000 pictures from different origins was conducted for every change made.

There is a block of custom logic for color image processing. Its function includes auto focusing, auto white-balancing, color image quality enhancement, etc. It was supplied by the camera maker in Verilog RTL.

There were more than 30 SRAM macros used in the SOC. We have jointly developed a memory BIST (Built-In Self Test) generator, again with a university laboratory. The generated BIST circuit performs testing...
of 100% coverage without patterns from the tester machines. Therefore, testing cost is greatly reduced during production.

After all IP models are made ready, whole system integration and verification is an even bigger challenge. We encountered the problem of in-consistent and in-sufficient testbenches. Therefore, developing testbench as the project goes is very important.

Our verification set up is a mixture of simulation and FPGA/chip co-emulation.

3. CHIP IMPLEMENTATION

Figure 4 depicts our chip implementation flow from RTL to GDSII ready for tape-out. The DSC controller consists of 240K gates excluding memory macros. After whole system verification with hybrid emulation/simulation, it was implemented in TSMC 0.25um 1P5M CMOS process and packed in TFBGA256 package. It took three months for a team of six engineers to complete the Netlist-to-GDSII implementation. During the course, there are 3 spec changes involving re-synthesis and FF modification, 10 netlist changes involving ECO of combinational logic, 3 ECO changes to fix setup/hold time violation, and 13 versions of pin assignments to simplify the substrate design.

There are 30 embedded memory macros in the controller. We use an in-house memory BIST circuit generator to insert one common BIST controller, multiple sequencers, and 30 pattern generators. The MBIST is from collaboration between us and a university research laboratory. After scan insertion, the fault coverage was 93%.

The physical design of the chip was done with timing-driven placement and routing, physical synthesis, formal verification and STA QoR check.

During chip implementation, we encountered several problems:

- During the course, there are 3 spec changes involving re-synthesis and FF modification, 10 netlist changes involving ECO of combinational logic, 3 ECO changes to fix setup/hold time violation, and 13 versions of pin assignments.
- There existed inconsistency between simulators/versions among customer, IP vendors and ourselves. The customer used PC-based Verilog/Modelsim while we used NC-Verilog. This lead to extra twist during ASIC sign-off.
- IP quality is less than ideal. We have to clean up many DRC/LVS violation in the database provided by the IP vendors.
- The USB IP was delivered in FPGA-targeted RTL. No robust synthesis
script was available and the first RTL level simulation was failed. We had to co-work with the IP vendor over 10 versions of RTL code modification or synthesis constraint updates.

Because there is no automation tool available, we manually performed many versions of pin assignments to reduce the number of substrate layers from four to two resulting in packaging cost saving.

After overcoming all of the above problems, we were able to tape-out on time. Figure 5 shows the layout image of the chip. We achieved the first silicon work.

During mass production, manufacturing tests uncovered that the yield killer (5% loss) was in the insufficient driving strength of an output buffer in the CPU. The chip also went through reliability tests including ESD performance test, temperature cycle test, high/low temperature storage test and humidity/temperature test.

The mass production yield was enhanced from 82.7% initially to very close to the foundry yield model of 93.4% over a period of 8 months. Our measures include optimizing probe card overdrive spec, optimizing power relay waiting time, and retargeting Isat and Vth by optimizing poly CD in the foundry according to results from corner lot splitting.
We have been asked to perform failure analysis on 20 returned chips that have pins shorted to GND. After checking substrate delaminating and popped-corner using scanning acoustics tomography, we found no abnormality. Finally, by sinking 400mA of current to the corresponding pin of a good chip we concluded that the failure was due to a system board bug.

4. **RECENT DEVELOPMENT**

We went on to produce over three million of the chips over 18 months. Our system customer was able take about 8% of world-wide market share in the 2 and 3 million pixels segment during that period. We have also migrated the chip from 0.25um process to 0.18um one, achieving 20% saving in die cost. The migration was easy because we have been familiar with the design and the design flow.

The project has demonstrated that it is feasible to bridge the gap between the need of an electronics system house without IC design capability and the production capacity of a semiconductor foundry with an SOC design service provider. We have been able to leverage the experience gained and lesson learned to serve more customers and more projects such as DVD player, cellular phone set, electronics photo display, etc.
As both applications and technology become more advanced, we have expanded our IP portfolio to include MPEG-4 Encoder/Decoder/Codec, USB2.0 Device Controller, USB On-The-Go (OTG), SerDes I/O and embedded non-volatile memory such as flash and one-time-programmable (OTP). We have also enhanced our EDA flow to be able to simultaneously handle dozens of multi-million gate design at 0.13um and 90nm processes.

Current complex SOC projects require virtual prototyping, signal integrity check (crosstalk, electron-migration, dynamic IR drop, de-coupling cell insertion), design for manufacturability (intra-die process variation modeling, double via, dummy metal insertion), STA sign-off with in-die variation analysis, hierarchical DFT and physical implementation, low power solution (multi Vt/VDD cell library, gated clock, power down isolation) and flip-chip solution.

We have extended the development of memory BIST to more complicated SOC testing. In an SOC employing multiple IPs, each with test sequence, effective integration of all tests with necessary additional circuitry and test schedule is very important.

We have also extended the multimedia IP development from JPEG to JPEG2000, MPEG-4 and H.264/AVC standards. Although there are many software or ASIP approaches, we focused on pure hardwired approach because cost is a very important factor in mass consumer market. Figure 6 depicts the block diagram of an H.264/AVC decoder.
5. CONCLUSION

We have presented a new business model called SOC design foundry along with a case study of putting together resources and IP from both industry and academia, from multiple countries to implement a successful SOC for digital still camera all the way to mass production.

As applications are becoming more demanding and process technology is becoming more advanced, we expect to see more and more complex SOC integration. We will see advanced video such as H.264/AVC and wireless communication function being integrated together. Dealing with more IP sources is certainly more complicated but unavoidable.

A mass-production-proven SOC platform including IP, system, chip implementation to GDSII, and production methodologies will be a feasible approach to response to the challenge.

REFERENCES

Chapter 3

MULTIMEDIA IP DEVELOPMENT
Image and video codecs

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Abstract: Multimedia intellectual property (IP) cores play a critical role in a successful multimedia SOC design. This chapter will focus on the design of image and video codec IPs, which usually requires lots of computational power. From theory to practice and from algorithm to hardware architecture, design methodologies toward an optimized architecture and also real design cases will be presented. Both top-down system analysis and bottom-up core module design are emphasized. Following theoretical discussions of the overall scenario, key building blocks of image and video codecs proposed in literature are reviewed. Examples will cover motion estimation, discrete cosine transform, discrete wavelet transform, and entropy coder. Then, complete image and video codec designs are explored. JPEG, JPEG 2000, and H.264/AVC are the three case studies. This chapter is intended to provide an overview, from theory to practice, on how to design efficient multimedia IPs.

Keywords: image; video; compression, codec; architecture; intellectual property (IP)

1. INTRODUCTION

In this chapter, the design issues and methodologies of image and video codec IPs are discussed. Driven by cost and performance, system-on-a-chip (SoC) is a design trend. Intellectual Property (IP) integration is a must for designers to bridge the gap between design productivity and technology advances. In the post-PC era, there are more and more multimedia consumer products. In a complex multimedia SoC, the development of an optimized image/video codec IP is a critical point.

Digital image/video compression and decompression require many computing and bandwidth resources. To cope with the design challenges of
high-specification image and video codecs, dedicated architecture is chosen to provide the most efficient implementation. No matter the final integration is in the form of a platform-based design with dedicated accelerators in module level or a fully hardwired codec system, dedicated hardware does efficiently off-load the processor in a complex SoC.

This chapter is organized as follows. Section 2 is a brief introduction of digital image and video coding. Section 3 is a comprehensive discussion about the design issues and methodology for the development of a good codec IP. In Section 4, some module-level design cases are presented. These critical modules are the basic building blocks of a codec system. In Section 5, the JPEG [1], JPEG 2000 [2] and H.264/AVC [3] codec designs are discussed. Finally, Section 6 summarizes this chapter.

2. DIGITAL IMAGE AND VIDEO CODING

2.1 Applications

We start by talking about applications since it is the application that drives the advances of technologies. There are more and more multimedia products in our daily life. Consumers continue to look for not only convenient but also fancier appliances (Figure 1), such as digital still camera (DSC), digital camcorder, multimedia phone, DVD player, digital TV, etc. Digital image and video become one of the most attractive features.

As we continuously pursue higher quality digital image and video, the huge amount of digital image and video data become a problem. Unlike

Figure 1. Digital image and video applications
voice or text data, whose data size is not that large, both the transmission and storage of image and video data are big issues since high resolution and high quality image and video always result in large data size. To transmit or store the uncompressed raw data is wasteful in the view of time and cost. To alleviate these problems, image and video compression are important enabling technologies for multimedia products.

Thanks to the advances of IC technologies, modern multimedia products can be light, thin, and small. In the old days, a system consists of many chips. Nowadays, more functions can be integrated on a single chip. The form factor of IC and hence the overall product become smaller. Less cost and higher performance are achieved. Successful and on-going examples such as

- DVD chips that integrate the MPEG core, the servo control, and related signal processing.
- DSC chips that integrate the JPEG, the image processing pipeline, and the camera control.
- Multimedia phone chips that integrate the multimedia engine (audio, video and graphics), the base-band processor and system control.

2.2 Image and Video Coding Basics

The basic concept of image and video compression is redundancy removal. The types of redundancy can be classified as spatial, temporal, statistical, and visual redundancy. By some mathematical algorithm and human visual system (HVS) characteristics, the digital image and video information can be manipulated and represented in a more compact way. That is what digital image and video coding (compression) does to shrink the data size.

It will be a long story to talk all the techniques on image and video compression. Readers are referred to some other books [4][5][6] that have more detailed introduction of image and video coding algorithms and standards. This section only provides a brief overview of some basic techniques that are more representative. In the following, transform coding, quantization, entropy coding, motion estimation (ME) and motion compensation (MC) will be briefly introduced.

2.2.1 Transform coding: Discrete Cosine Transform (DCT) and Discrete Wavelet Transform (DWT)

Transform coding is to transform the image data from the spatial domain to the frequency domain. After the transformation, there is an advantage of signal energy compaction, which is better for data compression. Also, the HVS characteristic of the sensitivity on different frequency components can be used for quantization.
Transform coding forms the basis of image and video coding standards. For image coding standards, JPEG selects DCT \([7]\) as its transformation, and JPEG 2000 adopts DWT. For current video coding standards, DCT is the mainstream. The DWT is adopted for the temporal filtering in the emerging scalable video coding (SVC) standard.

For an \(8 \times 8\) block \(x(m,n)\), where \(0 \leq m, n < 8\), the forward and inverse 2D DCT equations are

\[
Z(p,q) = \frac{1}{4} \sum_{m=0}^{7} \sum_{n=0}^{7} x(m,n) \cos \left(\frac{2m-1}{16}\right) \pi p \cos \left(\frac{2n-1}{16}\right) \pi q
\]

\[
x(m,n) = \frac{1}{4} \sum_{p=0}^{7} \sum_{q=0}^{7} Z(p,q) \cos \left(\frac{2m-1}{16}\right) \pi p \cos \left(\frac{2n-1}{16}\right) \pi q
\]

where \(0 \leq m, n, p, q < 8\), \(\alpha(0) = \frac{1}{\sqrt{2}}\), and \(\alpha(i) = 1\) for \(i \neq 0\). Figure 2 (a) shows the result of a Lena image after \(8 \times 8\) DCT. The \(Z(0,0)\) of each block is the DC coefficient, whose energy is usually higher. The other 63 coefficients are AC coefficients, which contain higher frequency information. Their values are usually small, and may be quantized to zero at high compression level.

The 2-D DWT is a series of low pass, high pass filtering and subsampling in both horizontal and vertical directions. The spatial domain data are transformed into the LL (horizontal low pass, vertical low pass), HL (horizontal high pass, vertical low pass), LH (horizontal low pass, vertical high pass) and HH (horizontal high pass, vertical high pass) sub-band signals.

Figure 2. Transform coding. (a) original Lena image (b) Lena image after \(8 \times 8\) DCT (c) Lena image after two-level DWT
in the frequency domain. In image coding, Mallat structure is usually adopted. That is, the LL sub-bands in each resolution can be further decomposed into four sub-bands. Figure 3 shows a 2-level 2-D DWT dataflow, and the result of a Lena image after the DWT of two-level dyadic decomposition is shown in Figure 2 (b). In JPEG 2000 Part 1, two filters are supported. The (5,3) filter is for lossless coding and the (9,7) filter is for lossy coding.

Figure 3. Two-level 2-D DWT. H(z): low-pass filter, G(z): high-pass filter

### 2.2.2 Quantization

Quantization is the main scheme to control the compression ratio. Lossless compression can only achieve limited compression ratio. By quantization, the range of compression ratio is widened, and can be adjusted by specifying different quantization extent.

In JPEG, 8x8 quantization matrices are used, and each entry of the quantization matrices can be specified by a user. The uniform quantizer of JPEG is defined as $Z_q(m,n) = \text{round}(Z(m,n) / Q(m,n))$, where $Z(m,n)$ is the DCT coefficients, $Q(m,n)$ is the quantizer step size, and $Z_q(m,n)$ is the quantized DCT coefficient, normalized by the quantizer step size. The dequantization is defined by $Z_{deq} = Z_q(m,n) \times Q(m,n)$. For JPEG 2000, a specific quantization step can be defined for each subband. In MPEG video coding, the quantization step size is chosen by the quantization parameter QP defined in standards. In H.264/AVC, 52 different QPs are supported, and when the QP increases by one, the required data rate will decrease approximately 12.5%.

Quantization is a lossy operation where some information is selectively discarded and cannot be recovered at the decoding side. Therefore, there will
be differences between the reconstructed image and the original one. The peak signal-to-noise ratio (PSNR) is a common index for objective quality evaluation. Quantization is based on rate-distortion model and HVS characteristics. Since human eyes are less sensitive to high frequency components, the quantization extent of higher frequency parts can be larger. In this case, the lost information is less apparent to human eyes.

2.2.3 **Entropy coding: Huffman coding and arithmetic coding**

Statistical redundancy can be removed by entropy coding. It is a lossless coding process based on the concept that more frequent symbols can be assigned shorter code words, and less frequent ones can be assigned longer code words. The average code length of the variable length coded data will therefore be shorter than fixed length codes. Huffman coding and arithmetic coding are the two main entropy coders used in image and video coding standards.

The implementation complexity of a Huffman coder is less than that of an arithmetic coder, while the compression performance of an arithmetic coder is usually better than a Huffman coder. In baseline JPEG [8] and MPEG-1/-2/-4, the Huffman coding is adopted. In JPEG, user-customized Huffman tables are supported, while in video coding, Huffman tables are fixed and predefined in the standards. In JPEG 2000 [9] and MPEG-4 Visual Texture Coding (VTC) tool, the binary arithmetic coding is adopted. The latest H.264/AVC standard supports both Huffman coding and Arithmetic coding as its coding tools. In baseline profile, context-based adaptive variable length coding (CAVLC) is supported, while in main profile, context-based adaptive binary arithmetic coding (CABAC) is adopted.

2.2.4 **Motion Estimation (ME) and Motion Compensation (MC)**

ME and MC are the most important techniques for the inter frame video coding to remove the temporal redundancy. They provide tens to hundreds more compression ratio compared with intra-only techniques. In a video sequence, the successive frames are similar since the time period between them is short. For a 30 frames per second video, the time differences between two frames are 1/30 second. The concept of ME and MC is to find a predictor in the reference frame(s) that can best predict the current frame data, and therefore, compensate the frame differences.

Block-matching ME is adopted in all video coding standards to find the best matched prediction data. A current frame is divided into macroblocks (MBs), and each MB in the current frame (current MB) is matched within the search range of the reference frame (Figure 4) by a matching criterion. The
sum of absolute differences (SAD) between a current MB and a reference MB is usually adopted as the matching criterion, which is defined by

$$SAD(k, p) = \sum_{i=1}^{N} \sum_{j=1}^{N} |cur(i, j) - ref(i + k, j + p)|,$$

where $N$ is the block size of a MB, $cur(i, j)$ is the pixel value in the current MB, $ref(i + k, j + p)$ is the pixel value in the reference block, the search range is $[-P_H, P_H]$ and $[-P_V, P_V]$ in the horizontal and vertical direction, and $(k, p)$ is the position of the search candidate (a reference block) in the search range, $-P_H \leq k < P_H$ and $-P_V \leq p < P_V$. After the search, the search candidate with the smallest SAD is selected as the best reference MB, and the associated MB position is the motion vector of this current MB. The motion vectors are variable length coded, and the prediction error (residue) between the current MB and the reference MB is coded by JPEG-like intra coding.

2.3 Standards

The standardization of image and video coding algorithms make data exchange easier. We have briefly described some basic compression techniques in the previous subsection, and there are actually more techniques than those basic techniques. A proprietary algorithm can be a combination of any basic component among them. Interoperability becomes an issue when we want to share the compressed data with others.

Interoperability of the coded data is a key issue of the product popularity and cost. Therefore, international organizations start to standardize image and video coding standards. In the digital image field, JPEG should be the best model of standardization. It is so successful and popular that current DSCs all support JPEG compression. As for the digital video field, the big
success of MPEG-2 is another good model. The DVD market is growing rapidly for the big entertainment requirement.

The advances of digital image and video coding standards keep going. The JPEG, MPEG and VCEG under ISO/IEC and ITU-T international organizations are the three groups consisting of many image and video experts who have long been devoted to the development of coding algorithms and standardizing them. Figure 5 shows the progress of some classical and state-of-the-art standards. Different standards focus on different applications. The trend is that the compression performance advances at the cost of higher complexity. Also, more features and functions are provided to fulfill the demands.

Figure 5. Advances of image and video coding standards.

Figure 6 shows the basic framework of image coding. Baseline JPEG [8] is a DCT and Huffman coding based coder, while JPEG 2000 [9] and MPEG-4 VTC is based on DWT and arithmetic coding. Figure 7 is the basic framework of a video coder. Besides the intra frame coding part (DCT, quantization and entropy coding), which is similar to a still image coder, the ME/MC is used for inter frame coding, and all this forms the hybrid coding architecture of most MPEG and H.26x standards. There is a decoder embedded in a video encoder, and a coding loop is formed in a video encoder. This is just a basic and simplified diagram. Different video coding standards have some specific features on some functional modules. Besides, in standards like H.264/AVC, there is an in-loop de-blocking filter.

The standard does not standardize everything. The scope of these image and video coding standards is only the detailed definition of the syntax and semantics of the bitstream and the decoding process. Standards still leave large room for the optimization of a codec design.
2.4 Characteristics of Image and Video Coding

The first step to design a good image/video codec is to understand the characteristics of image and video coding.

The standardized coding flows do not mean the standardized codec implementation. The design of a good image/video codec is not just a trivial mapping of standard algorithms to architectures but an optimization problem of timing, cost, power, etc., that requires many efforts. Besides the general IC design knowledge and techniques, we need to have an insight of the characteristics of the video data we need to process and the algorithms we are going to use. With deeper domain knowledge of image and video coding, designers can design better codec architectures.

Since an image or video codec has to process large raw data and compress them into smaller size, a codec itself also faces the large storage and bandwidth problem. For image encoding, the input is a huge amount of