

# Advanced Power MOSFET Concepts



B. Jayant Baliga

# Advanced Power MOSFET Concepts

 Springer

B. Jayant Baliga  
Department of Electrical and Computer  
Engineering  
North Carolina State University  
Raleigh NC 27695  
USA

ISBN 978-1-4419-5916-4 e-ISBN 978-1-4419-5917-1  
DOI 10.1007/978-1-4419-5917-1  
Springer New York Heidelberg Dordrecht London

Library of Congress Control Number: 2010929769

© Springer Science+Business Media, LLC 2010

All rights reserved. This work may not be translated or copied in whole or in part without the written permission of the publisher (Springer Science+Business Media, LLC, 233 Spring Street, New York, NY 10013, USA), except for brief excerpts in connection with reviews or scholarly analysis. Use in connection with any form of information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed is forbidden.

The use in this publication of trade names, trademarks, service marks, and similar terms, even if they are not identified as such, is not to be taken as an expression of opinion as to whether or not they are subject to proprietary rights.

Printed on acid-free paper

Springer is part of Springer Science+Business Media ([www.springer.com](http://www.springer.com))

# Dedication

*The author would like to dedicate this book to his wife, Pratima, for her unwavering support throughout his career devoted to the enhancement of the performance and understanding of power semiconductor devices.*



# Preface

With increased awareness of the adverse impact on the environment resulting from carbon emissions into the atmosphere, there is a growing demand for improving the efficiency of power electronic systems. Power semiconductor devices are recognized as a key component of all power electronic systems. It is estimated that at least 50 percent of the electricity used in the world is controlled by power devices. With the wide spread use of electronics in the consumer, industrial, medical, and transportation sectors, power devices have a major impact on the economy because they determine the cost and efficiency of systems. After the initial replacement of vacuum tubes by solid state devices in the 1950s, semiconductor power devices have taken a dominant role with silicon serving as the base material. These developments have been referred to as the *Second Electronic Revolution*.

In the 1970s, the power MOSFET product was first introduced by International Rectifier Corporation. Although initially hailed as a replacement for all bipolar power devices due to its high input impedance and fast switching speed, the silicon power MOSFET has successfully cornered the market for low voltage ( $<100$  V) and high switching speed ( $>100$  kHz) applications but failed to make serious inroads in the high voltage arena. This is because the on-state resistance of silicon power MOSFETs increases very rapidly with increase in the breakdown voltage. The resulting high conduction loss, even when using larger more expensive die, degrades the overall system efficiency.

The large on-state voltage drop for high voltage silicon power MOSFETs and the large drive current needed for silicon power bipolar transistors encouraged the development of the insulated gate bipolar transistor (IGBT) [1]. First commercialized in the early 1980s, the IGBT has become the dominant device used in all medium and high power electronic systems in the consumer, industrial, transportation, and military systems, and even found applications in the medical sector. The US Department of Energy has estimated that the implementation of IGBT-based variable speed drives for controlling motors is producing an energy savings of over 2 quadrillion btus per year, which is equivalent to 70 Giga-Watts of power. This energy savings eliminates the need for generating electricity from 70 coal-fired

power-plants resulting in reducing carbon dioxide emissions by over one-Trillion pounds each year.

With on-going investments in renewable energy sources such as wind and solar power that utilize power semiconductor device in inverters, it is anticipated that there will be an increasing need for technologists trained in the discipline of designing and manufacturing power semiconductor devices. My recently published textbook [2] provides a comprehensive analysis of the basic power rectifier and transistor structures. This textbook has been complemented with a monograph on “Advanced Power Rectifier Concepts” to familiarize students and engineering professionals with structures that exhibit improved performance attributes.

This monograph introduces the reader to advanced power MOSFET concepts that enable improvement of performance of these transistor structures. For the convenience of readers, analysis of the basic transistor structures, with the same voltage ratings as the novel device structures, have been included in the monograph to enable comparison of the performance. As in the case of the textbook, analytical expressions that describe the behavior of the advanced power MOSFET structures have been rigorously derived using the fundamental semiconductor Poisson’s, continuity, and conduction equations in this monograph. The electrical characteristics of all the power MOSFETs discussed in this book can be computed using these analytical solutions as shown by typical examples provided in each section. In order to corroborate the validity of these analytical formulations, I have included the results of two-dimensional numerical simulations in each section of the book. The simulation results are also used to further elucidate the physics and point out two-dimensional effects whenever relevant. Due to increasing interest in the utilization of wide band-gap semiconductors for power devices, the book includes the analysis of silicon carbide structures.

In the first chapter, a broad introduction to potential applications for power devices is provided. The electrical characteristics for ideal power MOSFETs are then defined and compared with those for typical devices. The second and third chapters provide analyses of the planar DMOSFET structure and the trench-gate UMOSFET structure with 30-V blocking capability, which can be used as a benchmark for understanding the improvements achieved using the advanced device concepts. The analysis includes the on-resistance, the input capacitance, the gate charge, and the output characteristics.

The next four chapters are devoted to various advanced power MOSFET structures that allow improvement in the performance of devices with 30-V blocking capability. The fourth chapter discusses on the “Shielded Channel Planar Power MOSFET” structure, which allows a significant reduction in the gate charge while achieving a specific on-resistance close to that of the UMOSFET structure. The fifth chapter discusses the power CC-MOSFET structure, which utilizes the two-dimensional charge coupling effect to reduce the specific on-resistance by an order of magnitude. This structure is favorable for use as a synchronous rectifier in the sync-buck circuit topology used in voltage regulator modules for providing power to microprocessors in computers.



The next two chapters are devoted to high-voltage silicon device structures that utilize the charge-coupling concept to reduce the resistance of the drift region. In chapter six, the charge-coupling phenomenon is accomplished by using a graded doping profile in conjunction with an electrode embedded in an oxide coated trench to create the power GD-MOSFET structure. In chapter seven, the charge-coupling phenomenon is accomplished with adjacent p-type and n-type layers in the drift region to create the power SJ-MOSFET structure.

Chapter eight provides a detailed discussion of the body-diode within the various silicon power MOSFET structures. The body-diode can be used in place of the fly-back rectifier utilized in the H-bridge circuit commonly used for motor control applications. It is demonstrated in this chapter that the judicious utilization of a Schottky contact within the power MOSFET cell structure can greatly improve the reverse recovery behavior of the body-diode.

Improvement in the performance of high voltage power MOSFET structures can also be achieved by replacing silicon with silicon carbide as the base material [3]. The much larger breakdown field strength for 4H-SiC allows increasing the doping concentration in the drift region by a factor of 200-times while shrinking the thickness of the drift region by one-order of magnitude. However, the silicon power MOSFET structure must be modified to shield the gate oxide from the much larger electric fields prevalent in silicon carbide to avoid rupture. In addition, the base region must be shielded to avoid reach-through breakdown. The on-resistance of these devices becomes limited by the channel resistance.

The final chapter provides a comparison of all the power MOSFET structures discussed in this book. The devices are first compared for the 30-V rating suitable for VRM applications and then with the 600-V rating suitable for motor control applications. In addition, the performance of all the devices is compared over a wide range of blocking voltages to provide a broader view.

I am hopeful that this monograph will be useful for researchers in academia and to product designers in the industry. It can also be used for the teaching of courses on solid state devices as a supplement to my textbook [2].

December, 2009  
Raleigh, NC

B. Jayant Baliga

## References

1. B.J. Baliga, "How the Super-Transistor Works", Scientific American Magazine, Special Issue on 'The Solid-State-Century', pp. 34–41, January 22, 1988.
2. B.J. Baliga, "Fundamentals of Power Semiconductor Devices", Springer Scientific, New York, 2008.
3. B.J. Baliga, "Silicon Carbide Power Devices", World Scientific Press, Singapore, 2006.



# Contents

<b>1</b>	<b>Introduction</b>	1
1.1	Ideal Power Switching Waveforms	2
1.2	Ideal and Typical Power MOSFET Characteristics	3
1.3	Typical Power MOSFET Structures	5
1.4	Ideal Drift Region for Unipolar Power Devices	6
1.5	Charge-Coupled Structures: Ideal Specific On-Resistance	8
1.6	Revised Breakdown Models for Silicon	12
1.7	Typical Power MOSFET Applications	18
1.7.1	DC-DC Sync-Buck Converter	18
1.7.2	Variable-Frequency Motor Drive	19
1.8	Summary	21
	References	21
<b>2</b>	<b>D-MOSFET Structure</b>	23
2.1	The D-MOSFET Structure	23
2.2	Power D-MOSFET On-Resistance	25
2.2.1	Channel Resistance	28
2.2.2	Accumulation Resistance	29
2.2.3	JFET Resistance	29
2.2.4	Drift Region Resistance	31
2.2.5	N <sup>+</sup> Substrate Resistance	32
2.2.6	Drain and Source Contact Resistance	32
2.2.7	Total On-Resistance	33
2.3	Blocking Voltage	37
2.3.1	Impact of Edge Termination	38
2.3.2	Impact of Graded Doping Profile	39
2.4	Output Characteristics	44
2.4.1	Simulation Example	45
2.5	Device Capacitances	46
2.5.1	Simulation Example	49

2.6	Gate Charge .....	51
2.6.1	Simulation Example .....	52
2.7	Device Figures of Merit .....	54
2.8	Discussion .....	56
	References .....	61
<b>3</b>	<b>U-MOSFET Structure .....</b>	<b>63</b>
3.1	The U-MOSFET Structure .....	63
3.2	Power U-MOSFET On-Resistance .....	66
3.2.1	Channel Resistance .....	67
3.2.2	Accumulation Resistance .....	68
3.2.3	Drift Region Resistance .....	68
3.2.4	Total On-Resistance .....	69
3.3	Blocking Voltage .....	73
3.3.1	Impact of Edge Termination .....	74
3.3.2	Impact of Graded Doping Profile .....	74
3.4	Output Characteristics .....	80
3.4.1	Simulation Example .....	80
3.5	Device Capacitances .....	81
3.5.1	Simulation Example .....	84
3.6	Gate Charge .....	86
3.6.1	Simulation Example .....	88
3.7	Device Figures of Merit .....	90
3.8	Thick Trench Bottom Oxide Structure .....	92
3.8.1	On-Resistance .....	92
3.8.2	Reverse Transfer Capacitance .....	92
3.8.3	Gate Charge .....	94
3.8.4	Device Figures-of-Merit .....	95
3.9	High Voltage Devices .....	101
3.9.1	Simulation Results .....	101
3.10	Inductive Load Turn-Off Characteristics .....	106
3.10.1	Simulation Results .....	111
3.11	Discussion .....	112
	References .....	117
<b>4</b>	<b>SC-MOSFET Structure .....</b>	<b>119</b>
4.1	The SC-MOSFET Structure .....	120
4.2	Power SC-MOSFET On-Resistance .....	122
4.2.1	Channel Resistance .....	124
4.2.2	Accumulation Resistance .....	124
4.2.3	JFET Resistance .....	125
4.2.4	Drift Region Resistance .....	126
4.2.5	Total On-Resistance .....	127

4.3	Blocking Voltage	133
4.3.1	Impact of Edge Termination	133
4.4	Output Characteristics	138
4.4.1	Simulation Example	139
4.5	Device Capacitances	139
4.5.1	Simulation Example	144
4.6	Gate Charge	147
4.6.1	Simulation Example	149
4.7	Device Figures of Merit	151
4.8	Discussion	153
	References	158
<b>5</b>	<b>CC-MOSFET Structure</b>	<b>159</b>
5.1	The CC-MOSFET Structure	160
5.2	Charge-Coupling Physics and Blocking Voltage	162
5.2.1	Simulation Results	173
5.3	Power CC-MOSFET On-Resistance	186
5.3.1	Channel Resistance	187
5.3.2	Accumulation Resistance for Current Spreading Region	188
5.3.3	Drift Region Resistance	189
5.3.4	Total On-Resistance	190
5.4	Output Characteristics	195
5.4.1	Simulation Example	195
5.5	Device Capacitances	196
5.5.1	Simulation Example	206
5.6	Gate Charge	209
5.6.1	Simulation Example	214
5.7	Device Figures of Merit	217
5.8	Edge Termination	220
5.8.1	Simulation Example	222
5.9	High Voltage Devices	224
5.9.1	Simulation Results	224
5.10	Process Sensitivity Analysis	232
5.11	Discussion	235
	References	239
<b>6</b>	<b>GD-MOSFET Structure</b>	<b>241</b>
6.1	The GD-MOSFET Structure	242
6.2	Charge-Coupling Physics and Blocking Voltage	244
6.2.1	Simulation Results	250
6.3	Power GD-MOSFET On-Resistance	263
6.3.1	Channel Resistance	265
6.3.2	Accumulation Resistance for Current Spreading Region	266

6.3.3	Drift Region Resistance	266
6.3.4	Total On-Resistance	268
6.4	Output Characteristics	271
6.4.1	Simulation Example	272
6.5	Device Capacitances	273
6.5.1	Simulation Example	276
6.6	Gate Charge	278
6.6.1	Simulation Example	280
6.7	Device Figures of Merit	283
6.8	Edge Termination	285
6.9	High Voltage Devices	285
6.9.1	Simulation Results	286
6.10	Process Sensitivity Analysis	306
6.11	Inductive Load Turn-Off Characteristics	310
6.11.1	Simulation Results	315
6.12	Discussion	317
	References	322
<b>7</b>	<b>SJ-MOSFET Structure</b>	<b>323</b>
7.1	The SJ-MOSFET Structure	324
7.2	Charge-Coupling Physics	326
7.2.1	Simulation Results	329
7.3	Power SJ-MOSFET On-Resistance	346
7.3.1	Channel Resistance	350
7.3.2	Accumulation Resistance for Current Spreading Region	351
7.3.3	Drift Region Resistance	351
7.3.4	Total On-Resistance	353
7.4	Output Characteristics	357
7.4.1	Simulation Example	357
7.5	Device Capacitances	357
7.5.1	Simulation Example	364
7.6	Gate Charge	367
7.6.1	Simulation Example	369
7.7	Device Figures of Merit	371
7.8	Edge Termination	373
7.8.1	Simulation Example	374
7.9	High Voltage Devices	378
7.9.1	Simulation Results	378
7.10	Process Sensitivity Analysis	381
7.11	Inductive Load Turn-Off Characteristics	385
7.11.1	Simulation Results	389
7.12	Discussion	391
	References	396

<b>8</b>	<b>Integral Diode</b>	399
8.1	Power MOSFET Body Diode	400
8.2	Computer Power Supplies	400
8.2.1	Power U–MOSFET Structure	402
8.2.2	Power CC–MOSFET Structure	407
8.2.3	Power JBSFET Structure	412
8.3	Motor Control Application	424
8.3.1	Power U–MOSFET Structure	425
8.3.2	Power JBSFET Structure	430
8.3.3	Power GD–MOSFET Structure	437
8.3.4	Power GD–JBSFET Structure	443
8.3.5	Power SJ–MOSFET Structure	461
8.3.6	Power SJ–JBSFET Structure	467
8.4	Discussion	472
8.4.1	Low–Voltage Devices	473
8.4.2	High–Voltage Devices	474
	References	476
<b>9</b>	<b>SiC Planar MOSFET Structures</b>	477
9.1	Shielded Planar Inversion-Mode MOSFET Structure	478
9.1.1	Blocking Mode	479
9.1.2	Threshold Voltage	484
9.1.3	On–State Resistance	486
9.1.4	Capacitances	493
9.1.5	Gate Charge	496
9.1.6	Device Figures of Merit	498
9.1.7	Inductive Load Turn-Off Characteristics	499
9.1.8	Body-Diode Characteristics	503
9.2	Shielded Planar ACCUFET Structure	504
9.2.1	Blocking Mode	505
9.2.2	Threshold Voltage	510
9.2.3	On–State Resistance	512
9.2.4	Capacitances	517
9.2.5	Gate Charge	519
9.2.6	Device Figures of Merit	522
9.2.7	Inductive Load Turn-Off Characteristics	523
9.2.8	Body–Diode Characteristics	527
9.3	Discussion	531
	References	533
<b>10</b>	<b>Synopsis</b>	535
10.1	Computer Power Supplies	536
10.1.1	Inadvertent Turn–On Suppression	537
10.1.2	Device Active Area	539

10.1.3 Switching Power Losses .....	540
10.1.4 Input Capacitance .....	540
10.1.5 Device Comparison .....	540
10.2 High Voltage Motor Control .....	543
10.3 Device Comparison .....	549
10.4 Summary .....	552
References .....	552
<b>About the Author</b> .....	<b>553</b>
<b>Index</b> .....	<b>557</b>



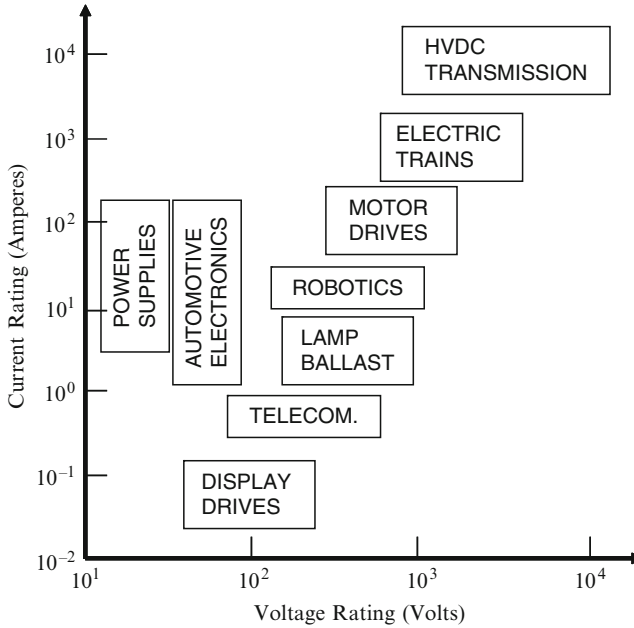
# Chapter 1

## Introduction

Power devices are required for applications that operate over a broad spectrum of power levels as shown in Fig. 1.1 [1]. Based up on this figure, the applications can be broken down into several categories. The first category is applications that require low operating current (typically less than 1 A) levels. These applications, such as display drives, usually require a large number of transistors that must be capable of blocking up to 300 V. The small size of the low-current transistors allows their integration on a single chip with control circuits to provide a cost-effective solution.

The second category is applications where the operating voltage of the power circuit is relatively small ( $<100$  V). Typical examples are automotive electronics and power supplies used in desktop computers and laptops. Silicon power MOSFET structures offer the best performance for these applications because of their low on-resistance and fast switching speed. This monograph describes a variety of power MOSFET structures that enable enhancement in their operating characteristics.

The third category is applications with high operating voltages (above 200 V). Typical examples are lamp ballasts, consumer appliances that utilize motors, and electric vehicle drives. The on-resistance of conventional silicon power MOSFET structures is too large to serve these applications. Consequently, these applications utilize silicon insulated gate bipolar transistors (IGBTs). The silicon IGBT combines the physics of the MOSFET structure with the physics of the bipolar transistor structure. Although the silicon IGBT has become ubiquitous for high voltage power electronic applications, silicon power MOSFETs that utilize two-dimensional charge coupling can be competitive with silicon IGBTs as shown in this monograph. In addition, power MOSFET structures built using silicon carbide as the base material have been shown to exhibit very promising characteristics for applications that require blocking voltages of up to 5,000 V [2]. Consequently, this monograph includes the discussion of the power MOSFET structures that are specially configured to obtain a high performance from silicon carbide.

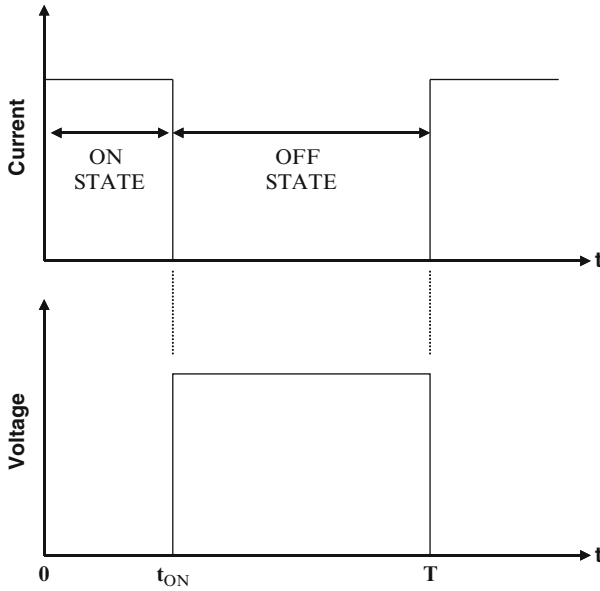


**Fig. 1.1** Applications for power devices

## 1.1 Ideal Power Switching Waveforms

An ideal power device must be capable of controlling the flow of power to loads with zero power dissipation. The loads encountered in systems may be inductive in nature (such as motors and solenoids), resistive in nature (such as heaters and lamp filaments), or capacitive in nature (such as transducers and LCD displays). Most often, the power delivered to a load is controlled by turning-on a power switch on a periodic basis to generate pulses of current that can be regulated by a control circuit. The ideal waveforms for the power delivered through a power switch are shown in Fig. 1.2. During each switching cycle, the switch remains on for a time up to  $t_{ON}$  and maintains an off-state for the remainder of the period  $T$ . This produces pulses of current that flow through the circuit as controlled by the turning-on of power switches. For an ideal power switch, the voltage drop during the on-state is zero resulting in no power dissipation. Similarly, during the off-state, the (leakage) current in the ideal power switch is zero resulting in no power dissipation. In addition, it is assumed that the ideal power switch makes the transition between the on-state and off-state instantaneously resulting in no power loss as well.

Typical power MOSFET structures exhibit a finite voltage drop in the on-state and leakage current flow in the off-state. In addition, the power MOSFET structure exhibits power losses during the turn-on and turn-off transients. These power losses are related to their large terminal capacitances which must be charged



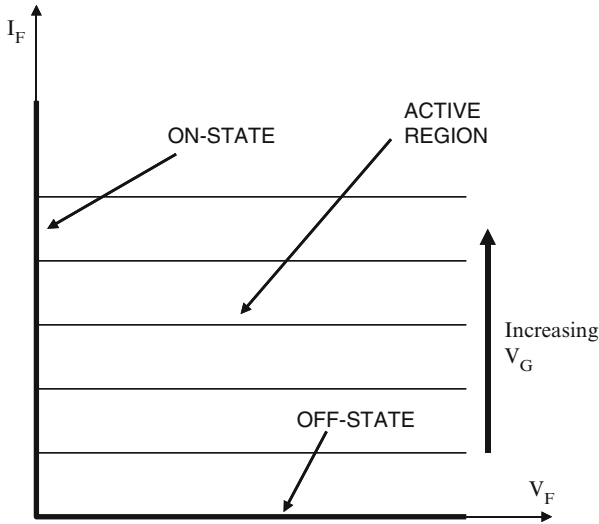
**Fig. 1.2** Ideal switching waveforms for power delivery

and discharged during each operating cycle. The novel power MOSFET structures that are discussed in this monograph were created to reduce the on-resistance and capacitance.

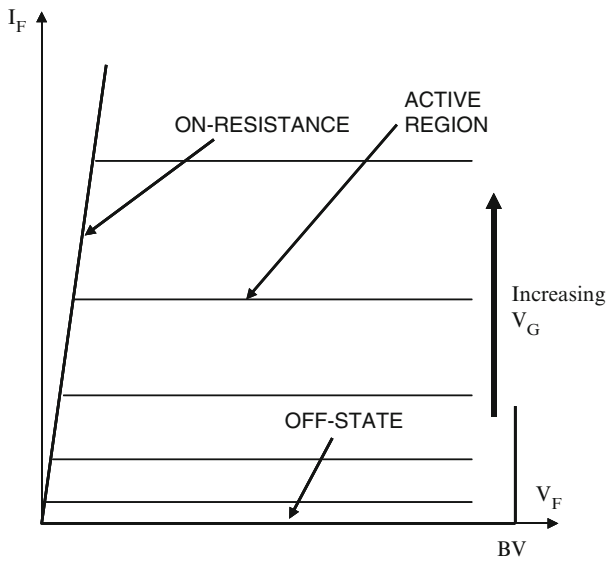
## 1.2 Ideal and Typical Power MOSFET Characteristics

The  $i-v$  characteristics of an ideal power switch are illustrated in Fig. 1.3. The ideal transistor conducts current in the on-state with zero voltage drop and blocks voltage in the off-state with zero leakage current. In addition, the ideal device can operate with a high current and voltage in the active region with the saturated forward current in this mode controlled by the applied gate bias. The spacing between the characteristics in the active region is uniform for an ideal transistor indicating a gain (transconductance) that is independent of the forward current and voltage.

The  $i-v$  characteristics of a typical power MOSFET structure are illustrated in Fig. 1.4. This device exhibits a finite resistance when carrying current in the on-state as well as a finite leakage current while operating in the off-state (not shown in the figure because its value is much lower than the on-state current levels). The breakdown voltage of a typical transistor is also finite as indicated in the figure with ‘BV’. The typical transistor can operate with a high current and voltage in the active region. This current is determined by a gate voltage for a MOSFET as indicated in the figure. It is desirable to have gate voltage controlled characteristics because the



**Fig. 1.3** Characteristics of an ideal power switch



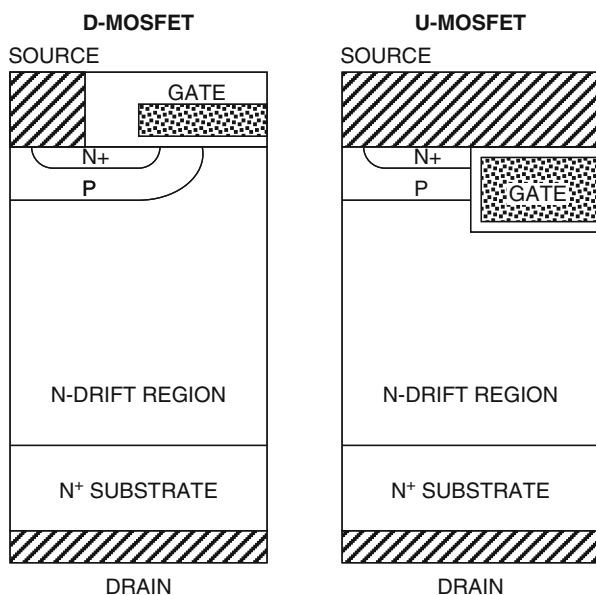
**Fig. 1.4** Characteristics of a typical power MOSFET structure

drive circuit can be integrated to reduce its cost. The spacing between the characteristics in the active region is non-uniform for a typical MOSFET with a square-law behavior for devices operating with channel pinch-off in the current saturation mode. Recently, devices operating under a new super-linear mode have been proposed and demonstrated for wireless base-station applications [3]. These devices

exhibit an equal spacing between the saturated drain current characteristics as the gate voltage is increased. This is an ideal behavior when the transistor is used for the amplification of audio, video or cellular signals because it eliminates signal distortion that occurs with the characteristics shown in Fig. 1.4.

### 1.3 Typical Power MOSFET Structures

The most commonly used unipolar power transistor is the silicon power Metal-Oxide-Semiconductor Field-Effect-Transistor or MOSFET. Although other structures, such as JFETs or SITs have been explored [4], they have not been popular for power electronic applications because of their normally-on behavior. The commercially available silicon power MOSFETs are based upon the structures shown in Fig. 1.5. The D-MOSFET was first commercially introduced in the 1970s and contains a ‘planar-gate’ structure. The P-base region and the  $N^+$  source regions are self-aligned to the edge of the polysilicon gate electrode by using ion-implantation of boron and phosphorus followed by their respective drive-in thermal cycles. The n-type channel is defined by the difference in the lateral extension of the junctions under the gate electrode. The device supports positive voltage applied to the drain across the P-base/N-drift region junction. The voltage blocking capability is determined by the doping and thickness of the N-drift region. Although low voltage silicon power MOSFETs have small on-resistances, the drift region resistance increases rapidly with



**Fig. 1.5** Typical silicon power MOSFET structures

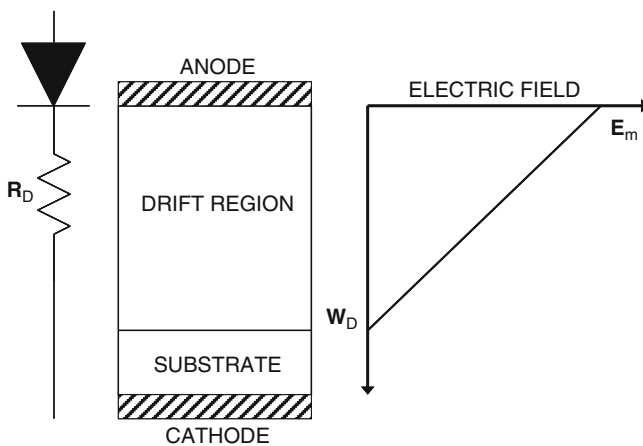
increasing blocking voltage limiting the performance of silicon power D-MOSFETs to below 200 V.

The silicon U-MOSFET structure became commercially available in the 1990s. It has a gate structure embedded within a trench etched into the silicon surface. The N-type channel is formed on the side-wall of the trench at the surface of the P-base region. The channel length is determined by the difference in vertical extension of the P-base and  $N^+$  source regions as controlled by the ion-implant energies and drive times for the dopants. The silicon U-MOSFET structure was developed to reduce the on-state resistance by elimination of the JFET component within the D-MOSFET structure.

## 1.4 Ideal Drift Region for Unipolar Power Devices

The power MOSFET structures discussed above contain a drift region which is designed to support the blocking voltage. The properties (doping concentration and thickness) of the *ideal drift region* can be analyzed by assuming an abrupt junction profile with high doping concentration on one side and a low uniform doping concentration on the other side, while neglecting any junction curvature effects by assuming a parallel-plane configuration. The resistance of the ideal drift region can then be related to the basic properties of the semiconductor material [5].

A Schottky rectifier structure is illustrated in Fig. 1.6. The solution of Poisson's equation in the voltage blocking mode leads to a triangular electric field distribution, as shown in Fig. 1.6, within a uniformly doped drift region with the slope of the field profile being determined by the doping concentration. The same behavior for the electric field profile occurs in the vertical power MOSFET structures as well. The maximum voltage that can be supported by the drift region is determined by the



**Fig. 1.6** The ideal drift region and its electric field distribution

maximum electric field ( $E_m$ ) reaching the critical electric field ( $E_c$ ) for breakdown for the semiconductor material. The critical electric field for breakdown and the doping concentration then determine the maximum depletion width ( $W_D$ ).

The specific resistance (resistance per unit area) of the ideal drift region is given by:

$$R_{on.sp} = \left( \frac{W_D}{q\mu_n N_D} \right) \quad (1.1)$$

where  $N_D$  is the doping concentration of the drift region. Since this resistance was initially considered to be the lowest value achievable with silicon devices, it has historically been referred to as the *ideal specific on-resistance of the drift region*. More recent introduction of the charge-coupling concept, described later in this chapter, has enabled reducing the drift region resistance of silicon devices to below the values predicted by this equation. The depletion width under breakdown conditions is given by:

$$W_D = \frac{2BV}{E_C} \quad (1.2)$$

where  $BV$  is the desired breakdown voltage. The doping concentration in the drift region required to obtain this breakdown voltage is given by:

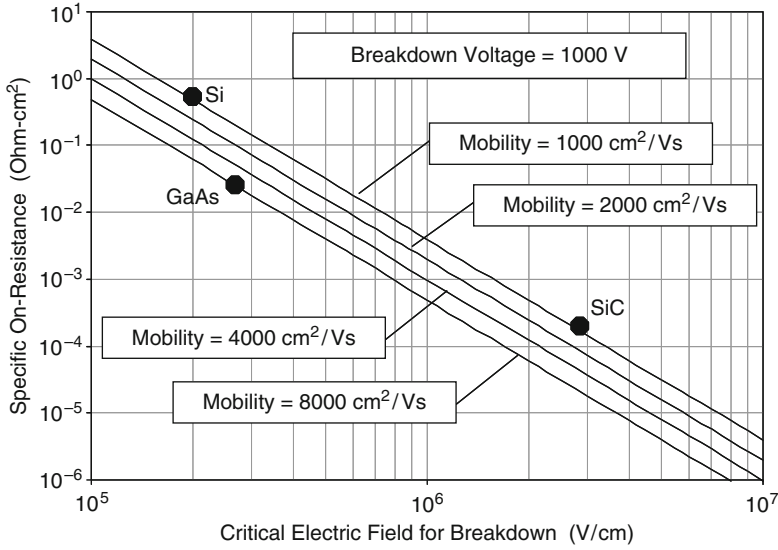
$$N_D = \frac{\epsilon_s E_C^2}{2qBV} \quad (1.3)$$

Combining these relationships, the specific resistance of the ideal drift region is obtained:

$$R_{on-ideal} = \frac{4BV^2}{\epsilon_s \mu_n E_C^3} \quad (1.4)$$

The denominator of (1.4) ( $\epsilon_s \mu_n E_C^3$ ) is commonly referred to as *Baliga's Figure of Merit for Power Devices*. It is an indicator of the impact of the semiconductor material properties on the resistance of the drift region. The dependence of the drift region resistance on the mobility (assumed to be for electrons here because in general they have higher mobility values than for holes) of the carriers favors semiconductors such as Gallium Arsenide. However, the much stronger (cubic) dependence of the on-resistance on the critical electric field for breakdown favors wide band gap semiconductors such as silicon carbide [2]. The critical electric field for breakdown is determined by the impact ionization coefficients for holes and electrons in semiconductors.

As an example, the change in the specific on-resistance for the drift region with critical electric field and mobility is shown in Fig. 1.7 for the case of a breakdown



**Fig. 1.7** Specific on-resistance of the *ideal drift region*

voltage of 1,000 V. The location of the properties for silicon, gallium arsenide, and silicon carbide are shown in the figure by the points. The improvement in drift region resistance for GaAs in comparison with silicon is largely due to its much greater mobility for electrons. The improvement in drift region resistance for SiC in comparison with silicon is largely due to its much larger critical electric field for breakdown. Based upon these considerations, excellent high voltage Schottky rectifiers were developed from GaAs in the 1980s [6] and from silicon carbide in the 1990s [7]. Interest in the development of power devices from wide-band-gap semiconductors, including silicon carbide and gallium nitride, continues to grow.

## 1.5 Charge-Coupled Structures: Ideal Specific On-Resistance

The depletion region extends in one-dimension from a junction or Schottky contact during the blocking mode for the conventional structure discussed in the previous section. In the charge coupled structure, the voltage blocking capability is enhanced by the extension of depletion layers in two-dimensions. This effect is created by the formation of a horizontal Schottky contact on the top surface as illustrated in Fig. 1.18 which promotes the extension of a depletion region along the vertical or y-direction. Concurrently, the presence of the vertical P-N junction created by the alternate N and P-type regions promotes the extension of a depletion region along the horizontal or x-direction. These depletion regions conspire to produce a two-dimensional charge coupling in the N-drift region



which alters the electric field profile. A similar phenomenon can be induced in the case of power MOSFET structures under the P-base region as discussed later in this monograph.

The optimization of the charge coupled structure requires proper choice of the doping concentration and thickness of the N and P-type regions. It has been found that the highest breakdown voltage occurs when the charge in these regions is given by:

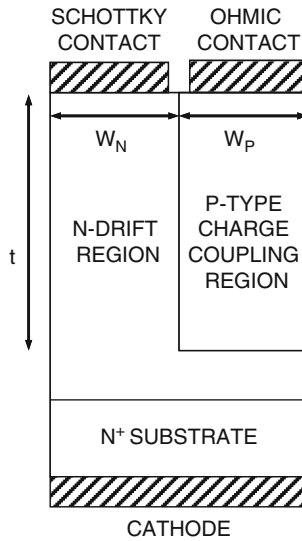
$$Q_{\text{optimum}} = 2qN_D W_N = \epsilon_s E_C \quad (1.5)$$

where  $q$  is the charge of an electron ( $1.6 \times 10^{-19}$  C),  $N_D$  is the doping concentration of the N-Type drift region,  $W_N$  is the width of the N-type drift region as shown in Fig. 1.8,  $\epsilon_s$  is the dielectric constant of the semiconductor, and  $E_C$  is the critical electric field for breakdown in the semiconductor. For silicon, the optimum charge is found to be  $3.11 \times 10^{-7}$  C/cm<sup>2</sup> based upon a critical electric field of  $3 \times 10^5$  V/cm. The optimum charge is often represented as a dopant density per unit area, in which case it takes a value of about  $2 \times 10^{12}$ /cm<sup>2</sup> for silicon. A slightly lower value for the doping concentration in the drift region may be warranted as discussed later in this section of the chapter.

The specific on-resistance for the drift region in the charge coupled structures is given by:

$$R_{D,sp} = \rho_D t \left( \frac{p}{W_N} \right) \quad (1.6)$$

where  $\rho_D$  is the resistivity of the N-type drift region,  $t$  is the trench depth and  $p$  is the cell pitch. Here, the uniform electric field is assumed to be produced only along the



**Fig. 1.8** Basic charge coupled Schottky diode structure

trench where the charge coupling occurs and the resistance of the remaining portion of the N-drift region is neglected. Using the relationship between the resistivity and the doping concentration, this equation can be written as:

$$R_{D,sp} = \frac{tp}{q \mu_N N_D W_N} \quad (1.7)$$

Combining this expression with (1.5):

$$R_{D,sp} = \frac{2tp}{\mu_N Q_{optimum}} \quad (1.8)$$

If the electric field along the trench, at the on-set of breakdown in the charge coupled device structure, is assumed to be uniform at a value equal to the critical electric field of the semiconductor:

$$t = \frac{BV}{E_C} \quad (1.9)$$

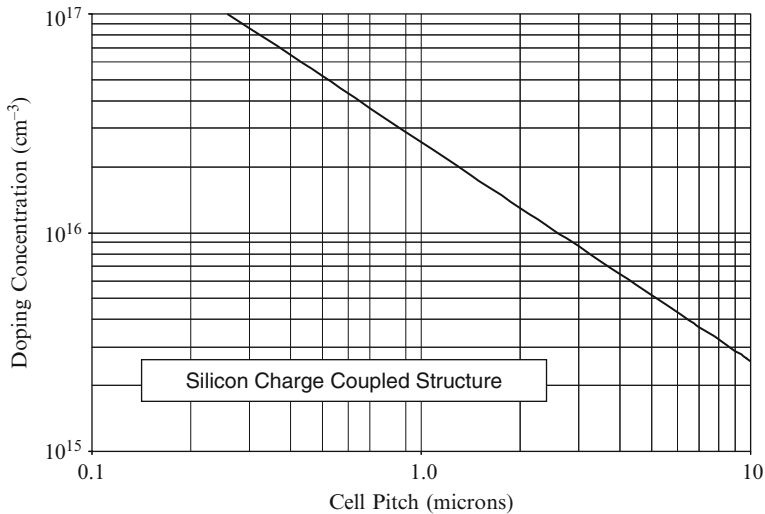
Using this expression, as well as the second part of (1.5), in (1.8) yields:

$$R_{D,sp} = \frac{2BVp}{\mu_N \epsilon_S E_C^2} \quad (1.10)$$

This is a fundamental expression for the *ideal specific on-resistance of vertical charge coupled devices*. By comparison of this expression with that for the one dimensional case (see 1.4), it can be observed that the specific on-resistance for the charge coupled devices increases linearly with the breakdown voltage unlike the more rapid quadratic rate for the conventional drift region. In addition, it is worth pointing out that the specific on-resistance for the drift region in the charge coupled structure can be reduced by decreasing the pitch. This occurs because the doping concentration in the drift region increases when the pitch is reduced in order to maintain the same optimum charge. The larger doping concentration reduces the resistivity and hence the specific on-resistance.

However, the analysis of the specific on-resistance for the drift region in charge coupled device structures must be tempered by several considerations. Firstly, it must be recognized that the mobility will become smaller when the doping concentration becomes larger. Secondly, the critical electric field for breakdown becomes smaller for the charge coupled structures because the high electric field in the drift region extends over a larger distance producing enhanced impact ionization. If a critical electric field for breakdown in the drift region for charge coupled structures is reduced to  $2 \times 10^5$  V/cm, an optimum charge of  $2.07 \times 10^{-7}$  C/cm<sup>2</sup>, with a corresponding dopant density of about  $1.3 \times 10^{12}$ /cm<sup>2</sup>, is more appropriate for silicon.

In designing the drift region for charge coupled structures, it is important to recognize that, unlike in the conventional one-dimensional case, the doping concentration of the drift region is dictated by the cell pitch and not the breakdown

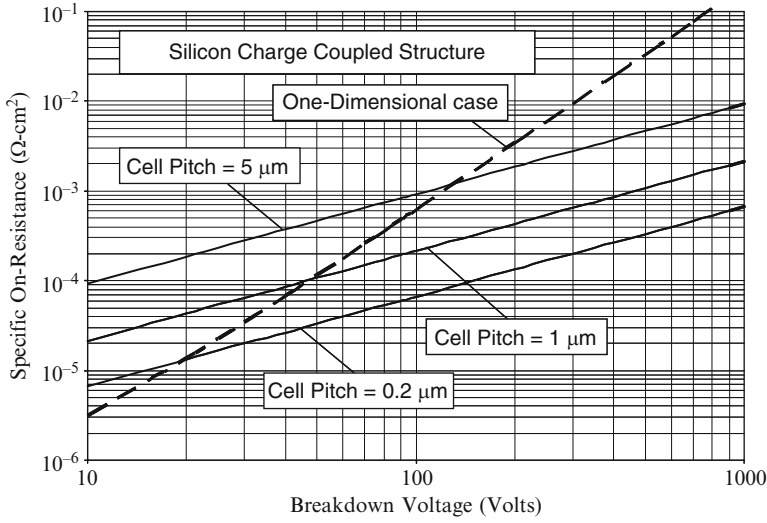


**Fig. 1.9** Drift region doping concentration for the charge coupled structure

voltage. The breakdown voltage in the charge coupled structure is determined solely by the depth of the trench used to provide the charge coupling effect and is independent of the doping concentration of the N-drift region. In the case of silicon charge coupled devices, the doping concentration for the N-type drift region is provided in Fig. 1.9 for the case of equal widths for the N-type and P-type charge coupling regions. For a typical cell pitch of 1  $\mu\text{m}$ , the doping concentration in the N-type drift region is about  $2.5 \times 10^{16}/\text{cm}^3$  when a critical electric field of  $2 \times 10^5$  V/cm is assumed.

It is interesting to compare the ideal specific on-resistance for the drift region in the silicon charge coupled structures to that for the one-dimensional parallel-plane case. This comparison is done in Fig. 1.10 using three values for the cell pitch in the case of the charge coupled structures. The doping concentration in the N-drift region increases when the cell pitch is reduced from 5 to 0.2  $\mu\text{m}$ , as already shown in Fig. 1.9, leading to a decrease in the specific on-resistance. The resulting reduction of the mobility with increasing doping concentration was included during the calculation of the specific on-resistance in Fig. 1.10. There is a cross-over in the specific on-resistance for the two types of structures. For the cell pitch of 1  $\mu\text{m}$ , the cross-over occurs at a breakdown voltage of about 50 V. The cross-over moves to a breakdown voltage of about 130 V when the cell pitch is increased to 5  $\mu\text{m}$ , and to about 20 V if a smaller cell pitch of 0.2  $\mu\text{m}$  is used. Consequently, the charge coupled structure is more attractive for reducing the specific on-resistance when the cell pitch is smaller. This entails a more complex process technology with higher attendant costs.

As a particular example, consider the case of silicon devices designed to support 200 V. In the case of the conventional structure with a one-dimensional junction,



**Fig. 1.10** Ideal specific on-resistance for the charge coupled structure. (solid lines: charge coupled structures; dashed line: one dimensional case)

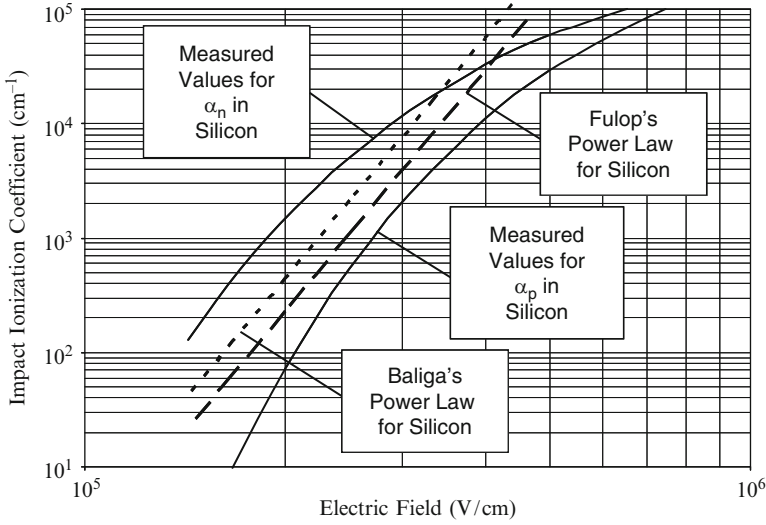
the specific on-resistance of the drift region is found to be  $3.4 \text{ m}\Omega \text{ cm}^2$  if a critical electric field for breakdown of  $3 \times 10^5 \text{ V/cm}$  is used. In contrast, the specific on-resistance for the drift region of the charge coupled structure with a cell pitch of  $1 \mu\text{m}$  is found to be only  $0.43 \text{ m}\Omega \text{ cm}^2$  if a critical electric field for breakdown of  $2 \times 10^5 \text{ V/cm}$  is used. In this calculation, a bulk mobility of  $1,120 \text{ cm}^2/\text{V s}$  was used corresponding to a doping concentration of  $2.6 \times 10^{16}/\text{cm}^3$  in the N-type portion of the drift region. In this example, the drift region for the charge coupled structure would have a thickness of  $10 \mu\text{m}$  when compared with  $12.5 \mu\text{m}$  needed in the conventional structure.

## 1.6 Revised Breakdown Models for Silicon

In the textbook [1], the breakdown voltage for silicon devices was analyzed by using the Fulop's power law relating the impact ionization coefficient to the electric field. The Fulop's power law [8] for impact ionization in silicon is given by:

$$\alpha_B(\text{Si}) = 1.80 \times 10^{-35} E^7 \quad (1.11)$$

The values for the impact ionization coefficient obtained by using this equation are compared with the impact ionization coefficients measured for electrons and holes in silicon [9] as represented by Chynoweth's equation in Fig. 1.11. It can be observed that Fulop's power law falls between that for electrons and holes and



**Fig. 1.11** Impact ionization coefficients for silicon

consequently underestimates the values for the impact ionization coefficients for electrons. This results in the prediction of larger breakdown voltages than in actual devices when performing the analytical calculations as pointed out in the textbook.

A better prediction of breakdown in silicon devices using analytical models can be achieved by improving the match between the power law and the measured data for impact ionization coefficients for electrons and holes in silicon. The proposed Baliga's power law for impact ionization in silicon is given by:

$$\alpha_B(\text{Si}) = 3.507 \times 10^{-35} E^7 \quad (1.12)$$

From Fig. 1.11, it can be observed that this equation provides a larger value for the impact ionization coefficients which will result in reducing the breakdown voltage.

In the case of one-dimensional parallel-plane junctions discussed in Chap. 3 of the textbook, the electric field takes a triangular distribution in the lightly doped side of the P-N junction given by:

$$E(x) = -\frac{qN_D}{\epsilon_S}(W_D - x) \quad (1.13)$$

where  $W_D$  is the depletion layer width, and  $N_D$  is the doping concentration on the lightly doped side of the junction. The breakdown voltage in this case is determined by the ionization integral becoming equal to unity:

$$\int_0^{W_D} \alpha dx = 1 \quad (1.14)$$

Substituting (1.12) into the above equation with the distribution given by (1.13), an expression for the depletion layer width at breakdown can be obtained:

$$W_{PP,B}(\text{Si}) = 2.404 \times 10^{10} N_D^{-7/8} \quad (1.15)$$

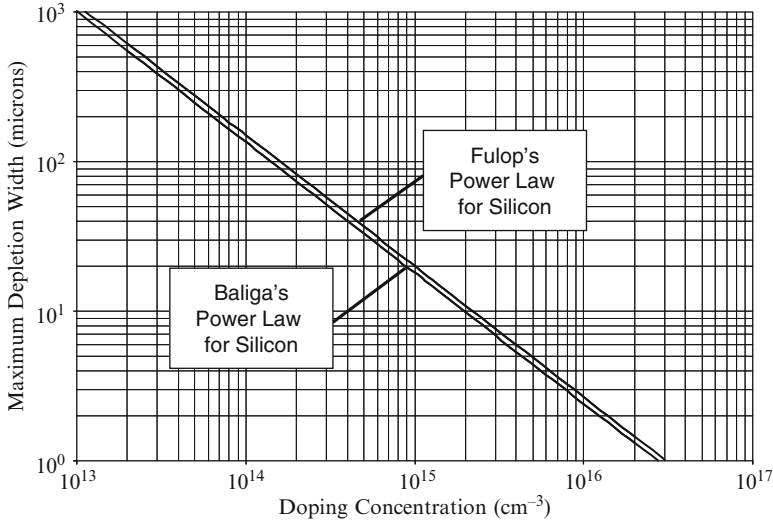
In contrast, the expression for the depletion layer width at breakdown obtained by using Fulop's power law is given by:

$$W_{PP,F}(\text{Si}) = 2.67 \times 10^{10} N_D^{-7/8} \quad (1.16)$$

The depletion layer widths at breakdown obtained for silicon devices by using the above equations can be compared in Fig. 1.12. The depletion layer widths computed using Baliga's power law are 11% smaller than those predicted by Fulop's power law.

The maximum electric field located at the P-N junction for the one-dimensional parallel-plane case is given by:

$$E_M = \frac{qN_D}{\epsilon_S} W_D \quad (1.17)$$



**Fig. 1.12** Depletion layer width at breakdown in silicon for the one-dimensional parallel-plane junction