Research and Development in
Intelligent Systems XXIV

Max Bramer Frans Coenen Miltos Petridis
Editors

Research and Development in Intelligent Systems XXIV

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TECHNICAL PROGRAMME CHAIR'S INTRODUCTION

M.A.BRAMER
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This volume comprises the refereed technical papers presented at AI-2007, the Twenty-seventh SGAI International Conference on Innovative Techniques and Applications of Artificial Intelligence, held in Cambridge in December 2007. The conference was organised by SGAI, the British Computer Society Specialist Group on Artificial Intelligence.

The papers in this volume present new and innovative developments in the field, divided into sections on Constraint Satisfaction, AI Techniques, Data Mining and Machine Learning, Multi-Agent Systems, Data Mining, and Knowledge Acquisition and Management. The volume also includes the text of short papers presented as posters at the conference.

This year's prize for the best refereed technical paper was won by a paper entitled 'An Evolutionary Algorithm-Based Approach to Robust Analog Circuit Design using Constrained Multi-Objective Optimization' by Giuseppe Nicosia, Salvatore Rinaudo and Eva Sciacca. SGAI gratefully acknowledges the long-term sponsorship of Hewlett-Packard Laboratories (Bristol) for this prize, which goes back to the 1980s.

This is the twenty-fourth volume in the *Research and Development* series. The Application Stream papers are published as a companion volume under the title *Applications and Innovations in Intelligent Systems XV*.

On behalf of the conference organising committee I should like to thank all those who contributed to the organisation of this year's technical programme, in particular the programme committee members, the executive programme committee and our administrators Rachel Browning and Bryony Bramer.

Max Bramer
Technical Programme Chair, AI-2007

ACKNOWLEDGEMENTS

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Adventures in Personalized Web Search

Barry Smyth
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Dublin, Ireland

Abstract

Even the most conservative estimates of the Web's current size refer to its billions of documents and daily growth rates that are measured in 10's of terabytes. To put this into perspective, in 2000 the entire World-Wide Web consisted of about 20 terabytes of information, now it grows by more than 3 times this every single day. This growth frames the information overload problem that is threatening to stall the information revolution as users find it increasingly difficult to locate the right information at the right time in the right way. Even today's leading search engine technologies are struggling to cope with the sheer quantity of information that is available, a problem that is greatly exacerbated by the apparent inability of Web users to formulate effective search queries that accurately reflect their information needs. This talk will focus on how so-called personalization techniques – which combine ideas from artificial intelligence, user modeling and user interface design – are being used as a practical response to this information overload problem. We will describe the experiences gained, and lessons learned, when it comes to personalizing Web search in the wild, taking special care to consider the issues that are inherent in any approach to personalization in today's privacy conscious world.

Professor Barry Smyth

Barry Smyth received a B.Sc. in computer science from University College Dublin in 1991 and a Ph.D. from Trinity College Dublin in 1996. He is currently the Head of the School of Computer Science and Informatics at University College Dublin where he holds the Digital Chair in Computer Science. He has published over 250 scientific articles in journals and conferences and has received a number of international awards for his research. His research interests include artificial intelligence, case-based reasoning, information retrieval, and user profiling and personalization. In 1999 he co-founded ChangingWorlds Ltd. to commercialise personalization technologies in the mobile sector. Today ChangingWorlds employs more than 100 people and has deployments in more than 40 mobile operators. Barry continues to serve as the company's Chief Scientist.

BEST TECHNICAL PAPER

An Evolutionary Algorithm-Based Approach to Robust Analog Circuit Design using Constrained Multi-Objective Optimization

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Abstract

The increasing complexity of circuit design needs to be managed with appropriate optimization algorithms and accurate statistical descriptions of design models in order to reach the design specifics, thus guaranteeing "*zero defects*". In the *Design for Yield* open problems are the design of effective optimization algorithms and statistical analysis for yield design, which require time consuming techniques. New methods have to balance accuracy, robustness and computational effort. Typical analog integrated circuit optimization problems are computationally hard and require the handling of *multiple, conflicting, and non-commensurate objectives having strong nonlinear interdependence*. This paper tackles the problem by evolutionary algorithms to produce *tradeoff solutions*. In this research work, Integrated Circuit (IC) design has been formulated as a constrained multi-objective optimization problem defined in a mixed integer/discrete/continuous domain. The *RF Low Noise Amplifier, Leapfrog Filter, and Ultra Wideband LNA* real-life circuits were selected as test beds. The proposed algorithm, A-NSGAII, was shown to produce acceptable and robust solutions in the tested applications, where state-of-art algorithms and circuit designers failed. The results show significant improvement in all the chosen IC design problems.

1 Introduction

During the last decade, advances made in fabrication technology and photolithography have fostered the step *from micro- to nano-electronics* allowing circuits to be produced on an ULSI (Ultra Large Scale Integration) basis. This has greatly increased the complexity of state-of-the-art integrated circuits

(ICs) whose design is even more targeted towards system-on-chip or system-in-package solutions [4]. In this context, the role of CAD techniques for circuit analysis and optimization became essential to obtain solutions that satisfy the requested performance with the minimum time effort (i.e., minimizing the *time-to-market*).

Due to the complexity of state-of-the-art analog circuits, global and local optimization algorithms have to be extensively employed to find *a set of feasible solutions* that satisfies all the *objectives* and the *constraints* required by a given application. Typical objective and constraint functions used in the IC design are area, noise, speed, linearity, or power consumption expressed as a function of the *design parameters* such as transistor sizes, resistor/capacitor values, spiral inductor geometry, etc. Very frequently two or more of these *objectives* are *conflicting*, i.e. improving one objective forces another or others to worsen, thus a *suitable tradeoff* has to be accomplished. Traditional single-objective optimization algorithms provide only one solution (sometimes *a set of candidate solutions*) to such problems, which minimizes/maximizes an overall objective function obtained by mixing individual targets through application of properly weighted mathematical operators. As a consequence, such techniques do not allow *multiple competing goals* to be accounted for explicitly. Moreover they do not give circuit designers the freedom to choose among different, *equally feasible* solutions. A big step forward in this direction can be achieved using a multi-objective approach [7]. This technique allows different objectives to be treated *separately and simultaneously* during the optimization process.

The circuit designer is allowed to choose a solution that privileges one objective (considered as primary) with respect to the others or another one that simply provides an acceptable tradeoff among conflicting goals. Another feature that characterizes IC design is that the objectives and the constraints to be optimized are usually defined in a *discrete domain*. Indeed, as far as design for manufacturability is of concern, each optimization variable is related to the physical dimensions of the components placed in the circuit layout, whose resolution is defined by photolithography. Therefore, optimization techniques that cannot manage *mixed continuous/discrete variables* are of limited (if any) applicability in real-life problems. Based on the above considerations, IC design can, in general, be treated as a constrained multi-objective optimization problem (MOP) defined in a mixed continuous/discrete domain.

The paper is structured as follows: Section 2 describes the *nominal design* and the *design for yield* for the analog IC design; Section 3 formally introduces the adopted multi-objective framework; Section 4 presents the multi-objective evolutionary algorithm, A-NSGAII; Sections 5, 6, and 7 detail the three real-world applications faced *RF Low Noise Amplifier, LeapFrog Filter* and *Ultra WideBand Low Noise Amplifier*. For each circuit, the nominal circuits, the design for yield values and the corresponding Pareto Fronts obtained have been reported and the results are compared with those obtained by state-of-art optimization algorithms and designers' circuits. Concluding remarks are presented in Section 8.

2 Nominal Design versus Design for Yield

Analog IC design is a rather complex task that involves two important steps: 1) the definition of a *circuit topology* and 2) *circuit sizing*. The first step requires deep knowledge of microelectronics and *good design experience* because it is essential to verify the overall feasibility of the circuit. The analyses carried out in this step allow the designer to discard solutions that cannot be employed for a given application due to structural incompatibility. The second step consists in defining a set of optimal circuit parameters with the aim to push the performance of the selected topology until all the specifications are met. Iterations might be necessary if the outcome of the second step (*circuit sizing*) does not confirm the feasibility analysis carried out in the first one (*topology definition*). Two types of specifications have to be met in the step of circuit sizing: *1) performance*, i.e., fulfilment of the specifications imposed by a given application, and *2) robustness*, i.e., insensitiveness to parametric and environmental variations. To simplify the design, these two specifications are commonly treated separately. Therefore, the performance is first assessed under the hypotheses that no parametric or environmental variations take place. This task is commonly referred to as *nominal design* because such hypotheses define the so-called nominal (i.e., ideal) operating condition. Nominal design represents a first verification of the feasibility analysis carried out during the topology definition: an unsuccessful outcome mandates circuit topology to be reviewed.

The so-called *nominal operating conditions* are defined a priori and depend on the application for which the IC is being designed. Most commonly they include given values of supply voltage and ambient temperature, and the typical (i.e., mean) fabrication process setup. In these conditions, the nominal design basically consists of determining a set of component parameters (i.e., transistors width and length, resistor or capacitor values, inductor geometry, etc.) of a given circuit topology that satisfy all specifications. If nominal design is successful, then circuit robustness is assessed by verifying that all specifications are satisfied even when *parametric and environmental variations* take place. This is extremely important to ensure that the performance of the IC is still acceptable once it has undergone the fabrication process and it is put in operation in a real-world (as opposed to ideal) environment. This task is referred to as design for robustness or, more commonly, *design for yield*.

The term *yield* in the framework of the microelectronics industry denotes the ratio between the number of chips that have acceptable performance over those that have been manufactured. There are two classes of causes by which the performance of a circuit can be classified as unacceptable: *1) local perturbation* (silicon crystal defects that cause the malfunctioning of a single chip in a wafer) and *2) global perturbations* (process imprecision like mask misalignment, temperature and/or implantation dose variations involving all the chips in a wafer). Since there is a direct correlation between the yield and the production level, yield maximization is a strategic objective of the microelectronics industry [5].

3 IC Design as a Constrained MOP

The research work is motivated by the observation that most circuit design problems involve *multiple, conflicting, and non-commensurate objectives*; hence, it is necessary to use proper algorithms to optimise multiple conflicting objectives while satisfying several constraints. While both integer and discrete variables have a discrete nature, only discrete variables can assume floating-point values (they are often unevenly spaced, by a *step variable*, a designer defined parameter). In general, variables are commonly defined in *a mixed integer discrete continuous domain*. IC design can be defined as a constrained multi-objective optimization problem defined in a mixed integer/discrete/continuous domain. A Multi-objective Optimization Problem (MOP) can be formally defined as follows:

Definition 1 *Find a vector* $\vec{x}^* = [x_1^*, x_2^*, \ldots, x_n^*]^T = [X^{(I)}, X^{(D)}, X^{(C)}]^T$ *which satisfies the variable bounds:*

$$x_i^{(L)} \leq x_i \leq x_i^{(U)} \quad i = 1, 2, \ldots, n \tag{1}$$

satisfies the p equality constraints:

$$h_i(\vec{x}) = 0 \quad i = 1, 2, \ldots, p \tag{2}$$

is subject to the m inequality constraints:

$$g_i(\vec{x}) \geq 0 \quad i = 1, 2, \ldots, m \tag{3}$$

and optimizes the vector function

$$\vec{f}(\vec{x}) = [f_1(\vec{x}), f_2(\vec{x}), \ldots, f_k(\vec{x})]^T \tag{4}$$

where $X^{(I)}, X^{(D)}, X^{(C)}$ *denote feasible subsets of Integer, Discrete and Continuous variables respectively.*

Equations (1), (2) and (3) define the *feasible region*

$$\begin{aligned} \Omega = \{\vec{x} \in \Re^n : x_i^{(L)} \leq x_i \leq x_i^{(U)} \quad & i = 1, 2, \ldots, n; \\ g_i(\vec{x}) \geq 0 \quad & i = 1, 2, \ldots, m; \\ h_i(\vec{x}) = 0 \quad & i = 1, 2, \ldots, p\} \end{aligned} \tag{5}$$

and any point $\vec{x} \in \Omega$ defines a *feasible solution*. The vector function $\vec{f}(\vec{x})$ maps the elements of Ω into a set Λ which represents all possible values of the objective functions:

$$\Lambda = \{\vec{f}(\vec{x}) \in \Re^k : \vec{x} \in \Omega\} \tag{6}$$

The evaluation function of the MOP $f : \Omega \rightarrow \Lambda$, maps decision variables $\vec{x} = (x_1, x_2, \ldots, x_n)$ to vectors $\vec{y} = (y_1, y_2, \ldots, y_k)$.

Definition 2 *A point* $\vec{x}^* \in \Omega$ *is Pareto optimal if for every* $\vec{x} \in \Omega$ *and* $I = \{1, 2, \ldots, k\}$ *either,*

$$\forall_{i \in I}(f_i(\vec{x}) = f_i(\vec{x}^*)) \tag{7}$$

or there is at least one $i \in I$ *such that*

$$f_i(\vec{x}) \geq f_i(\vec{x}^*) \tag{8}$$

A vector $\vec{u} = (u_1, \ldots, u_k)$ is said to dominate $\vec{v} = (v_1, \ldots, v_k)$, denoted by $\vec{u} \preceq \vec{v}$ if and only if $\vec{u}$ is partially less than $\vec{v}$, i.e., for all $i \in \{1, \ldots, k\}$, $u_i \leq v_i \wedge \exists i \in \{1, \ldots, k\} : u_i < v_i$. If the vector $\vec{u}$ dominates the vector $\vec{v}$, or mathematically $\vec{u} \preceq \vec{v}$, we also say that $\vec{v}$ is dominated by $\vec{u}$, or $\vec{u}$ is non-dominated by $\vec{v}$.

Definition 3 *For a given MOP* $\vec{f}(\vec{x})$*, the Pareto optimal set,* $\mathcal{P}^*$*, is defined as:*

$$\mathcal{P}^* = \{\vec{x} \in \Omega : \neg\exists \vec{x}' \in \Omega \quad \vec{f}(\vec{x}') \preceq \vec{f}(\vec{x})\}. \tag{9}$$

x^* is Pareto optimal if there exists no feasible point x which would decrease some criterion without causing a *simultaneous* increase in at least one other criterion. The notion of *optimum* is changed, we are using the *Edgeworth-Pareto Optimum* notion [6]: the aim is to find good compromises (or trade-offs) rather than a single solution as in global optimization. A Pareto optimal set that truly meets this definition is called a true Pareto optimal set, $\mathcal{P}^*_{true}$. In contrast, a Pareto optimal set that is obtained by means of an optimization method is referred to as an *observed Pareto optimal set*, $\mathcal{P}^*_{obs}$. In reality, an observed Pareto optimal set is an *estimate* of a true Pareto optimal set. Identifying a good estimate $\mathcal{P}^*_{obs}$ is the key factor for the decision maker's selection of a compromise solution, which satisfies the objectives as much as possible. We denote the observed Pareto optimal set at time step t obtained using an optimization method by $\mathcal{P}^{*,t}_{obs}$ (or the current observed Pareto optimal set). Moreover, we have $\mathcal{P}^{*,t}_{obs} = \{\vec{x}^t_1, \ldots, \vec{x}^t_\ell\}$ where $\ell = \mid \mathcal{P}^{*,t}_{obs} \mid$ is the total number of observed Pareto solutions at time step t. Obviously, the major problem a decision maker needs to solve, is to find "the best" $\vec{x} \in \mathcal{P}^*_{obs}$.

Definition 4 *For a given MOP* $\vec{f}(\vec{x})$ *and Pareto optimal set* $\mathcal{P}^*$*, the Pareto front,* $\mathcal{PF}^*$*, is defined as:*

$$\mathcal{PF}^* = \{\vec{u} = \vec{f} = (f_1(\vec{x}), \ldots, f_k(\vec{x})) \mid \vec{x} \in \mathcal{P}^*\} \tag{10}$$

As for the Pareto optimal set, we can define the *observed Pareto front* [7] at time step t by an optimization method: $\mathcal{PF}^{*,t}_{obs} = \{\vec{u}^t_1, \vec{u}^t_2, \ldots, \vec{u}^t_N\}$ where $N = \mid \mathcal{PF}^{*,t}_{obs} \mid$ is the total number of observed Pareto front solutions at time step t. Identifying a good estimate of $\mathcal{PF}^{*,t}_{obs}$ is crucial for the decision maker's selection of a good IC in terms of nominal design and yield value.

Summarizing, for a MOP we can define the following procedures: find the optimal (or the observed) Pareto front; and choose one of the candidate solutions in the Pareto front, using some higher-level information (for instance

yield in IC design). In this research work we adopt a simple selection criterion: our selection procedure chooses the non-dominated solution closest to the *ideal point* (for each of the k objectives, there exists one different optimal solution; an objective vector constructed with these individual optimal objective values constitutes the ideal objective vector).

4 The Algorithm

Evolutionary Algorithms (EAs) are a class of stochastic optimization methods that simulate the process of natural evolution [7]. EAs can be defined as *population-based stochastic generate-and-test algorithms*. They operate on a set of candidate solutions, which is subsequently modified by the two basic principles: *selection* and *variation*. While selection mimics the competition for resources among living beings, variation imitates the natural capability of creating new living beings by means of recombination and mutation. Although the underlying mechanisms are simple, these algorithms have proven to be general, robust and powerful search tools [7]. Such approaches do not guarantee that optimal solutions are identified, but try to find a good approximation of suboptimal or optimal solutions. Classical optimization methods use a point-to-point approach, where one solution in each iteration is modified to a different (hopefully better) solution. The outcome is a single optimized solution in a single simulation run. One of the most striking differences to classical optimization algorithms is that EAs, use a *population of candidate solutions* in each iteration instead of a single solution and the outcome is also a population of solutions. An EA can be used to capture multiple optimal solutions in its final population. In evolutionary computing there is *no restriction on the objective function(s)* that can be used.They can be non-differentiable or even discontinuous, there is no need to know the exact form of the objective function and simulations (*runs*) can be used to derive a fitness value. The initial population does not necessarily have to be generated *randomly* but it can also be initialised *ad-hoc* (for instance the designer's circuit). Candidate solutions may be represented by using various codings (binary, integer, real, mixed, etc.). In this paper, a well-known evolutionary algorithm, NSGAII, is used. NSGAII [7] is an elitist evolutionary algorithm with a fast non-dominated sorting procedure and a density estimation of the solutions provided by the crowding distance. In order to tackle the integer/discrete/continuous variables, we designed and implemented a modified version of NSGAII, ADVANCED NSGAII (A-NSGAII). Different kind of mutations could be used, in particular *convex mutation, self-adaptive mutation, Gaussian mutation* and *hybrid Gaussian mutation* [8]. They differ in the procedure used to obtain the mutated value. In detail:

- Self-adaptive mutation is computed by $x_i^{new} = x_i + \sigma_i * N(0,1)$; where $\sigma_i' = \sigma_i * exp((\tau * N(0,1)) + (\tau' * N_i(0,1))$ with $\tau = (\sqrt{2\sqrt{n}})^{-1}$, $\tau' = 1/\sqrt{2n}$, and $\sigma_i^{(t=0)} = ((U_B - L_B)/\sqrt{n}) \times 0.4$
- Hybrid Gaussian Mutation acts according to the following equation:

$x_i^{new} = x_i + \sigma * N(0,1);$

$$\sigma = \begin{cases} \beta * |x_i - x_j|, & x_i \neq x_j, \quad \text{if } x_i * x_j > 0 \\ \beta * |x_i + x_j|, & x_i \neq x_j, \quad \text{if } x_i * x_j < 0 \end{cases}$$

where $\beta \in [0.5, 1.5]$ is a random number obtained with uniform distribution.

- The Gaussian mutation operator instead applies the following equation: $x_i^{new} = x_i + \alpha * N(0,1)$; where $\alpha = (\frac{1}{\beta})e^{(-f)}$ is the mutation potential.

Finally, A-NSGAII uses constrained tournament selection to deal with *unfeasible solutions* during the optimization process. One difficult matter in constrained optimization problems is finding a feasible set. In the first steps it could represent a true challenge. One of the possible reasons is that feasible regions could be a very small subset of the search space. This method uses binary tournament selection, that is, two individuals of the population are chosen and compared and the fittest is copied in the following population. When a problem presents constraints, two solutions can be feasible or unfeasible. Just one of the following cases is possible: (i) both are feasible; (ii) one solution is feasible and the other is not; (iii) both are unfeasible. Case (i) is solved using a dominance relation that takes into account the constraint violation. In case (ii) only the feasible solution is chosen and in case (iii) a penalty function is used (see definition of Ω below). Let $g_j(\mathbf{x}) \geq 0, j = 1...m$ be the constraints of the normalized problem. The constraints violation is defined as follows:

$$\omega_j = \begin{cases} |g_j(\mathbf{x})|, & \text{if } g_j(\mathbf{x}) < 0; \\ 0, & \text{otherwise.} \end{cases} \tag{11}$$

The overall violation Ω is defined as: $\Omega = \sum_{j=1}^{m} \omega_j(\mathbf{x})$ A solution $\mathbf{x}_i$ is said to "*constrain dominate*" a solution $\mathbf{x}_j$ if one of these conditions is true: (1) Solution $\mathbf{x}_i$ is feasible and $\mathbf{x}_j$ is not. (2) Solutions $\mathbf{x}_i$ and $\mathbf{x}_j$ are infeasible but $\mathbf{x}_i$ has a lesser Ω value. (3) Solutions $\mathbf{x}_i$ and $\mathbf{x}_j$ are both feasible, but $\mathbf{x}_i$ dominates $\mathbf{x}_j$. In constrained tournament selection, the individual having a lower Ω value wins the tournament.

Finally, the optimization process ends when a maximum number of runs is reached or the information gain reaches a final steady state [2].

5 Radio Frequency Low Noise Amplifier

The RF Low Noise Amplifier (LNA) is one of the most critical building blocks in modern integrated radio frequency (RF) transceivers. It is integrated into the receiving chain and is either directly connected to the antenna or placed after the RF pass-band filter [3]. It must enhance input signal levels at gigahertz frequencies whilst preserving the signal-to-noise ratio. Moreover, low DC current consumption is mandatory in all portable hand-held application to

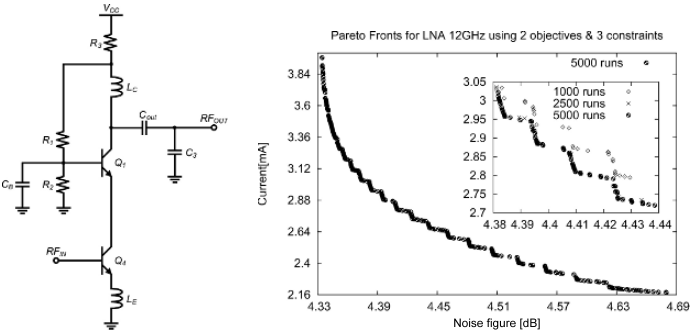

Figure 1: Left plot: Circuit schematic of the RF LNA. Right plot: Pareto Front obtained by A-NSGAII for RF LNA.

allow for long battery life. Other critical performance parameters of LNAs are gain and impedance matching. The circuit schematic of the RF LNA under investigation is shown in Fig. 1 (left plot). It is based on a cascode configuration with integrated emitter degeneration inductor. The cascode topology provides excellent frequency stability at high gain and high isolation between input and output terminals. Moreover, it eliminates Miller amplification of the base collector capacitance making input and output matching almost independent of each other. These advantages are obtained at the cost of negligible drawbacks in comparison with the common-emitter configuration, such as lower output swing and a slight increase in noise figure. The Pareto Front of the RF LNA (obtained after 5000 runs) is sketched in Fig. 1 (right plot). It displays the "*zig-zag*" behaviour that characterizes optimization problems defined in a discrete domain. The algorithm is able to find 664 *distinct non-dominated solutions* that are well distributed and *cover* almost all the trade-off curve. The number, distribution, and coverage of solutions found are all important parameters to assess an algorithm's performance when it is employed in IC design problems. Indeed, they can demonstrate its exploratory capabilities leaving few doubts about the possibility of pushing the performance of the circuit furthermore. The inset plot of Fig. 1 (right plot) shows a zoom of the central part of the Pareto Front where solutions found after 1000 and 2500 runs are also reported. It demonstrates that reducing the computational load by a large amount (up to 5) does not degrade algorithm's performance so much. Indeed, the Pareto Front found after 1000 and 2500 runs still exhibits very good algorithm performance since it includes solutions that differ only slightly from those belonging to the "final" one.

The *nominal performance* of six notable solutions are reported in table 1 together with that of the designer (achieved through "*manual*" sizing). Corresponding values of yield (computed from Montecarlo simulations with 200 samples in the mismatch-only mode), obtained from Montecarlo simulations,

Table 1: Multi-Objective Optimization of RF LNA using 5 objectives with A-NSGAII.

Variable	Min NF	Min I_C	Min S_{11}	Max S_{21}	Min S_{22}	Opt. Nom.	Designer
$Area_1$	2	1	3	1	1	2	2
$Area_4$	3	3	3	3	3	3	3
C_3 (fF)	320	400	440	460	450	400	350
C_{out} (fF)	170	240	150	200	200	170	190
R_1 (Ω)	4k	8.5k	7.3k	5.4k	6.8k	8.2k	6k
R_3 (Ω)	30	80	200	70	10	80	400
V_{BE} (mV)	884	864	887	886	867	877	885
Performance Function							
$\mid S_{11} \mid < -14$ dB	-16.337	-14.884	-19.852	-14.855	-14.603	-16.673	-17.40
$\mid S_{21} \mid > 8$ dB	9.736	8.526	8.378	10.936	8.753	9.402	9.30
$\mid S_{22} \mid < -6$ dB	-21.074	-8.216	-7.374	-21.933	-44.297	-28.223	-10.99
NF < 4.7 dB	4.334	4.670	4.456	4.562	4.606	4.377	4.46
$I_C < 4$ mA	3.985	2.193	3.907	3.981	2.460	3.076	3.70
Yield	64.5%	68%	85.5%	70%	94%	**100%**	99.5%

are also reported. As expected, solutions found (in particular, the optimal nominal solution) using the multi-objective optimization approach *dominate the designer's one* (i.e., the current or noise "nominal" performance is better). However, solutions with minimum noise or minimum current (placed at the edge of the Pareto Front of Fig. 1 (right plot) and thus farthest away from the "ideal" point), exhibit lower values of yield. In fact, statistical fluctuations around the nominal point cause either the current or noise performance to jump out of the feasible set, making the whole circuit faulty. On the other hand, the point selected according to the "optimality" criterion (i.e., placed closest to the "ideal" solution) performs 100% yield (see table 1). In the Pareto Front region closest to the "ideal" point there is a good probability of finding high-yielding circuits before design centering process.

6 LeapFrog Filter

Analog front-end filters are essential components in many electronic equipments ranging from communication systems to medical instruments to signal processors and so on. They provide a narrow pass-band to the signal and attenuate unwanted noise in the stop-band [1]. Fabrication of analog filters in state-of-the-art VLSI technology allows both passive and active components to be integrated in the same silicon die. Although there is a great advantage from the economic point of view, it generally requires wise design because integrated components suffer from higher process tolerances than their discrete counterpart. This feature elects integrated analog filters as excellent candidates to benchmark the performance of circuit optimization tools when yield maximization is of concern. The circuit block employed as test case, i.e. a

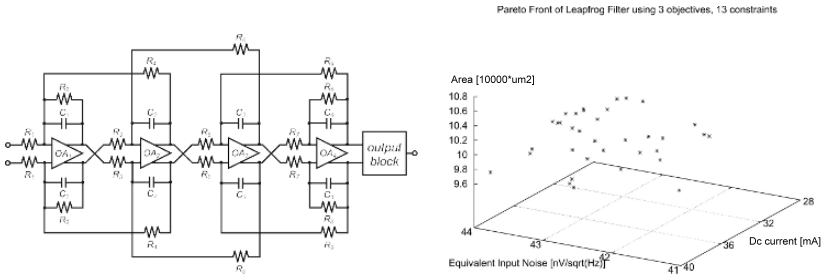

Figure 2: Left Plot: Circuit schematic of the Leapfrog Filter. Right Plot: Pareto Front observed of Leapfrog Filter using 3 objectives and 13 constrains after 30000 runs.

fifth-order leapfrog filter, is depicted in Fig. 2 (left plot). Four leapfrog loops are realized through 4 (equal) differential opamps (OA1-OA4), 18 resistances (two times R1-R9), and 8 capacitances (two times C1-C4). Differential-to-single conversion is performed by the output block, which also implements an additional time constant via a real pole. The filter design was accomplished in two steps: 1) opamps AO1-AO4 were first designed at the transistor level; 2) the passive network of the filter was then optimized using a behavioural model of the opamps. Resistance and capacitance values are calculated on the basis of other quantities that will be treated as input variables of the optimization problem. Expressions relating the resistance and the capacitance values to these quantities are quite complex and will not be reported in the following. The 20 variables used as input of the optimization problem are: k1, k2, k3, k4, m1, m2, m3, m4, Vn1, Vn2, Vn3, Vn4, w0, wrp, Ra, C, C1, L2, C3, L4. The first 4 parameters (k1-k4) influence the output dynamic of each operational amplifier, m1-m4 allow the scaling of the resistances and capacitances leaving the leapfrog time constants unchanged; Vn1-Vn4 impose the equivalent input noise of each operational amplifier; w0 provides a frequency shift of the filter transfer function; wrp is the frequency of the real pole in the output block; Ra through to L4 determine the filter time constants. The set of objective functions and related constraints employed in the formulation of the optimization problem are reported in table 2. Dc gain, pass-band ripples and stop-bands are directly related to the frequency mask of the filter, whereas the network delay is assessed using the group delay (ripple and slope). Other performance metrics are: low-frequency input resistance; output dynamic of each opamp; equivalent input noise, to which both active and passive components contribute; dc current consumption, related to the equivalent opamp input noise in the behavioural model; silicon area. The optimization results obtained by using A-NSGAII are summarized in Table 2, where a comparison with three state-of-the-art deterministic algorithms (Powel's algorithm NEWUOA [12], DIRECT [11], A-CRS [9]) is also reported. None of the investigated algo-

Table 2: LeapFrog Filter results: comparisons among **NEWUOA**[12], **DIRECT**[11], **A-CRS** [9], Designer, and **A-NSGAII**.

Goals	**Bounds**	new**UOA**	**DIRECT**	**A-CRS**	**Designer**	**A-NSGAII**
DC gain	≥ -0.01 dB	-0.003	-0.003	-0.0026	-0.003	-0.0025
Pb ripple 9.1MHz	$\leq 0.8\ dB_{PP}$	**0.95**	**0.86**	**0.85**	**0.806**	0.55
Pb ripple 9.7MHz	$\leq 1.8\ dB_{PP}$	0.97	1.33	1.07	0.97	0.55
Sb 22.5MHz	$\geq 25\ dB_C$	26.60	36.56	31.86	36.64	36.84
Sb 34.2MHz	$\geq 56\ dB_C$	**46.11**	**55.08**	**51.64**	**55.92**	56.23
Gd ripple 9.1MHz	≤ 20 ns	**24.52**	20.7	14.80	19.28	16.17
Gd ripple 9.7MHz	≤ 40 ns	30.55	39.6	16.50	26.36	24.18
Gd slope 6.0MHz	≤ 3 fs/Hz	2.63	1.28	**3.23**	2.10	2.36
Eq. in. resistance	$\geq 12.2\ k\Omega$	**11.82** k	31.54 k	13.42k	**12.18** k	12.24 k
Out. dynamic 1	≤ 2.8 V	**2.88**	2.23	2.72	**2.83**	2.76
Out. dynamic 2	≤ 2.8 V	2.68	1.36	2.20	2.22	2.43
Out. dynamic 3	≤ 2.8 V	**3.17**	2.60	**3.01**	1.71	2.70
Out. dynamic 4	≤ 2.8 V	2.13	1.32	1.43	1.53	1.73
Eq. in. noise	$\leq 44\ nV/Hz^{\frac{1}{2}}$	**47.73**	**139**	**47.41**	**46.44**	42.14
Dc current cons.	$\leq 40mA$	**40.64**	30	**42.17**	39.58	34.47
Silicon area	$\leq 18000\mu m^2$	15964	**29500**	14457	14037	14622
Global Error		85.95%	289.1%	43.9%	7.8%	0
Yield		n.a.	n.a.	n.a.	n.a.	69.5%

rithms is able to find feasible solutions, moreover the best solutions found by such algorithms violate more than one constraint. The *DIRECT* algorithm exhibits the worst performance with huge errors on the equivalent input noise and silicon area. The *NEWUOA* violates 8 out of 16 constraints (in boldface) with moderate errors in each one. The A-CRS performs better than any other investigated algorithm on this test bed, however its best solution is very far from being acceptable because it does not satisfy 6 constraints. It is interesting to note that in most cases such algorithms encountered difficulties in satisfying performance metrics that also have given problems to the designer. Another interpretation is that they are not able to perform better than the designer due to their limited exploration capabilities. On the other hand, A-NSGAII finds feasible solutions also providing a considerable amount of over-achievement in most performance metrics producing high yield values. To further consolidate this concept, Fig. 2 (right plot) shows the Pareto Front of the leapfrog filter obtained after 30000 runs using A-NSGAII. Among the feasible solutions, the algorithm provides 36 non dominated points. Moreover, the degree of coverage and distribution across the objective space is satisfactory.

7 Ultra WideBand Low Noise Amplifier

Ultra wideband (UWB) signalling [14] is the modern art of reusing previously allocated RF bands by hiding signals under the noise floor. UWB systems transmit signals across a much wider frequency than conventional narrowband

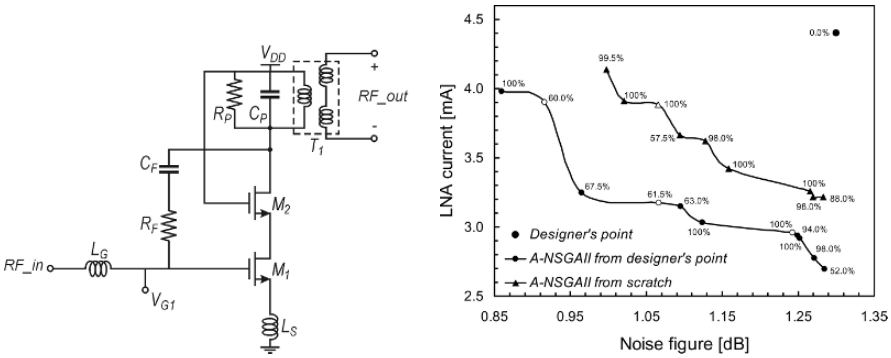

Figure 3: Left Plot: Ultra Wideband Low Noise Amplifier Schematic. Right Plot: Pareto Fronts obtained A-NSGAII. For A-NSGAII the empty triangle and empty circle are *sub-threshold circuits*.

systems do, moreover they are usually very difficult to detect. Government regulators are testing UWB emissions to ensure that adequate protection exists to current users of the communications bands. The amount of spectrum occupied by an UWB signal, i.e. the bandwidth of the UWB signal, is at least 25% of the centre frequency. Thus, an UWB signal centred at 4 GHz would have a minimum bandwidth of 1 GHz. The most common technique for generating an UWB signal is to transmit pulses with durations of less than 1 nanosecond. Recently, the interest in UWB systems for wireless personal area network applications has increased significantly. Due to the extremely low emission levels currently allowed by regulatory agencies, UWB systems tend to be short-range and indoor. The schematic of an UWB Low Noise Amplifier [15] is shown in Fig. 3 (left plot). The UWB LNA adopts a single cascode topology, which allows high input/output isolation to be achieved. The design should be carried out to achieve wideband input matching together with good noise performance. The LS and LG inductors perform the UWB LNA input matching as in the classical narrow-band design, while CF and RF implement an ac resistive feedback to broaden the input matching bandwidth. The value of RF should be chosen as a compromise between the input bandwidth widening and the amount of noise added by the resistor. An RLC shunt resonator represents the load of the LNA. The capacitor CP and the primary winding of the load transformer T1 should be designed to resonate at the frequency of 4 GHz, while the shunt resistance RP was inserted to lower the quality factor of the resonator. Such a shunted resonant load allows an adequate gain spectral flatness to be achieved.

Power consumption is a crucial performance parameter in many fields of electronic design. Indeed, it determines battery life in portable applications such as *mobile phones* or contributes to thermal heating in *VLSI circuits* such as *memories* and *microprocessors*. For these reasons, several efforts have been undertaken to minimize power dissipations in both analog and digital ICs. The *Sub-threshold* operation of MOS transistors has demonstrated to be an effective

way to accomplish this task without degrading circuit performance. Besides this, the trend toward sub-threshold operation of MOS transistors has been motivated by the need for reducing the supply voltage in deeply scaled CMOS technologies. In fact, the threshold voltage of nanometre CMOS does not scale down at the same rate as the supply voltage does, moreover it does not scale at all in some cases. The resulting smaller voltage headroom renders the task of IC design even more challenging and makes the sub-threshold operation of MOS devices necessary. The benefits achievable by sub-threshold operations are paid at the price of much higher sensitivity of ICs to variations in supply voltage, temperature and in the fabrication process. This in turn contributes to lower circuit robustness because large deviations from nominal operating conditions are more likely to take place. Therefore, robust design approaches such that described in this paper become essential to avoid faulty operations of MOS-based ICs pushed into the sub-threshold region. Figure 3 (right plot) shows the Pareto Fronts obtained by A-NSGAII. Empty triangles and empty circles indicate the subthreshold circuits discovered by A-NSGAII.

8 Conclusions

The present research work is motivated by the observation that most circuit design problems involve multiple, conflicting, and non-commensurate objectives and several constraints. We formulated IC design as a constrained multi-objective optimization problem defined in a mixed integer/discrete/continuous domain. To face this problem an optimization algorithm, A-NSGAII, for analog circuit sizing has been presented. The proposed algorithm, A-NSGAII, was shown to produce acceptable solutions for RF Low Noise Amplifier, Leapfrog Filter, and Ultra WideBand Low Noise Amplifier where state-of-art techniques and circuit designers failed. The results show significant improvements in both the chosen IC design problems in terms of nominal design and yield values. Furthermore, the results also show that the sizing of robust analog circuits can be achieved at lower computational effort than that required by traditional optimization algorithms minimizing the time-to-market.

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CONSTRAINT SATISFACTION

DisBO-wd: a Distributed Constraint Satisfaction Algorithm for Coarse-Grained Distributed Problems

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Abstract. We present a distributed iterative improvement algorithm for solving coarse-grained distributed constraint satisfaction problems (DisCSPs). Our algorithm is inspired by the Distributed Breakout for coarse-grained DisCSPs where we introduce a constraint weight decay and a constraint weight learning mechanism in order to escape local optima. We also introduce some randomisation in order to give the search a better chance of finding the right path to a solution. We show that these mechanisms improve the performance of the algorithm considerably and make it competitive with respect to other algorithms.

1 Introduction

The recent growth of distributed computing has created more opportunities for collaboration between agents (individuals, organisations and computer programs) where there is a shared objective but, at the same time, there is also a competition for resources. Hence, participants make compromises in order to reach agreement - a process which can be automated if the situation is modelled as a Distributed Constraint Satisfaction Problem (DisCSP) [12]. DisCSPs formally describe distributed problems where each participant in the problem is represented by an agent, and the collection of agents have to collaborate in order to reach a satisfactory agreement (or find a solution) for a problem. Research in this emerging field includes problem solving techniques which are classified as constructive search or iterative improvement search. Iterative improvement search is normally able to converge quicker than constructive search on large problems, but it has a propensity to converge to local optima. Previous work on iterative improvement search has considered a variety of techniques for dealing with local optima. Prominent amongst these is the breakout, which attaches weights to constraints which are difficult to satisfy [13].

Distributed iterative improvement algorithms for DisCSPs such as DisPeL[1] and DBA[13] assume that each agent is responsible for one variable only and knows its domain, the constraints which apply to the variable, the agents whose variables are constrained with its variable and the current value for any varible directly related to