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Pipelined ADC Design and Enhancement Techniques

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# Pipelined ADC Design and Enhancement Techniques

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# Preface

Pipelined ADCs have seen a tremendous growth in innovation and scope over the past few years. As such understanding both the basic concepts and the leading edge techniques required to realize pipelined ADCs which meet the challenging specifications of today's market and applications is required. While pipelined ADCs are popular circuit blocks, beyond publications in periodicals there are only a few condensed resources which are dedicated to education in the area. This book aims to help bridge the gap with a thorough discussion of pipelined ADCs.

This book is targeted to both the beginner and expert looking to acquire knowledge in pipelined ADCs. In the first section of this book, a tutorial discussion of several key design tradeoffs involved in designing a pipelined ADC is given. The discussion is presented with sufficient detail so as to allow those with only introductory knowledge of pipelined ADCs to quickly understand the limiting factors which motivate research into methods which enhance the performance of pipelined ADCs. In the second half of this book a detailed overview and discussion of four state-of-the-art pipelined ADCs with silicon implementations and measured results is given. The innovations include: a technique to rapidly digitally correct gain + DAC errors in a pipelined ADC, an architecture to enable a single ADC to be designed to achieve low power for a very wide range of sampling rates, a circuit technique to eliminate front-end sample-and-holds in pipelined ADCs, and finally a very low power pipelined ADC architecture based on capacitive charge pumps.

The innovations presented in this book provides several tools which can be of great use to help a pipelined ADC designer deliver a design with good linearity, broad application, and very low power.

# Acknowledgements

Research is a unique proposition. One is forced to look into the depths of the unknown and find an answer to a question that does not necessarily have an answer. In some cases your answer fits the question – in some cases your answer fits the question like a square peg in a round hole. Regardless of the madness, the journey of developing abstract ideas into ultimately something which works is truly a unique and completely enriching experience – an experience that I for one am tremendously thankful for and very fortunate to have undergone in developing the material for this book. Acknowledging specific people in the development of an abstract piece of art is somewhat partial, as undoubtedly every person one interacts with during the course of a writing a book in some shape or form impacts the work. There are a few key people however who have helped this work take form. Firstly I must thank Professor David Johns at the University of Toronto. His guidance in developing many of the ideas discussed in this book were invaluable. I am also thankful to Professor Ken Martin, also of the University of Toronto, whose rigor and boldness significantly helped this work take shape. I also thank the support of the team of excellent designers at Broadcom Netherlands, especially Jan Mulder and Klaas Bult, who in addition to providing a wealth of knowledge, have inspired me to be excited about the future in mixed signal circuit design. Of course one cannot accomplish anything in life without the unquestioned pillar of support one's family offers. This book is dedicated to my family.

# Contents

# Abbreviations

| | |
|---|---|
| ADC | Analog to digital converter |
| CBSC | Comparator based switched capacitor |
| CM | Common mode |
| CMFB | Common mode feed back |
| CMPS | Current modulated power scaling |
| CMR | Common mode rejection |
| DAC | Digital to analog converter |
| dBFS | dB relative to full scale |
| DLL | Delay locked loop |
| DNL | Differential non-linearity |
| DNW | Deep N-well |
| ENOB | Effective number of bits |
| FOM | Figure of merit |
| IC | Integrated Circuit |
| INL | Integral non-linearity |
| KCL | Kirchhoff's current law |
| MDAC | Multiplying digital to analog converter |
| MIM | Metal-insulator-metal |
| NM | Nominal mode |
| PGA | Programmable gain amplifier |
| PRM | Power reduction mode |
| S/H | Sample-and-hold |
| SAR | Successive approximation register |
| SFBO | Switched feedback biased Opamp |
| SFDR | Spurious free dynamic range |
| SNR | Signal to noise ratio |
| SNDR | Signal to noise plus distortion ratio |

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# Chapter 1
# Introduction

## 1.1 Overview

The pipelined topology is a popular option for ADCs which require resolutions on the order of 8–14 bits and sampling rates between a few MS/s to hundreds of MS/s. The popularity of the topology can be attributed to its relatively simple and repetitive unit structure, as well as a significant reduction in the number of comparators required to achieve a fixed resolution when compared to other Nyquist-rate data converters such as Flash, and Folding + Interpolating based converters. Pipelined ADCs are used in a variety of applications such as: mobile systems, CCD imaging, ultrasonic medical imaging, digital receivers, base stations, digital video (e.g. HDTV), xDSL, cable modems, cellular base stations, and fast Ethernet. Since pipelined ADCs are used in a variety of electronic systems, research in improving the performance of pipelined ADCs has attracted much attention over the past decade, where the most popular areas of research have been: linearity enhancement, and power reduction. In recent years, an emerging area of research in ADCs has been the development of reconfigurable ADCs [1].

Linearity enhancement has been an active area of research as with deeper submicron technology low intrinsic gain, low supply voltages, and device mismatch have made achieving very linear data converters (i.e. >10-bit linear) challenging using conventional pipelined ADC design techniques. Low power consumption in pipelined ADCs is motivated by the fact that low power consumption enables increased battery life and thus increased user productivity in mobile systems. In wired systems where many ADCs can be integrated on-chip in parallel, large net power consumption can generate high amounts of heat requiring expensive packaging for heat dissipation; hence lower power enables more cost-effective packaging. With the green-shift of modern electronics, a paradigm of 'doing more with less' has become a popular mantra in the latest semiconductor systems. In the interest of saving power as well as recycling as much area in an electronic implementation as possible (and thus reducing implementation costs), reconfigurable

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data converters, which can operate at a variety of different operating points have become an emerging area of research. A reconfigurable ADC for example which has its power scale with sampling speed, would allow a single ADC to be used to meet the demands a variety of different standards and/or inputs without using multiple ADCs. As multiple devices and communication protocols are integrated onto single devices such as cell phone, designing flexible reconfigurable electronic systems is emerging as an area of great interest to ADC designers.

This book aims to be of interest to those who are new to pipelined ADCs and those who are seasoned experts in the field. The book is divided into two sections: Section I discusses pipelined ADC design, and Section II discusses pipelined ADC enhancement techniques. Although many topics related to pipelined ADCs are discussed in both sections, the primary focus of the book is on design techniques which (1) improve linearity, (2) enable reconfigurable ADCs, and (3) Facilitate low power consumption. Throughout the book examples of prior art and silicon implementations of state of the art solutions in these areas will be described in detail.

Section I of the book is aimed at those new to pipelined ADCs, where a review of the basic knowledge and design trade-offs required to understand how a pipelined ADC works are detailed. By understanding the conventional approaches used to implement a pipelined ADC it is expected that the casual reader can put together a functional ADC with reasonable specifications. By understanding the conventional approaches used to implement pipelined ADCs the reader will gain an appreciation of the limitations of the conventional approaches, and the motivation of state of the art designs described in the second portion of the book.

The second portion of the book is aimed at those already familiar with the basics of pipelined ADCs. In the second portion of the book four state of the art pipelined ADC designs are reviewed and presented in detail. For each implementation a state of the art architectural innovation which substantially improved on the prior art, with verification in silicon will be discussed. The following are brief summaries of the four pipelined ADC architectures discussed in this book:

1. A topology [2, 3] to rapidly digitally correct for both DAC and gain errors in the multi-bit first stage of an 11-bit pipelined ADC. Using a dual-ADC based approach the digital background scheme is validated with a proof-of-concept prototype fabricated in a 1.8 V, 0.18 μm CMOS process, where the calibration scheme improves the peak INL of a 45 MS/s ADC from 6.4 to 1.1 LSB after calibration. The SNDR/SFDR is improved from 46.9/48.9 dB to 60.1/70 dB after calibration. Calibration is achieved in approximately $10^4$ clock cycles.
2. A 10-bit pipelined ADC which has its average power is scalable with sampling rate over a large variation of sampling rates [4, 5]. Fabricated in a 1.8 V, 0.18 μm CMOS process, the ADC uses a novel Rapid Power-On Opamp to achieve power scalability between sampling rates as high as 50 MS/s (35 mW), and as low as 1 kS/s (15 μW), while achieving 54–56 dB of SNDR (at Nyquist) for all sampling rates. A current modulation technique is used to avoid the less accurate simulation, poorer matching, and increased bias sensitivity associated with