COMPACT MOSFET MODELS FOR VLSI DESIGN

A.B. Bhattacharyya

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Dedication

To my parents to whom I promised in my childhood that I would write a book.

To my wife Pranati, daughters Usree and Urmi, and family members Arun, Isha and Bela, for their selfless sacrifice and support, which allowed me to honor the most sacred of all obligations—the promise to my parents.

Contents

Preface

The microelectronics industry has witnessed an explosive progress in the capability to integrate components on a silicon chip with CMOS as the predominant technology. The present day System-on-Chip (SOC) contains billions of devices with the Metal–Oxide–Semiconductor (MOS) transistor forming the basic building block. The successful design of such a complex integrated system requires extensive computer simulation where an accurate and faithful mathematical description of the MOS transistor is an essential prerequisite. MOS characteristics, therefore, are described by a set of mathematical equations producing a *compact model* for the device. These models are ported into a SPICE circuit simulator for faithful representation of MOSFET characteristics. Models provide the communicating interface between design and manufacturing.

As the complexity and application domains of silicon chips continue to enlarge, the challenge to satisfy apparently conflicting conditions of precision and simplicity is demanding and formidable. The litmus test of a compact model describing the MOS transistor lies in its capability to describe the device characteristics in a way that it is computationally efficient and reliable to handle simulation of ever increasing complex circuits of an electronic system ensuring cost effectiveness and fast turn around time. Further, the model needs to be scalable, predictive for the generations of technology nodes to follow, and capable of addressing statistical process variations. With such multidimensional requirements, different approaches have emerged which can be broadly categorized as *Engineering models, Physical models, and Application Specific hybrid models*.

Historically, development of the threshold voltage, V_T, based compact MOSFET model was pioneered by the University of California, Berkeley (UCB) and placed in the public domain. MOSIS (MOS Implementation Service) provides to the customers parameters for UCB models for a specified technology. The pedagogical approach, interfacing design with technology, has consequently been exclusively through V_T based models. However, there have been developments in recent years which have led to a paradigm shift. Apart from the threshold voltage based method, new approaches using inversion charge and surface potential as state variables have emerged, providing a new perspective in the field of compact models. PSP is already recognized as an alternative standard for the compact MOSFET model.

The measured characteristics reflecting various phenomena related to the device is the ultimate physical reality as far as users are concerned. The *perceived* model representations for the same phenomena, however, may be altogether different depending on the framework on which the model is structured. In the VLSI community, technologists use the model parameters to project the *most* optimistic limit of the MOSFET performance, making parameter extraction as important as model development. Designers, on the other hand, judge the model parameters

from the perspective of technological details revealed, and their compliance to simulation requirements such as convergence, etc.

Scaling of feature size of MOSFETs is associated with ever increasing number of model parameters. Thus, VLSI designers are confronted with a complex situation which forces them to handle a large number of parameters for a given model. Further, they need to make a judicious choice from a multiplicity of competing models. The formation of the Compact Model Council (CMC), more of an industry response, has been a natural and inevitable development for providing benchmarks and standards for compact models. As there is very little possibility that a single model will be able to meet the requirements of a wide range of application domains, the diversity of models has to be accepted as a reality. Thus, VLSI designers need to be better informed and broadly educated with *inclusive* coverage of various compact MOSFET models, as against the prevailing practice of training on a specific or an *exclusive* model. However, the emerging pattern in the field of the compact MOSFET model rarely gets reflected in VLSI education in undergraduate and postgraduate courses. On the other hand, cutting edge insights of new perceptions can stimulate the students and model users to a deeper understanding of the models. This will lead to a class of educated model consumers capable of exploiting the models judiciously.

The objective of the author is to create awareness regarding the different approaches prevalent in compact MOSFET modeling in a single text at an introductory level. The present text is the outcome of a project initiated by the author over the last six years in organizing broad-based courses on compact MOSFET models supporting VLSI design at both the undergraduate and postgraduate levels. Selected topics from the material given in this text have also formed the basis for customized modular courses on VLSI design for industry professionals. The author received encouragement from both the academic and industry communities for preparing a text that highlights the core concepts of different models, which can prepare the foundation for further model-specific specialization.

The text has been organized in such a way that it is self-contained. It summarizes in Chapter 1 the basic equations of semiconductor physics necessary for understanding phenomena related to MOS transistors. Chapter 2 deals with an ideal MOS capacitor structure, where the basic concepts and equations that are required to understand various compact models are developed. In Chapter 3 non-ideal effects, which are an integral part of real world practical MOS structures, are considered as add-on phenomena or perturbations over the ideal structure. Keeping in view the fact that the ITRS projected scaled MOSFET performance targets require intervention of non-classical structures, the basic MOS capacitor platform has been discussed with potential gate and channel engineering alternatives requiring the use of an Si–Ge heterostructure and undoped silicon as the substrate, and the use of a high-k dielectric as a replacement of the silicon–dioxide gate dielectric. Chapter 4 presents the formulation of four types of compact models, namely, V_T based models, charge based models, and two surface-potential based models. Chapter 5 deals with the effects of scaling on MOS transistor characteristics, and discusses how such phenomena are integrated into the various compact models. Chapter 6 presents dynamic MOSFET models in quasistatic and non-quasistatic conditions outlining approaches of the BSIM, EKV, HiSIM, and PSP models. The noise model has also been presented briefly. Quantum mechanical effects in nanoscale-MOSFETs have been outlined in Chapter 7. The final chapter is on emerging non-classical structures which hold the prospect to replace mainstream conventional bulk CMOS structures. The basic equations for a double gate MOSFET, which is projected to spearhead nanoscale CMOS, are derived.

There is modularity in the organization of the chapters which enables the reader to be selective. The field trials carried out by the author for undergraduate and postgraduate courses are as follows: at both undergraduate and postgraduate levels the materials which are generic are discussed as core material. For undergraduates, the course was not for beginners but for those who opted for the course on compact MOSFET models as an elective for specializing in VLSI design. The core material prepares the platform on which any particular model can be launched. At the undergraduate level, the author experimented with threshold voltage based models for classroom teaching, using the EKV approach for assignments. PSP/HiSIM was referred only qualitatively. The non-classical structures, quantum effects, and non-quasistatic models were not part of curriculum. At the postgraduate level, threshold voltage based models formed the classroom teaching material, and PSP/HiSIM constituted the assignment activity. EKV was referred qualitatively. The non-classical MOSFET structure, non-quasistatic effect, quantum phenomena and noise form the core material at the postgraduate level. Modularity in the presentation of topics, built in the text, allows flexibility to the instructor to mix and match the content with the requirement of the course. Proficiency in the use of a Computer Algebra System (CAS) is helpful, as compact model equations can be simulated. Such activity can form an important component of assignments.

As more than one category of compact models have been presented in the text, it has been impractical to impose a common list of symbols globally. This would have required modifications to all compact model equations with symbols that differ from those given in the corresponding model documentation. As readers are expected to turn to the official documentation of a specific compact model for details, such a change in symbols would create unnecessary confusion. Hence, a set of generic symbols, which relate to core material on MOS physics independent of model framework specifics, has been identified. The symbols of specific models, by and large, have been kept intact, and have been defined locally wherever used.

The book discusses model equations for highlighting the conceptual framework, and selects them based on suitability from a pedagogical viewpoint. Therefore, equations for the latest version have not necessarily been considered to be the most suitable for introducing a model. At times, an earlier version happens to be a more convenient entry point to the model. The selection of model equations in the text has to be viewed from this perspective. The framework of each class of model being different, the emphasis of the author has been to get the readers initiated to the core concepts that form the basis of an approach, rather than on evolutionary improvements in a given approach. The text is neither a handbook, nor a replacement to the official documentation available for each category of models. Further, as the models are regularly upgraded, the model equations used in the book do not necessarily reflect the current status of a model. For some models information was sketchy and restricted. At many places, the text has used equations suitably truncated to serve the limited objective of pedagogy. Therefore, the readers are again advised to refer to the official documentation for the selected model.

In the presentation of models the author has taken the position to be non-judgmental on the merits, suitability, or otherwise, of a given model, leaving the reader to draw his/her own conclusions. The extent of coverage of a given model, at times, has been dictated by the availability of materials rather than assignment of any planned weightage on the coverage.

The text will be supported by a solution manual for instructors, which will be available from the publisher's website for the book. The simulation plots given in the text have mostly

been implemented using MATLAB. The source code for these simulations shall also be made available. These important and useful supplements can be found at the following URL: http://www.wiley.com/go/bhattacharyya.

It is believed that the broad pedagogical presentation of various models will bring them out of the captive domain of the few select industries using them for design and product development. Increased awareness regarding the various compact models available will hopefully lead to wider participation in benchmarking the performance and evaluation of the models. The author believes that such widespread participation from universities, through courses on compact models, will culminate in foundries providing model parameters for *all* categories of models. This will allow VLSI designers to make optimal use of the possibilities provided by the diversity of compact models.

A. B. Bhattacharyya
Noida, Uttar Pradesh
India

Acknowledgements

I express my gratitude for the grace and blessings I received from my mentors, academic and spiritual, but for whom I could not have overcome many insurmountable roadblocks which came on the way since the project of writing a book on compact models for VLSI design was launched at the University of Goa, about five years ago. Prof. B. S. Sonde and Prof. P. R. Sarode provided the initial support. The author initiated an academic program where the compact MOSFET model, *albeit* in a small way, formed the nucleus of the concept of bringing different categories of MOSFET models as a part of the curriculum. At a later stage, MOSFET compact model related topics formed the course content at the Jaypee Institute of Information Technology University (JIITU), NOIDA (India), both at the undergraduate and the postgraduate level. The author records his appreciation for Gajanan Dessai, for useful interaction as a student, having participated in model related courses delivered by the author both at Goa University and at JIITU. His involvement later transcended beyond the classroom assignments. His contribution in Chapter 7 is specially acknowledged. He was also associated with the implementation of simulations for the text and the solution manual. The following students of JIITU made supporting contributions for the solution manual: Umang Sah, Parul Gupta, Ankur Srivastava, Yashshri Negi, Kirminder Singh, Saurabh Chaturvedi, Nishant Chandra, and Apoorva Yati. No less has been the influence of my doctoral, postgraduate, and undergraduate students whose enthusiasm has been responsible for my remaining abreast with the current state of developments in microelectronics. Prof. M. S. Tyagi provided useful editorial suggestions for Chapter 1. The timely help from Dr Manoj Saxena, University of Delhi, for his contributions and review on MOSFET noise, is thankfully acknowledged. Rohit Sharma assisted the author in checking the manuscript of a few chapters. Usree Bhattacharya contributed significantly in arranging reference materials which was immensely useful. Urmi Battu offered her bit in helping me with the illustrations.

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relating MOSFET models with VLSI design, when the author was with them on a sabbatical. Prof. Kinnen's practical suggestions regarding how not to get lost in the expanding MOS universe, and his abiding interest in the project, have been extremely refreshing.

The works of the authors of various compact modeling groups have been referred to frequently, as their models have been the subject of discussion. The book, however, has been no less influenced by the work of Prof. C. T. Sah, Prof. J. R. Brews, and Prof. Y. Tsividis. The author is apologetic about the fact that many deserving works might not have been referred to.

The author records his deep appreciation for the sustained support of Prof. Suneet Tuli, Indian Institute of Technology, Delhi, and Prof. D. N. Singh, University of Punjab, Chandigarh, on making available supporting technical literature. The constructive suggestions of unknown reviewers were responsible for the inclusion of some enriching content not originally planned in the book.

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The author is conscious of omissions and the scope for improvement of the book. Suggestions are welcome from readers.

Last but not the least, I have no adequate words to express my gratitude to my colleague Harkesh Singh Dagar, but for whom perhaps the completion of the book would have ever remained so near yet so far. Even though not belonging to the area of VLSI design, the project benefited enormously from his varied knowledge and experience spanning multiple science and engineering disciplines. His knowledge of digital typography also proved indispensable in the preparation of the manuscript. Stimulating and objective discussions with him, free from subjective biases, led to a better appreciation of the limitations of the existing approaches to compact modeling.

Further, he undertook the painful task of carrying out the review of the entire text and the solution manual. His efforts have resulted in the ironing out of inconsistencies in the content, and simplified the presentation. He set up editorial discipline in the absence of which, in spite of all technical content, the book would not have been anywhere near the level attained. His uncanny ability to uncover errors and inconsistencies has hopefully eliminated most blemishes at the pre-production stage. The author owns responsibility for any errors or omissions which remain. I remain indebted to him forever for his selfless effort. I take this opportunity to thank his family, and record my deep appreciation for their self-effacing support and sacrifice, while Harkesh got involved with this project.

This is practice, but remember first to set forth the theory.

Leonardo da Vinci

John Wheeler was an advocate of doing more with less. That is how scientific modeling should be done, rather than heaping on a bunch of parameters to match phenomena—a good model accomplishes more, explains more than what it contains.

Todd Rowland
Academic Director
NKS Summer School
Wolfram Research, Inc.

List of Symbols

Physical Constants

$\epsilon_0 = 8.854 \times 10^{-14}\,\mathrm{F\,cm^{-1}}$	Permittivity of free space
$\epsilon_{\mathrm{Si}} = 11.7\epsilon_0$	Permittivity of Si
$\epsilon_{ox} = 3.97\epsilon_0$	Permittivity of SiO_2
$q = 1.6 \times 10^{-19}\,\mathrm{C}$	Electron charge
$k = 1.38 \times 10^{-23}\,\mathrm{JK^{-1}}$	Boltzmann's constant
$h = 6.63 \times 10^{-34}\,\mathrm{J\,sec}$	Planck's constant
$m = 9.1 \times 10^{-31}\,\mathrm{kg}$	Free electron mass

Select Parameter Values for Silicon

$m_n^* = 0.33$ (relative to unity)	Effective mass of electron
$m_p^* = 0.55$ (relative to unity)	Effective mass of hole

Values at a temperature of 300 K

$n_i = 1.4 \times 10^{10}\,\mathrm{cm^{-3}}$	Intrinsic carrier concentration
$\mu_n = 1400\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$	Electron mobility in bulk silicon
$\mu_p = 500\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$	Hole mobility in bulk silicon
$v_{sat,n} = 8.5 \times 10^6\,\mathrm{cm\,s^{-1}}$	Saturation velocity for electrons
$v_{sat,p} = 5.0 \times 10^6\,\mathrm{cm\,s^{-1}}$	Saturation velocity for holes
$F_{c,n} = 2.5 \times 10^3\,\mathrm{V\,cm^{-1}}$	Critical electric field for electron saturation velocity
$F_{c,p} = 2.5 \times 10^3\,\mathrm{V\,cm^{-1}}$	Critical electric field for hole saturation velocity

Dimensions

L_G	Mask defined gate length
$L = L_G - 2L_D$	Channel length
L_D	Length of lateral diffusion from source/drain under the gate
L_e	Corrected channel length in saturation
$L(S, D)$	Length of source, drain diffusion region in the direction of channel
L_b	Debye length
ΔL	Length of pinched-off/high field region near drain
L_n	Electron diffusion length
L_p	Hole diffusion length
$\bar{l}$	Mean free path
l	Characteristic length (context dependent)
$W = W_g - 2DW$	Effective channel width

W_d	Width of depletion region
W_{ds}	Depletion width at source
W_{dd}	Depletion region at source
W_{dc}	Channel depletion width
W_{dm}	Maximum width of depletion region at threshold
W_{dps}	Depletion width in polysilicon
W_i	Inversion layer thickness
W_I	Implant depth
W_E	Equivalent depletion layer depth source/drain
X_j	Source/drain junction depth
T_{ox}	Gate oxide thickness
T_{fox}	Field oxide thickness
a_0	Lattice constant of silicon
x	Direction perpendicular to channel
y	Direction parallel to channel

Doping and Carrier Concentrations

N_B	Bulk impurity doping volume concentration
N_D	Donor impurity doping volume concentration
N_A	Acceptor impurity doping volume concentration
n_{n0}	Electron concentration in n-type Si at thermal equilibrium
p_{n0}	Hole concentration in n-type Si at thermal equilibrium
N_P	Polysilicon doping concentration
N_c	Effective density of states in conduction band (cm^{-3})
N_v	Effective density of states in valence band (cm^{-3})
n_n	Non-equilibrium free electron density in n-type Si
p_p	Non-equilibrium free hole density in p-type Si
n_p	Non-equilibrium free electron density in p-type Si
p_n	Non-equilibrium free hole density in n-type Si
n_i	Instrinsic carrier concentration
n_{ie}	Effective instrinsic carrier concentration
n^+	Highly doped n-region
N_I	Implant layer doping volume concentration
N_E	Equivalent transformed doping volume concentration for inhomogeneous substrate

Energy

E	Energy
E_c	Lower edge of the conduction energy band
E_{cb}	Lower edge of the conduction band of the bulk (substrate) material
E_{cg}	Lower edge of the conduction band of the gate material
E_v	Upper edge of the valence energy band
E_f	Fermi energy level
E_g	Energy band gap (eV)
ΔE_g	Energy band gap narrowing
χ_{Si}	Electron affinity for Si (eV)
E_i	Intrinsic Fermi level
E_d	Donor energy level
E_a	Acceptor energy level

E_{fg}	Fermi energy level of gate material
E_{fn}	Quasi-Fermi energy level for electrons
E_{fp}	Quasi-Fermi energy level for holes

Voltages and Currents

ϕ_g	Potential corresponding to work function of gate material
ϕ_{Si}	Potential corresponding to work function of Si
ϕ	Electrostatic potential
ϕ_F	Fermi potential
ϕ_f	Bulk potential; the potential difference between Fermi and intrinsic energy level
ϕ_t	Thermal voltage ($= kT/q$)
ϕ_s	Surface potential with reference to bulk
ϕ_{ss}	Surface potential with reference to source
ϕ_{sS}	Surface potential at source end of the channel
ϕ_{sD}	Surface potential at drain end of the channel
Φ_b	Conduction band offset between Si–SiO_2
ϕ_{bi}	Built-in potential barrier across junction
ϕ_{gs}	Potential corresponding to work function difference between gate and substrate
ϕ_n	Quasi-Fermi potential of electrons
ϕ_p	Potential drop across polysilicon depletion layer
ϕ_{sm}	Surface potential at midpoint of the channel ($L/2$)
ϕ_0	Surface potential at onset of strong inversion
$\Delta\phi_0$	Drain induced barrier lowering w.r.t. source
ϕ_i	Potential at high–low/low–high transition point in inhomogeneous substrate
V_{GB}	Gate voltage w.r.t. bulk
V_{DB}	Drain voltage w.r.t. bulk
V_{SB}	Source voltage w.r.t. bulk
V_{ox}	Voltage drop across gate oxide
V_{DS}	Drain voltage w.r.t. source
V_{GS}	Gate voltage w.r.t. source
V_{CB}	Channel potential w.r.t. bulk
V_{DG}	Drain to gate voltage
V_{CS}	Channel potential w.r.t. source
V_{fb}	Flat band voltage
V_T	Threshold voltage
V_{T0}	Threshold voltage without substrate bias
V_{TB}	Threshold voltage w.r.t. bulk
V_{TS}	Threshold voltage w.r.t. source
V_{MI}	Gate voltage corresponding to $\phi_s = 2\phi_F$
V_{WI}	Gate voltage corresponding to $\phi_s = \phi_F$
V_{SI}	Gate voltage corresponding to $\phi_s = (2\phi_F + m\phi_t)$
V_{DSsat}	Drain current saturation voltage
V_P	Pinch-off voltage
I_{DSsat}	Saturation drain current
I_{DS}	Drain to source current
I	Current

I_{diff}	Diffusion current
I_{drift}	Drift current
I_{DB}	Drain to bulk current
I_{sub}	Substrate current due to hot electrons
I_G	Gate current
I_{GS}	Gate to source tunneling current
J	Current density
$J_{n,diff}$	Diffusion current density due to electrons
$J_{p,diff}$	Diffusion current density due to holes
$J_{n,drift}$	Drift current density due to electrons
$J_{p,drift}$	Drift current density due to holes
TC	Tunneling coefficient
S	Supply function

Charges

Q'_b	Bulk charge density per unit area
Q'_{bm}	Maximum bulk charge density per unit area
Q'_n	Inversion layer charge density per unit area
Q'_g	Gate charge density per unit area
Q'_{sc}	Surface space charge density per unit area
Q'_f	Fixed oxide charge density per unit area in SiO_2
Q'_m	Mobile charge density per unit area in SiO_2
Q'_{it}	Interface trapped charge density per unit area
Q'_{ot}	Oxide trapped charge density per unit area
Q_s	Total inversion charge assigned to source
Q_d	Total inversion charge assigned to drain
ρ	Volume space charge density per unit volume

Capacitances

C'_{ox}	Oxide capacitance per unit area
C'_{sc}	Space charge capacitance per unit area
C'_b	Depletion layer capacitance per unit area
C'_n	Inversion layer capacitance per unit area
C'_{eq}	Equivalent gate–substrate capacitance per unit area
C'_{min}	Minimum gate–bulk capacitance per unit area
C'_{dmin}	Minimum depletion capacitance per unit area
C'_{fb}	Flat band capacitance per unit area
C_{diff}	Diffusion capacitance
C'_j	Junction capacitance per unit area
C'_{j0}	Zero bias junction capacitance per unit area
C_{gs}	Gate–source intrinsic capacitance
C_{gd}	Gate–drain intrinsic capacitance
C_{gb}	Gate–bulk intrinsic capacitance
C_{bs}	Bulk–source intrinsic capacitance
C_{bd}	Bulk–drain intrinsic capacitance
$C_{ox} = C'_{ox}WL$	Total oxide capacitance
C_{ov}	Total gate to source/drain capacitance

1

Semiconductor Physics Review for MOSFET Modeling

1.1 Introduction

The idea of controlling electric current through the field effect on a semiconductor surface dates back to as early as 1930. It was proposed in a patent claim by Lilienfeld which forms the conceptual framework of present day MOSFET operation [1]. From the account of the evolution of the MOS transistor, as outlined by Sah [2], it appears that MOS technology did not emerge primarily as a consequence of a focussed pursuit to realize Lilienfeld's field effect concept, but as a by-product of a series of revolutionary developments in the field of solid-state electronics. These developments include the invention of point contact and junction bipolar transistors by Bardeen [3], and Shockley [4], innovations in planar technology and selective diffusion through windows etched in oxide as demonstrated by Hoerni [5], integration of passive and active components by Kilby [6], to name only a few landmark milestones. These technological capabilities enabled the realization of the Metal–Oxide–Semiconductor Field Effect Transistor (MOSFET) structure by Kahng and Atalla [7–9], which was considered suitable for replacement of prevailing bipolar integrated transistor logic circuits. The complementary PMOS–NMOS inverter structure by Wanlass and Sah [10] provided a defining innovation which heralded the CMOS digital era. While the realization of MOSFET on silicon took about as long as thirty years, taking the initial patent as the reference in the time scale, the history of the *subsequent* development and scaling phase driven by Moore's law has been breathtaking [14]. The acronym MOS, originally signifying a Metal–Oxide–Semiconductor structure, has now become synonymous with Microsystem-On-Silicon [12].

After the initial metal gate form, the *polysilicon gate* MOS structure has been central to continuous MOS technology upgradation [11]. Its essential constituents are shown in Figure 1.1 and illustrated below.

(i) A *single crystal* silicon serves as the substrate at the surface of which the field effect transistor action is manifested. At the interface of the silicon substrate and the gate dielectric layer, a channel of mobile carriers is formed by the application of a gate voltage which

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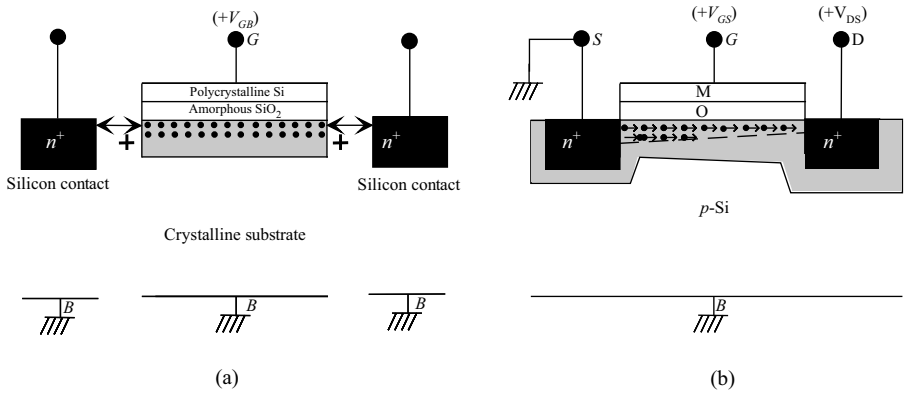

Figure 1.1 Components of the field effect transistor structure: (a) MOS capacitor and contacts; (b) composite MOSFET device

controls the conductivity of the channel. For the device to be reproducible and reliable, it is obligatory that the substrate material be a single crystal where *atoms are arranged in an orderly array*.

(ii) A silicon-dioxide layer is integrated with the substrate at the top of the silicon surface which insulates the silicon substrate from the gate electrode. The insulating film is structurally *amorphous* where *no perceivable long-range crystalline order exists*.

(iii) Over the insulating dielectric a *polysilicon* film is deposited where *a relatively small segment of the film has an ordered crystalline order*. The poly-layer at the top serves as the gate electrode, and is heavily doped to make its conductivity approach that of a metal. Though high conductivity polycrystalline silicon replaces the original metal electrode on top of the gate oxide, it continues to be labelled as a metal as a historic continuity of the nomenclature of MOS for the device structure.

(iv) Finally, *ohmic* contacts are established with the polysilicon layer at the top and the silicon substrate at the bottom, for which aluminum has been the most commonly used material. The stack of the above three layers, with the top and bottom electrodes designated as *Gate* and *Bulk* terminals, respectively, provide the platform for *Field Effect* characteristics.

(v) The two terminal MOS capacitor described above, provides the platform to observe the *Field Effect* phenomenon at the Si–SiO_2 interface in the form of a gate controlled space charge constituted by mobile carriers and fixed bulk charges. The mobile carriers induced at the silicon substrate under the gate at the interface are connected to the external world through *conducting silicon probes* of the *same conductivity* as that of the mobile carriers in the channel. The external voltage applied at the two end terminals results in a current which is controlled by the gate field. The basic *four terminal* MOSFET structure shown in Figure 1.1 is formed by *integrating* the diffusion contacts with the MOS capacitor on a common substrate. The capacitor under the gate forms the *intrinsic* part of the MOS transistor, whereas the contact terminals form the *extrinsic* part of the device.

MOS technology has undergone unprecedented evolution to keep pace with projection on *scaling* as envisaged by Gordon Moore [14]. Unlike the pre-birth history of the MOS transistor, the future has been made almost predictive. The International Technology Roadmap for

Semiconductor (ITRS) lays down projections for a comprehensive development of MOS technology which is indicative of the trends, tasks, challenges, and opportunities in the years ahead in terms of process integration, system development, materials, device architecture, bottlenecks, etc. The document is dynamically updated. Table 1.1 is an illustrative projection [13].

Table 1.1 ITRS 2003 roadmap for high-performance logic

Year	2003	2006	2009	2012	2015	2018
Technology node (nm)	100	70	50	35	25	18
MPU gate length (nm)	45	28	20	14	10	7
V_{dd} (V)	1.2	1.1	1.0	0.9	0.8	0.7
T_{ox} (Å)	13	10	8	7	6	5
Clock frequency (MHz)	2 976	6 783	12 369	20 065	33 403	53 207
Maximum power (W)	149	180	210	240	270	300
Static power (W/μm)	4.0×10^{-7}	6.1×10^{-7}	7.7×10^{-7}	9.9×10^{-7}	2.6×10^{-6}	3.9×10^{-6}
Nominal gate delay (ps)	30.24	18.92	12.06	7.47	4.45	2.81
Power delay product (J/μm)	1.4×10^{-15}	9.7×10^{-15}	7.7×10^{-16}	4.8×10^{-16}	3.0×10^{-16}	1.7×10^{-16}
Transistors per chip ($\times 10^6$)	153	307	614	1227	2454	4908

Though the basic MOS structure remains the core of development forecast, the primitive Metal–Oxide–Semiconductor has evolved into a significant complex structure which resembles a stack of multiple layers of varying properties and increasing number of interfaces as shown in Figure 1.2 due to the requirements of gate, channel, and interface engineering.

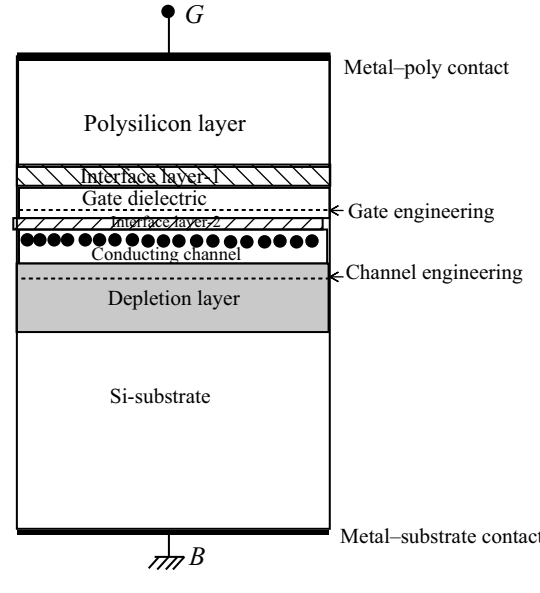

Figure 1.2 Stacked layers and interfaces in the evolving MOS structure

The channel engineering has resulted in substrate *inhomogeneity, stratification, and heterogeneity* of material near the Si–SiO_2 interface as shown by dashed lines. The gate engineering has lead to stacking of dielectric layers to avoid tunneling through the thin gate insulator. The *transitions* at the interfaces are not abrupt, introducing effectively transition layers with graded material composition. Thus, the device characteristics and modeling are closely linked with the properties of the materials forming the layers. With miniaturization, the dimensions correspond to only a few atomic layers, where quantum effects start governing the device physics.

The inputs required for MOSFET modeling are: material properties, device structure and dimensions, process details, parameters related to carrier statistics, mobility, band gap narrowing, carrier recombination, generation and multiplication, quantization and tunnelling effects, etc. The present chapter provides a brief summary of the above aspects, more in the form of statements, for the purpose of ready reference without going to details which are available in a number of texts on the subject [17–22].

1.2 Crystal Planes

The crystal structure of silicon (Si) is *diamond cubic* type, where each atom makes covalent bonds with four neighboring atoms to form a tetrahedral structure. In a MOSFET, the device characteristics depend on the crystal plane on which the device is fabricated. In a crystal structure, the orientation of planes is defined by Miller indices, which are expressed by a set of integer numbers. The procedure to obtain Miller indices of a crystal plane is explained through an illustration shown in Figure 1.3, where x, y, and z define the directions of the primitive vectors of the lattice.

- **Step1:** Find the intercept of the plane under consideration in terms of the *axial units* along the axes. In Figure 1.3 the intercepts are A, B, and C where $A = 3$, $B = 2$, and $C = 2$ units.
- **Step2:** Take reciprocals of the intercepts which, for the present case, are: $1/A$, $1/B$, and $1/C$, i.e. $1/3$, $1/2$, and $1/2$ respectively.
- **Step3:** Get the common denominator D of the intercepts A, B, and C. Multiplying the reciprocal numbers by D we get the sets of numbers defining the Miller indices (h, k, l) where $h = D/A$, $k = D/B$, and $l = D/C$, i.e. (2, 3, 3) for the plane under consideration.

In case a plane is parallel to an axis, the intercept of the plane with the above axis is taken as infinity and the reciprocal of the intercept becomes $1/\infty = 0$.

Figure 1.3 shows the (100) plane in a cubic crystal. The preferred orientation of the plane of a silicon crystal for fabrication of conventional MOS devices is (100) with SiO_2 as the dielectric

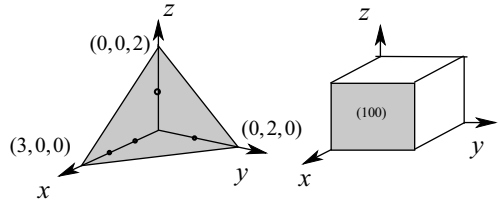

Figure 1.3 Crystal plane representation in a lattice