This page intentionally left blank
### Multipliers

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>terra</td>
<td>T</td>
<td>$10^{12}$</td>
</tr>
<tr>
<td>giga</td>
<td>G</td>
<td>$10^9$</td>
</tr>
<tr>
<td>mega</td>
<td>M (MEG in SPICE)</td>
<td>$10^6$</td>
</tr>
<tr>
<td>kilo</td>
<td>k</td>
<td>$10^3$</td>
</tr>
<tr>
<td>milli</td>
<td>m</td>
<td>$10^{-3}$</td>
</tr>
<tr>
<td>micro</td>
<td>μ (or u)</td>
<td>$10^{-6}$</td>
</tr>
<tr>
<td>nano</td>
<td>n</td>
<td>$10^{-9}$</td>
</tr>
<tr>
<td>pico</td>
<td>p</td>
<td>$10^{-12}$</td>
</tr>
<tr>
<td>femto</td>
<td>f</td>
<td>$10^{-15}$</td>
</tr>
<tr>
<td>atto</td>
<td>a (not used in SPICE)</td>
<td>$10^{-18}$</td>
</tr>
</tbody>
</table>

### Physical Constants

<table>
<thead>
<tr>
<th>Name</th>
<th>Symbol</th>
<th>Value/Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vacuum dielectric constant</td>
<td>$\varepsilon_0$</td>
<td>8.85 aF/μm</td>
</tr>
<tr>
<td>Silicon dielectric constant</td>
<td>$\varepsilon_{si}$</td>
<td>11.7$\varepsilon_0$</td>
</tr>
<tr>
<td>SiO$_2$ dielectric constant</td>
<td>$\varepsilon_{ox}$</td>
<td>3.97$\varepsilon_0$</td>
</tr>
<tr>
<td>SiN$_3$ dielectric constant</td>
<td>$\varepsilon_{si}$</td>
<td>16$\varepsilon_0$</td>
</tr>
<tr>
<td>Boltzmann’s constant</td>
<td>$k$</td>
<td>$1.38 \times 10^{-23}$ J/K</td>
</tr>
<tr>
<td>Electronic charge</td>
<td>$q$</td>
<td>$1.6 \times 10^{-19}$ C</td>
</tr>
<tr>
<td>Temperature</td>
<td>$T$</td>
<td>Kelvin</td>
</tr>
<tr>
<td>Thermal voltage</td>
<td>$V_T$</td>
<td>$kT/q = 26$ mV @ 300K</td>
</tr>
</tbody>
</table>
CMOS
No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, recording, scanning, or otherwise, except as permitted under Section 107 or 108 of the 1976 United States Copyright Act, without either the prior written permission of the Publisher, or authorization through payment of the appropriate per-copy fee to the Copyright Clearance Center, Inc., 222 Rosewood Drive, Danvers, MA 01923, (978) 750-8400, fax (978) 750-4470, or on the web at www.copyright.com. Requests to the Publisher for permission should be addressed to the Permissions Department, John Wiley & Sons, Inc., 111 River Street, Hoboken, NJ 07030, (201) 748-6011, fax (201) 748-6008, or online at http://www.wiley.com/go/permission.

Limit of Liability/Disclaimer of Warranty: While the publisher and author have used their best efforts in preparing this book, they make no representations or warranties with respect to the accuracy or completeness of the contents of this book and specifically disclaim any implied warranties of merchantability or fitness for a particular purpose. No warranty may be created or extended by sales representatives or written sales materials. The advice and strategies contained herein may not be suitable for your situation. You should consult with a professional where appropriate. Neither the publisher nor author shall be liable for any loss of profit or any other commercial damages, including but not limited to special, incidental, consequential, or other damages.

For general information on our other products and services or for technical support, please contact our Customer Care Department within the United States at (800) 762-2974, outside the United States at (317) 572-3993 or fax (317) 572-4002.

Wiley also publishes its books in a variety of electronic formats. Some content that appears in print may not be available in electronic format. For information about Wiley products, visit our web site at www.wiley.com.

Library of Congress Cataloging-in-Publication Data:
Baker, R. Jacob, 1964-
p. cm.
Summary: "The third edition of CMOS: Circuit Design, Layout, and Simulation continues to cover the practical design of both analog and digital integrated circuits, offering a vital, contemporary view of a wide range of analog/digital circuit blocks, the BSIM model, data converter architectures, and much more. The 3rd edition completes the revised 2nd edition by adding one more chapter (chapter 30) at the end, which describes on implementing the data converter topologies discussed in Chapter 29. This additional, practical information should make the book even more useful as an academic text and companion for the working design engineer. Images, data presented throughout the book were updated, and more practical examples, problems are presented in this new edition to enhance the practicality of the book"— Provided by publisher.
Summary: "The third edition of CMOS: Circuit Design, Layout, and Simulation continues to cover the practical design of both analog and digital integrated circuits, offering a vital, contemporary view of a wide range of analog/digital circuit blocks, the BSIM model, data converter architectures, and much more"— Provided by publisher.
ISBN 978-0-470-88132-3 (hardback)
TK7871.99.M44B35 2010
621.39732—dc22
2010016630

Printed in the United States of America.
10 9 8 7 6 5 4 3 2 1
To my wife Julie
Contents

Preface xxxi

Chapter 1 Introduction to CMOS Design 1
  1.1 The CMOS IC Design Process ....................... 1
    1.1.1 Fabrication 3
    Layout and Cross-Sectional Views 4
  1.2 CMOS Background ................................. 6
    The CMOS Acronym 6
    CMOS Inverter 7
    The First CMOS Circuits 7
    Analog Design in CMOS 8
  1.3 An Introduction to SPICE .......................... 8
    Generating a Netlist File 8
    Operating Point 9
    Transfer Function Analysis 10
    The Voltage-Controlled Voltage Source 11
    An Ideal Op-Amp 12
    The Subcircuit 13
    DC Analysis 13
    Plotting IV Curves 14
    Dual Loop DC Analysis 15
    Transient Analysis 15
    The SIN Source 16
    An RC Circuit Example 17
    Another RC Circuit Example 18
    AC Analysis 19
    Decades and Octaves 20
    Decibels 20

vii
<table>
<thead>
<tr>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design Rules for the Well</td>
</tr>
<tr>
<td>SEM Views of Wells</td>
</tr>
</tbody>
</table>

**Chapter 3 The Metal Layers** | 59 |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 The Bonding Pad</td>
<td>59</td>
</tr>
<tr>
<td>3.1.1 Laying Out the Pad I</td>
<td>60</td>
</tr>
<tr>
<td>Capacitance of Metal-to-Substrate</td>
<td>60</td>
</tr>
<tr>
<td>Passivation</td>
<td>62</td>
</tr>
<tr>
<td>An Important Note</td>
<td>62</td>
</tr>
<tr>
<td>3.2 Design and Layout Using the Metal Layers</td>
<td>63</td>
</tr>
<tr>
<td>3.2.1 Metal1 and Via1</td>
<td>63</td>
</tr>
<tr>
<td>An Example Layout</td>
<td>63</td>
</tr>
<tr>
<td>3.2.2 Parasitics Associated with the Metal Layers</td>
<td>64</td>
</tr>
<tr>
<td>Intrinsic Propagation Delay</td>
<td>65</td>
</tr>
<tr>
<td>3.2.3 Current-Carrying Limitations</td>
<td>68</td>
</tr>
<tr>
<td>3.2.4 Design Rules for the Metal Layers</td>
<td>69</td>
</tr>
<tr>
<td>Layout of Two Shapes or a Single Shape</td>
<td>69</td>
</tr>
<tr>
<td>A Layout Trick for the Metal Layers</td>
<td>69</td>
</tr>
<tr>
<td>3.2.5 Contact Resistance</td>
<td>70</td>
</tr>
<tr>
<td>3.3 Crosstalk and Ground Bounce</td>
<td>71</td>
</tr>
<tr>
<td>3.3.1 Crosstalk</td>
<td>71</td>
</tr>
<tr>
<td>3.3.2 Ground Bounce</td>
<td>72</td>
</tr>
<tr>
<td>DC Problems</td>
<td>72</td>
</tr>
<tr>
<td>AC Problems</td>
<td>72</td>
</tr>
<tr>
<td>A Final Comment</td>
<td>74</td>
</tr>
<tr>
<td>3.4 Layout Examples</td>
<td>75</td>
</tr>
<tr>
<td>3.4.1 Laying Out the Pad II</td>
<td>75</td>
</tr>
<tr>
<td>3.4.2 Laying Out Metal Test Structures</td>
<td>78</td>
</tr>
<tr>
<td>SEM View of Metal</td>
<td>79</td>
</tr>
</tbody>
</table>

**Chapter 4 The Active and Poly Layers** | 83 |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1 Layout Using the Active and Poly Layers</td>
<td>83</td>
</tr>
<tr>
<td>The Active Layer</td>
<td>83</td>
</tr>
<tr>
<td>The P- and N-Select Layers</td>
<td>84</td>
</tr>
<tr>
<td>The Poly Layer</td>
<td>86</td>
</tr>
<tr>
<td>Self-_aligned Gate</td>
<td>86</td>
</tr>
<tr>
<td>The Poly Wire</td>
<td>88</td>
</tr>
<tr>
<td>Silicide Block</td>
<td>89</td>
</tr>
<tr>
<td>4.1.1 Process Flow</td>
<td>89</td>
</tr>
</tbody>
</table>
Damascene Process Steps 90
4.2 Connecting Wires to Poly and Active ................................. 92
Connecting the P-Substrate to Ground 93
Layout of an N-Well Resistor 94
Layout of an NMOS Device 95
Layout of a PMOS Device 96
A Comment Concerning MOSFET Symbols 96
Standard Cell Frame 97
Design Rules 98
4.3 Electrostatic Discharge (ESD) Protection ......................... 100
Layout of the Diodes 100
Chapter 5 Resistors, Capacitors, MOSFETs 105
5.1 Resistors ........................................................................ 105
Temperature Coefficient (Temp Co) 105
Polarity of the Temp Co 106
Voltage Coefficient 107
Using Unit Elements 109
Guard Rings 110
Interdigitated Layout 110
Common-Centroid Layout 111
Dummy Elements 113
5.2 Capacitors ....................................................................... 113
Layout of the Poly-Poly Capacitor 114
Parasitics 115
Temperature Coefficient (Temp Co) 116
Voltage Coefficient 116
5.3 MOSFETs ...................................................................... 116
Lateral Diffusion 116
Oxide Encroachment 116
Source/Drain Depletion Capacitance 117
Source/Drain Parasitic Resistance 118
Layout of Long-Length MOSFETs 120
Layout of Large-Width MOSFETs 121
A Qualitative Description of MOSFET Capacitances 123
5.4 Layout Examples ........................................................... 125
Metal Capacitors 125
Polysilicon Resistors 127
## Chapter 6 MOSFET Operation

### 6.1 MOSFET Capacitance Overview/Review
- Case I: Accumulation 132
- Case II: Depletion 133
- Case III: Strong Inversion 133
- Summary 135

### 6.2 The Threshold Voltage
- Contact Potentials 137
- Threshold Voltage Adjust 140

### 6.3 IV Characteristics of MOSFETs
- 6.3.1 MOSFET Operation in the Triode Region 141
- 6.3.2 The Saturation Region 143
- Cgs Calculation in the Saturation Region 145

### 6.4 SPICE Modeling of the MOSFET
- Model Parameters Related to $V_{THN}$ 146
- Long-Channel MOSFET Models 146
- Model Parameters Related to the Drain Current 146
- SPICE Modeling of the Source and Drain Implants 147
- Summary 147

6.4.1 Some SPICE Simulation Examples 148
- Threshold Voltage and Body Effect 148

### 6.5 Short-Channel MOSFETs
- Hot Carriers 151
- Lightly Doped Drain (LDD) 151
- 6.5.1 MOSFET Scaling 152

### 6.5.2 Short-Channel Effects
- Negative Bias Temperature Instability (NBTI) 153
- Oxide Breakdown 154
- Drain-Induced Barrier Lowering 154
- Gate-Induced Drain Leakage 154
- Gate Tunnel Current 154

### 6.5.3 SPICE Models for Our Short-Channel CMOS Process
- BSIM4 Model Listing (NMOS) 154
- BSIM4 Model Listing (PMOS) 156
- Simulation Results 157
## Chapter 7 CMOS Fabrication by Jeff Jessing

<table>
<thead>
<tr>
<th>Section</th>
<th>Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.1 CMOS Unit Processes</td>
<td>161</td>
</tr>
<tr>
<td>7.1.1 Wafer Manufacture</td>
<td>161</td>
</tr>
<tr>
<td>Metallurgical Grade Silicon (MGS)</td>
<td>162</td>
</tr>
<tr>
<td>Electronic Grade Silicon (EGS)</td>
<td>162</td>
</tr>
<tr>
<td>Czochralski (CZ) Growth and Wafer Formation</td>
<td>162</td>
</tr>
<tr>
<td>7.1.2 Thermal Oxidation</td>
<td>163</td>
</tr>
<tr>
<td>7.1.3 Doping Processes</td>
<td>165</td>
</tr>
<tr>
<td>Ion Implantation</td>
<td>165</td>
</tr>
<tr>
<td>Solid State Diffusion</td>
<td>166</td>
</tr>
<tr>
<td>7.1.4 Photolithography</td>
<td>167</td>
</tr>
<tr>
<td>Resolution</td>
<td>168</td>
</tr>
<tr>
<td>Depth of Focus</td>
<td>168</td>
</tr>
<tr>
<td>Aligning Masks</td>
<td>170</td>
</tr>
<tr>
<td>7.1.5 Thin Film Removal</td>
<td>170</td>
</tr>
<tr>
<td>Thin Film Etching</td>
<td>170</td>
</tr>
<tr>
<td>Wet Etching</td>
<td>171</td>
</tr>
<tr>
<td>Dry Etching</td>
<td>171</td>
</tr>
<tr>
<td>Chemical Mechanical Polishing</td>
<td>173</td>
</tr>
<tr>
<td>7.1.6 Thin Film Deposition</td>
<td>173</td>
</tr>
<tr>
<td>Physical Vapor Deposition (PVD)</td>
<td>175</td>
</tr>
<tr>
<td>Chemical Vapor Deposition (CVD)</td>
<td>176</td>
</tr>
<tr>
<td>7.2 CMOS Process Integration</td>
<td>177</td>
</tr>
<tr>
<td>FEOL</td>
<td>177</td>
</tr>
<tr>
<td>BEOL</td>
<td>177</td>
</tr>
<tr>
<td>CMOS Process Description</td>
<td>178</td>
</tr>
<tr>
<td>7.2.1 Frontend-of-the-Line Integration</td>
<td>180</td>
</tr>
<tr>
<td>Shallow Trench Isolation Module</td>
<td>181</td>
</tr>
<tr>
<td>Twin Tub Module</td>
<td>187</td>
</tr>
<tr>
<td>Gate Module</td>
<td>190</td>
</tr>
<tr>
<td>Source/Drain Module</td>
<td>193</td>
</tr>
<tr>
<td>7.2.2 Backend-of-the-Line Integration</td>
<td>199</td>
</tr>
<tr>
<td>Self-Aligned Silicide (Salicide) Module</td>
<td>199</td>
</tr>
<tr>
<td>Pre-Metal Dielectric</td>
<td>200</td>
</tr>
<tr>
<td>Contact Module</td>
<td>202</td>
</tr>
<tr>
<td>Metallization 1</td>
<td>203</td>
</tr>
<tr>
<td>Intra-Metal Dielectric 1 Deposition</td>
<td>205</td>
</tr>
</tbody>
</table>
Chapter 8 Electrical Noise: An Overview 213

8.1 Signals ................................................. 213
  8.1.1 Power and Energy 213
      Comments 215
  8.1.2 Power Spectral Density 215
      Spectrum Analyzers 216

8.2 Circuit Noise ........................................ 219
  8.2.1 Calculating and Modeling Circuit Noise 219
      Input-Referred Noise I 220
      Noise Equivalent Bandwidth 220
      Input-Referred Noise in Cascaded Amplifiers 223
      Calculating $V_{\text{noise},\text{RMS}}$ from a Spectrum: A Summary 224
  8.2.2 Thermal Noise 225
  8.2.3 Signal-to-Noise Ratio 230
      Input-Referred Noise II 231
      Noise Figure 233
      An Important Limitation of the Noise Figure 233
      Optimum Source Resistance 236
      Simulating Noiseless Resistors 236
      Noise Temperature 239
      Averaging White Noise 240
  8.2.4 Shot Noise 242
  8.2.5 Flicker Noise 244
  8.2.6 Other Noise Sources 252
      Random Telegraph Signal Noise 252
      Excess Noise (Flicker Noise) 253
      Avalanche Noise 253
Chapter 9 Models for Analog Design 269

9.1 Long-Channel MOSFETs ........................................... 269
  9.1.1 The Square-Law Equations 271
    PMOS Square-Law Equations 272
    Qualitative Discussion 272
    Threshold Voltage and Body Effect 276
    Qualitative Discussion 276
    The Triode Region 278
    The Cutoff and Subthreshold Regions 278
  9.1.2 Small Signal Models 279
    Transconductance 280
    AC Analysis 285
    Transient Analysis 286
    Body Effect Transconductance, \( g_{mb} \) 287
    Output Resistance 288
    MOSFET Transition Frequency, \( f_T \) 290
    General Device Sizes for Analog Design 291
    Subthreshold \( g_m \) and \( V_{THN} \) 292
  9.1.3 Temperature Effects 293
    Threshold Variation and Temperature 293
    Mobility Variation with Temperature 295
    Drain Current Change with Temperature 295
9.2 Short-Channel MOSFETs ............................................. 297
  9.2.1 General Design (A Starting Point) 297
    Output Resistance 298
    Forward Transconductance 298
    Transition Frequency 299
  9.2.2 Specific Design (A Discussion) 300
9.3 MOSFET Noise Modeling ............................................ 302
  Drain Current Noise Model 302
Chapter 10 Models for Digital Design 311

Miller Capacitance 311

10.1 The Digital MOSFET Model .................................. 312

Effective Switching Resistance 312

Short-Channel MOSFET Effective Switching Resistance 314

10.1.1 Capacitive Effects 315

10.1.2 Process Characteristic Time Constant 316

10.1.3 Delay and Transition Times 317

10.1.4 General Digital Design 320

10.2 The MOSFET Pass Gate .................................... 321

10.2.1 Delay through a Pass Gate 323

10.2.2 Delay through Series-Connected PGs 325

10.3 A Final Comment Concerning Measurements .............. 326

Chapter 11 The Inverter 331

11.1 DC Characteristics ....................................... 331

Noise Margins 333

Inverter Switching Point 334

Ideal Inverter VTC and Noise Margins 334

11.2 Switching Characteristics .................................. 337

The Ring Oscillator 339

Dynamic Power Dissipation 339

11.3 Layout of the Inverter ...................................... 341

Latch-Up 341

11.4 Sizing for Large Capacitive Loads ........................... 344

Buffer Topology 344

Distributed Drivers 347

Driving Long Lines 348

11.5 Other Inverter Configurations .............................. 349

NMOS-Only Output Drivers 350

Inverters with Tri-State Outputs 351

Additional Examples 351

Chapter 12 Static Logic Gates 353

12.1 DC Characteristics of the NAND and NOR Gates .......... 353

12.1.1 DC Characteristics of the NAND Gate 353
Chapter 17 Sensing Using $\Delta\Sigma$ Modulation

17.1 Qualitative Discussion ........................................ 484
  17.1.1 Examples of DSM ........................................ 484
    The Counter ............................................. 485
    Cup Size .............................................. 486
    Another Example ........................................ 486
  17.1.2 Using DSM for Sensing in Flash Memory ................. 487
    The Basic Idea .......................................... 487
    The Feedback Signal .................................... 492
    Incomplete Settling ..................................... 496
17.2 Sensing Resistive Memory ...................................... 497
  The Bit Line Voltage ....................................... 497
  Adding an Offset to the Comparator .......................... 498
  Schematic and Design Values ................................ 499
  A Couple of Comments ....................................... 502
17.3 Sensing in CMOS Imagers .................................... 504
  Resetting the Pixel ....................................... 504
  The Intensity Level ....................................... 504
  Sampling the Reference and Intensity Signals ............... 505
  Noise Issues ............................................. 506
  Subtracting $V_R$ from $V_s$ ................................ 508
  Sensing Circuit Mismatches ................................ 517

Chapter 18 Special Purpose CMOS Circuits

18.1 The Schmitt Trigger ........................................ 523
  18.1.1 Design of the Schmitt Trigger ......................... 524
    Switching Characteristics ................................ 526
  18.1.2 Applications of the Schmitt Trigger .................... 527
18.2 Multivibrator Circuits ........................................ 529
  18.2.1 The Monostable Multivibrator .......................... 529
  18.2.2 The Astable Multivibrator .............................. 530
18.3 Input Buffers .................................................. 531
  18.3.1 Basic Circuits .............................................. 531
    Skew in Logic Gates ............................................. 533
  18.3.2 Differential Circuits ...................................... 534
    Transient Response ............................................. 535
  18.3.3 DC Reference .............................................. 538
  18.3.4 Reducing Buffer Input Resistance ....................... 541
18.4 Charge Pumps (Voltage Generators) ........................ 542
  Negative Voltages ............................................... 543
  Using MOSFETs for the Capacitors ............................ 544
  18.4.1 Increasing the Output Voltage ......................... 544
  18.4.2 Generating Higher Voltages: The Dickson Charge Pump
    Clock Driver with a Pumped Output Voltage ................ 546
    NMOS Clock Driver ............................................. 546
  18.4.3 Example ................................................... 547

Chapter 19 Digital Phase-Locked Loops 551
  19.1 The Phase Detector .......................................... 553
    19.1.1 The XOR Phase Detector .................................. 553
    19.1.2 The Phase Frequency Detector ......................... 557
  19.2 The Voltage-Controlled Oscillator ......................... 561
    19.2.1 The Current-Starved VCO .............................. 561
      Linearizing the VCO's Gain ................................ 564
    19.2.2 Source-Coupled VCOs .................................. 565
  19.3 The Loop Filter .............................................. 567
    19.3.1 XOR DPLL .................................................. 568
      Active-PI Loop Filter ....................................... 573
    19.3.2 PFD DPLL .................................................. 575
      Tri-State Output ............................................. 575
      Implementing the PFD in CMOS ............................ 576
      PFD with a Charge Pump Output ............................ 578
      Practical Implementation of the Charge Pump ............ 579
      Discussion ................................................... 581
  19.4 System Concerns ............................................. 582
19.4.1 Clock Recovery from NRZ Data 584
The Hogge Phase Detector 588
Jitter 591

19.5 Delay-Locked Loops .................................. 592
Delay Elements 595
Practical VCO and VCDL Design 596

19.6 Some Examples .................................... 596
19.6.1 A 2 GHz DLL 596
19.6.2 A 1 Gbit/s Clock-Recovery Circuit 602

Chapter 20 Current Mirrors 613
20.1 The Basic Current Mirror .......................... 613
20.1.1 Long-Channel Design 614
20.1.2 Matching Currents in the Mirror 616
  Threshold Voltage Mismatch 616
  Transconductance Parameter Mismatch 616
  Drain-to-Source Voltage and Lambda 617
  Layout Techniques to Improve Matching 617
  Layout of the Mirror with Different Widths 620
20.1.3 Biasing the Current Mirror 621
  Using a MOSFET-Only Reference Circuit 622
  Supply Independent Biasing 624
20.1.4 Short-Channel Design 627
  An Important Note 630
20.1.5 Temperature Behavior 631
  Resistor-MOSFET Reference Circuit 631
  MOSFET-Only Reference Circuit 633
  Temperature Behavior of the Beta-Multiplier 634
  Voltage Reference Using the Beta-Multiplier 634
20.1.6 Biasing in the Subthreshold Region 635
20.2 Cascoding the Current Mirror ..................... 636
20.2.1 The Simple Cascode 636
  DC Operation 637
  Cascode Output Resistance 637
20.2.2 Low-Voltage (Wide-Swing) Cascode 639
  An Important Practical Note 641
  Layout Concerns 642
20.2.3 Wide-Swing, Short-Channel Design 642
20.2.4 Regulated Drain Current Mirror 645

20.3 Biasing Circuits ................................................. 647
  20.3.1 Long-Channel Biasing Circuits 647
    Basic Cascode Biasing 648
    The Folded-Cascode Structure 648
  20.3.2 Short-Channel Biasing Circuits 650
    Floating Current Sources 651
  20.3.3 A Final Comment 651

Chapter 21 Amplifiers 657

21.1 Gate-Drain Connected Loads ................................. 657
  21.1.1 Common-Source (CS) Amplifiers 657
    Miller's Theorem 660
    Frequency Response 661
    The Right-Hand Plane Zero 662
    A Common-Source Current Amplifier 666
    Common-Source Amplifier with Source Degeneration 667
    Noise Performance of the CS Amplifier with Gate-Drain Load 669
  21.1.2 The Source Follower (Common-Drain Amplifier) 670
  21.1.3 Common Gate Amplifier 671

21.2 Current Source Loads .......................................... 671
  21.2.1 Common-Source Amplifier 671
    Class A Operation 672
    Small-Signal Gain 673
    Open Circuit Gain 673
    High-Impedance and Low-Impedance Nodes 673
    Frequency Response 674
    Pole Splitting 676
    Pole Splitting Summary 679
    Canceling the RHP Zero 685
    Noise Performance of the CS Amplifier with Current Source Load 686
  21.2.2 The Cascode Amplifier 686
    Frequency Response 687
    Class A Operation 688
    Noise Performance of the Cascode Amplifier 688
    Operation as a Transimpedance Amplifier 688
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>21.2.3 The Common-Gate Amplifier</td>
<td>689</td>
</tr>
<tr>
<td>21.2.4 The Source Follower (Common-Drain Amplifier)</td>
<td>690</td>
</tr>
<tr>
<td>Body Effect and Gain</td>
<td>691</td>
</tr>
<tr>
<td>Level Shifting</td>
<td>692</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>693</td>
</tr>
<tr>
<td>Noise Performance of the SF Amplifier</td>
<td>694</td>
</tr>
<tr>
<td>Frequency Behavior</td>
<td>694</td>
</tr>
<tr>
<td>SF as an Output Buffer</td>
<td>696</td>
</tr>
<tr>
<td>A Class AB Output Buffer Using SFs</td>
<td>697</td>
</tr>
<tr>
<td>21.3 The Push-Pull Amplifier</td>
<td>698</td>
</tr>
<tr>
<td>21.3.1 DC Operation and Biasing</td>
<td>699</td>
</tr>
<tr>
<td>Power Conversion Efficiency</td>
<td>699</td>
</tr>
<tr>
<td>21.3.2 Small-Signal Analysis</td>
<td>702</td>
</tr>
<tr>
<td>21.3.3 Distortion</td>
<td>704</td>
</tr>
<tr>
<td>Modeling Distortion with SPICE</td>
<td>705</td>
</tr>
<tr>
<td><strong>Chapter 22 Differential Amplifiers</strong></td>
<td>711</td>
</tr>
<tr>
<td>22.1 The Source-Coupled Pair</td>
<td>711</td>
</tr>
<tr>
<td>22.1.1 DC Operation</td>
<td>711</td>
</tr>
<tr>
<td>Maximum and Minimum Differential Input Voltage</td>
<td>712</td>
</tr>
<tr>
<td>Maximum and Minimum Common-Mode Input Voltage</td>
<td>713</td>
</tr>
<tr>
<td>Current Mirror Load</td>
<td>715</td>
</tr>
<tr>
<td>Biasing from the Current Mirror Load</td>
<td>717</td>
</tr>
<tr>
<td>Minimum Power Supply Voltage</td>
<td>717</td>
</tr>
<tr>
<td>22.1.2 AC Operation</td>
<td>718</td>
</tr>
<tr>
<td>AC Gain with a Current Mirror Load</td>
<td>719</td>
</tr>
<tr>
<td>22.1.3 Common-Mode Rejection Ratio</td>
<td>721</td>
</tr>
<tr>
<td>Input-Referred Offset from Finite CMRR</td>
<td>723</td>
</tr>
<tr>
<td>22.1.4 Matching Considerations</td>
<td>724</td>
</tr>
<tr>
<td>Input-Referred Offset with a Current Mirror Load</td>
<td>725</td>
</tr>
<tr>
<td>22.1.5 Noise Performance</td>
<td>726</td>
</tr>
<tr>
<td>22.1.6 Slew-Rate Limitations</td>
<td>727</td>
</tr>
<tr>
<td>22.2 The Source Cross-Coupled Pair</td>
<td>727</td>
</tr>
<tr>
<td>Operation of the Diff-Amp</td>
<td>728</td>
</tr>
<tr>
<td>Input Signal Range</td>
<td>729</td>
</tr>
<tr>
<td>22.2.1 Current Source Load</td>
<td>731</td>
</tr>
<tr>
<td>Input Signal Range</td>
<td>732</td>
</tr>
</tbody>
</table>
Common-Mode Rejection Ratio (CMRR) 789
Power Supply Rejection Ratio (PSRR) 790
Increasing the Input Common-Mode Voltage Range 791
Estimating Bandwidth in Op-Amp Circuits 792

24.2 An Op-Amp with Output Buffer 793
Compensating the Op-Amp 794

24.3 The Operational Transconductance Amplifier (OTA) 796
Unity-Gain Frequency, $f_{\text{un}}$ 797
Increasing the OTA Output Resistance 798
An Important Note 799
OTA with an Output Buffer (An Op-Amp) 800
The Folded-Cascode OTA and Op-Amp 803

24.4 Gain-Enhancement 808
Bandwidth of the Added GE Amplifiers 809
Compensating the Added GE Amplifiers 811

24.5 Some Examples and Discussions 812
A Voltage Regulator 812
Bad Output Stage Design 817
Three-Stage Op-Amp Design 820

Chapter 25 Dynamic Analog Circuits 829

25.1 The MOSFET Switch 829
Charge Injection 830
Capacitive Feedthrough 831
Reduction of Charge Injection and Clock Feedthrough 832
$kT/C$ Noise 833
25.1.1 Sample-and-Hold Circuits 834
25.2 Fully-Differential Circuits 836
Gain 836
Common-Mode Feedback 837
Coupled Noise Rejection 838
Other Benefits of Fully-Differential Op-Amps 838
25.2.1 A Fully-Differential Sample-and-Hold 838
Connecting the Inputs to the Bottom (Poly1) Plate 840
Bottom Plate Sampling 841
SPICE Simulation 841
25.3 Switched-Capacitor Circuits 843
25.3.1 Switched-Capacitor Integrator 845
Contents

Lowering Input Capacitance 887
Making the Op-Amp More Practical 888
Increasing the Op-Amp's Open-Loop Gain 889
Offsets 892
Op-Amp Offset Effects on Outputs 893
Single-Ended to Differential Conversion 894
CMFB Settling Time 895
CMFB in the Output Buffer (Fig. 26.43) or the Diff-Amp (Fig. 26.40)? 895

26.4 Op-Amp Design Using Switched-Capacitor CMFB ............... 896
Clock Signals 896
Switched-Capacitor CMFB 896
The Op-Amp's First Stage 898
The Output Buffer 900
An Application of the Op-Amp 901
Simulation Results 902
A Final Note Concerning Biasing 904

Chapter 27 Nonlinear Analog Circuits 909

27.1 Basic CMOS Comparator Design ......................... 909
Preamplification 910
Decision Circuit 910
Output Buffer 913

27.1.1 Characterizing the Comparator 915
Comparator DC Performance 915
Transient Response 916
Propagation Delay 918
Minimum Input Slew Rate 918

27.1.2 Clocked Comparators 918

27.1.3 Input Buffers Revisited 920

27.2 Adaptive Biasing ................................................. 920

27.3 Analog Multipliers ............................................. 923

27.3.1 The Multiplying Quad 924
Simulating the Operation of the Multiplier 926

27.3.2 Multiplier Design Using Squaring Circuits 928

Chapter 28 Data Converter Fundamentals by Harry Li 931

28.1 Analog Versus Discrete Time Signals ...................... 931

28.2 Converting Analog Signals to Digital Signals .......... 932
28.3 Sample-and-Hold (S/H) Characteristics .................. 935
  Sample Mode 936
  Hold Mode 937
  Aperture Error 937
28.4 Digital-to-Analog Converter (DAC) Specifications .......... 938
  Differential Nonlinearity 941
  Integral Nonlinearity 943
  Offset 945
  Gain Error 945
  Latency 945
  Signal-to-Noise Ratio (SNR) 945
  Dynamic Range 947
28.5 Analog-to-Digital Converter (ADC) Specifications .......... 947
  Quantization Error 948
  Differential Nonlinearity 950
  Missing Codes 951
  Integral Nonlinearity 951
  Offset and Gain Error 953
  Aliasing 953
  Signal-to-Noise Ratio 956
  Aperture Error 956
28.6 Mixed-Signal Layout Issues .............................. 957
  Floorplanning 958
  Power Supply and Ground Issues 958
  Fully Differential Design 960
  Guard Rings 960
  Shielding 961
  Other Interconnect Considerations 962

Chapter 29 Data Converter Architectures by Harry Li 965
29.1 DAC Architectures ........................................ 965
  29.1.1 Digital Input Code 965
  29.1.2 Resistor String 966
    Mismatch Errors Related to the Resistor-String DAC 967
    Integral Nonlinearity of the Resistor-String DAC 969
    Differential Nonlinearity of the Worst-Case Resistor-String DAC 970
  29.1.3 R-2R Ladder Networks 971