Chemical Mechanical Planarization of Microelectronic Materials

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Library of Congress Card No.:
Applied for

British Library Cataloging-in-Publication Data:
A catalogue record for this book is available from the British Library

Bibliographic information published by
Die Deutsche Bibliothek
Die Deutsche Bibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data is available in the Internet at <http://dnb.ddb.de>.

Printed in the Federal Republic of Germany
Printed on acid-free paper

Printing Strauss GmbH, Mörlenbach
Bookbinding Litges & Dopf Buchbinderei GmbH, Heppenheim

ISBN-13: 978-0-471-13827-3
ISBN-10: 0-471-13827-4

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PREFACE

In spite of being a historically ancient technology, chemical mechanical planarization (CMP) has never attracted so much attention as it has in the last few years. This is because of its applicability in planarizing the dielectrics and metal films used in the silicon integrated circuit (Si IC) fabrication. Continued miniaturization of the device dimensions and the related need to interconnect an increasing number of devices on a chip have led to building multilevel interconnections on planarized levels. The difference between the historical uses of CMP and those in the Si IC fabrication lies in the amount of material that can be removed prior to achieving the desired planarity. Very thin (usually less than 0.5 μm) materials have to be removed precisely, ending up on a different material and on a sea of embedded metal and dielectric surfaces. Maintaining the precise control on the remaining thickness, which is also very small ($\leq$ 0.5 μm), to within 0.01–0.05 μm while maintaining the integrity of underlying structures are added requirements. This severity of such criteria for CMP has challenged both scientists and engineers. Understanding the CMP process with a large number of variables and the science of pads, abrasives, slurry chemistry, post-CMP cleaning, feature size dependency, etc. have become essential in developing a reliable high-performance and

cost-effective CMP process. These requirements have led to an unprecedented research and development activity, both in the industrial and university sectors, as well as in tool and consumable manufacturers. A close association between these different groups and among various branches of science and engineering has developed, driven by the economic leverage that is provided by low-cost, multilevel interconnect structures for advanced ICs.

At Rensselaer Polytechnic Institute's Center for Integrated Electronics and Electronics Manufacturing, we have been involved in CMP-related research from the time when IBM demonstrated the advantages to the rest of the world. Several years of research in this area has evolved into this book, which describes the science and technology of CMP, along with IC applications, and with a review of the available data. The scientific challenges of CMP as well as the engineering challenges for implementation in IC manufacturing environments are appreciable. This book is intended to be a resource for both groups. We have also provided problem sets in the Appendix at the end of the book for the students in this area. Problems have been defined to encourage scientific understanding leading to engineering applications.

Chapters 1 and 2 introduce the CMP process and historical motivations. The present status of CMP is discussed in Chapter 2, which focuses on establishing the need of advanced metallization schemes and planarization. There are a large number of variables that control the process; these are discussed in Chapter 3. Chapter 4 presents the science of CMP—mechanical and chemical concepts important in understanding the CMP fundamentals. The CMP of the SiO_2 films, the most commonly used insulator interlayer dielectric, is discussed in Chapter 5. Chapters 6 and 7 cover the CMP of the two most studied metals, W and Cu, respectively. Chapter 8 examines the applicability of CMP to new materials, e.g., Al, polymers, and Si_3N_4 photoresists. Finally, Chapter 9 covers post-CMP cleaning science and technology.

The authors thank a large number of groups and people who have directly or indirectly contributed to making this book possible. IBM, Intel, SEMATECH, and SRC have funded and monitored the CMP programs at Rensselaer leading to the present state of knowledge. A large number of people involved in research at these institutions and National Semiconductor, Texas Instruments, AMD, Motorola, LSI Logic, and IPEC/Planar

have also contributed during the research at Rensselaer and in preparation of the manuscript. Professors M. Tomozawa and D. Duquette have provided insights and reviews very valuable in the preparation of the book. Discussions with L. Cook, M. Fury, K. Holland, R. Jairath, and several graduate students working in CMP-related research at Rensselaer have been very fruitful.

Many thanks are due and sincerely given to Mrs. Lori Wilson for putting the manuscript together. Without her several hours of hard work, the production of this book would not have been possible. We also wish to note our appreciation to Mr. Jan Neirynck for helping us diligently in finding referenced materials.

We are grateful to many authors whose papers we have followed closely in various parts of the book and who allowed us to use their work in this book. We are also thankful to Academic Press, Adam Hilger, American Institute of Physics, American Ceramic Society, Butterworth-Heinemann, The Electrochemical Society, Institute of Electrical and Electronics Engineers, Japan International Conference on Solid State Devices and Materials, John Wiley & Sons, Journal of Cellular Plastics, Journal of Crystalline Growth, Macmillan Publishing Company, Materials Research Society, and the University of South Florida (T.E. Wade), which publishes Proceedings of the VLSI Multilevel Inteconnection Conference, for the use of copyrighted materials.

Most of all, we would like to thank our families for the understanding and love that made writing of this book possible.

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CHAPTER 1

CHEMICAL MECHANICAL PLANARIZATION — AN INTRODUCTION

Planarization is the process of smoothing and planing surfaces. Chemical mechanical planarization (CMP) is the process of smoothing and planing aided by the chemical and mechanical forces. CMP also refers to chemical mechanical polishing that causes planarization of surfaces. Note, however, that polishing and planarization are not synonyms. Polishing generally refers to smoothing of the surface not necessarily planar. Here we shall use CMP for chemical mechanical planarization.

1.1 INTRODUCTION

Historically CMP has been used to polish a variety of materials for thousands of years, for example to produce optically

flatand mirror finished surfaces. Nature has run its own CMP processes to produce beautifully finished stones, finishing affected by years of exposure to generally not-so-aggressive chemical and mechanical forces. Beautifully finished inlaid metal objects have been prepared by the so-called "damascene" process. More recently optically flat and damage-free glass and semiconductor surfaces have been prepared by the use of the CMP processes. Now CMP is being introduced in planarizing the interlayer dielectric (ILD) and metal used to form interconnections between devices and between devices and the world. It is projected that the observed effectiveness of the CMP process will lead to the widespread use of this process at various stages of integrated circuit (IC) fabrication, for a variety of high performance and application-specific ICs, and for a variety of materials.

What is so unique about CMP? CMP achieves planarization of the nonplanarized surfaces. Nonplanarized surface topography is a result of the fabrication process that ends up with a deposition of the film on a previously patterned surface, with a pattern generated by an etching. The generation of surface topography by several deposition, pattern etch, and planarization processes have been examined by Pai et al.[1] Table 1.1, adapted to include other processes not originally considered, compare various processes with G, N, S, and P defining generation or amplification of steps, with no effect or neutral, local planarization or smoothing, and global or true planarization (caused by the process under consideration), respectively. Loss of planarity also arises during lithography not explicitly discussed in Table 1.1. Several other factors, namely autofocus errors, residual lens aberrations, resist thickness variations, and wafer curvature associated with wafer preparations and with film stresses, influence planarity. One can judiciously identify the process sequence to enhance a topography or to obtain localized or globally planarized structure. Only CMP is universally applicable to cause global planarization.

Table 1.2 lists several advantages of CMP.[2] These are discussed again in Chapter 2. The most important advantage is that CMP achieves global planarization which is essential in building

Table 1.1 The Effects of Certain Processes on Wafer Surface Topography[1]

Process Step	Planar Surface	Arbitrary Geometries	Fine Raised Geometries	Fine Sunken Geometries
Evaporation	N	G	G	G
Sputtering	N	G	G	G
Biassputtering	N	S	P	S
Nonconformal CVD	N	G	G	G
Conformal CVD	N	S	S	P
Selective Deposition	N	P[a]	P[a]	P[a]
Spin Coating	N	S	S	P[b]
Wet Etching	G	G	G	G
Dry Etching	G	G	G	G
Liftoff	G	P[c]	P[c]	P[c]
Reflow	N	S	S	p[d]
Etch-back Planarization	N	S	S	P
Chemmech Polishing	P	P	P	P

[a]Requires suitable surface for selectivity. [b]Assumes negligible shrinkage. [c]Requires lift-off medium self-aligned to geometries. [d]Severe restriction on total areas and pattern geometries.

G = Generation or amplification of steps
N = No effect
S = Local planarization or smoothing
P = Global planarization

multilevel interconnections (see Chapter 2). Table 1.3, adapted from the Semiconductor Industry Association's (SIA) National Technology Roadmap for Semiconductors (NTRS), [3] shows the increasing number of interconnection levels in high performance circuits and memories. Note the chronologically increasing planarity requirements.[4]

Table 1.2 Advantages of CMP[2]

• Achieves global planarization.
• Universal or materials insensitive — all types of surfaces can be planarized.
• Useful even for multi-material surfaces.
• Reduces severe topography allowing for fabrication with tighter design rules and additional interconnection levels.
• Provides an alternate means of patterning metal (e.g., damascene) eliminating the need of the reactive ion etching or plasma etching for difficult-to-etch metals and alloys.
• Leads to improved metal step coverage (or equivalent).
• Helps in increasing reliability, speed and yield (lower defect density) of sub-0.5 μm devices/circuits.
• Expected to be a low cost process.
• Does not use hazardous gases in dry etching process.

1.2 APPLICATIONS

It is noted that the successful applications of the CMP process in silicon integrated circuits (IC) were started with building multilevel (greater than 2) interconnection structures employing deposited SiO_2 as the ILD and the chemical vapor deposited (CVD) tungsten as the via fill metal with sputtered aluminum as the planar interconnection metal.[5] In this application CMP achieved two results: (i) planarization of the SiO_2 surface and (ii) removal of CVD tungsten from horizontal surfaces, thus allowing the excellent via fill metal to be then connected to horizontal aluminum interconnections formed by sputter deposition and the subsequent reactive ion etching. Thus initial process developments focused on the CMP of SiO_2 and tungsten layers.[6,7] Since these developments, the use of CMP has expanded to (i) a large variety of materials including metals (Al, Cu, Ta, Ti, TiN, W, and their alloys), insulators (SiO_2 and doped SiO_2 glasses, Si_3N_4, and polymers), and polysilicon, (ii) a variety of applications involving even larger area planarization such as those used in multichip modules

Table 1.3 National Technology Roadmap for Semiconductors[3]

Technology Characteristics	Year[a] 1995	1998	2001	2004	2007	2010
MFS[b] (μm)	0.35	0.25	0.18	0.13	0.10	0.07
Chip Size (mm^2)						
DRAM	190	280	420	640	960	1400
Microprocessor	250	300	360	430	520	620
ASIC	450	660	750	900	1100	1400
Maximum Substrate Diameter (mm)	200	200	300	300	400	400
Number of Metal Levels						
DRAM	2	2-3	3	3	3	3
Microprocessor	4-5	5	5-6	6	6-7	7-8
Maximum Interconnection Length						
Logic (meter/chip)	380	840	2100	4100	6300	10,000
Planarity Requirements (nm) within Litho Field for Minimum Interconnection CD	300	300	250	150	150	150
Minimum Interconnection CD (μm) (metal 1)	0.40	0.30	0.22	0.15	0.11	0.08
Interconnection Metal	Al	Al, Cu	Al, Cu	Cu, Al	Cu, Al	Cu, Al
ILD Dielectric Constant	3.9 (3-3.9)	<3	≤2.5	≤2	1-2	1-2
Particle Size (μm)	≥0.12	≥0.08	≥0.06	≥0.04	≥0.04	≥0.03
Integrated Particle Density per Module (particles/$meter^2$)	125	125	125	125	125	125

[a]Year of first DRAM shipment.
[b]MFS = minimum feature size.

Table 1.4 Materials to be Polished and Possible Applications

	Materials	Application[a]
Metal	Al	Interconnection
	Cu	Interconnection
	Ta	DB/AP[b]
	Ti	DB/AP
	TiN, TiN_xC_y	DB/AP
	W	Interconnection
		e-Emitter
	Cu-Alloys	Interconnection
	Al-Alloys	Interconnection
	Polysilicon	Gate/Interconnection
Dielectric	SiO_2	ILD
	BPSG	ILD
	PSG	ILD
	Polymers	ILD
	Si_3N_4 or SiO_xN_y	Passivation/Hard CMP
		Stop Layer
	Aerogels	ILD
Other	ITO	Flat Panel
	High K Dielectrics	Packaging/Capacitor
	High T_c Superconductor	Interconnection/Packaging
	Optoelectronic Materials	Optoelectronics
	Plastics, Ceramic	Packaging
	Silicon-on-Insulator (SOI)	Advanced Devices/Circuits

[a]Among other process applications are the use of CMP to improve shallow trench isolation, Bird's beak planarization, and stacked or trench capacitor.
[b]DB/AP = Diffusion Barrier/Adhesion Promoter

and in other IC packaging and in flat panel displays, and (iii) planarizing materials at different levels of silicon device and integrated front-end circuit processing, even as early as at the polysilicon level. Table 1.4 lists the materials and possible appli-cations.

References to these research and development efforts are given throughout this book.

1.3 THE CMP PROCESS

The CMP process simply consists of moving the sample surfaces to be polished against a pad that is used to provide support against the sample surface (the pad thus experiences the pressure exerted on the sample), and to carry slurry between the sample surface and pad to affect the polishing leading to planarization. Abrasive particles in the slurry cause mechanical damage on the sample surface, loosening the material for enhanced chemical attack or fracturing off the pieces of surface into a slurry where they dissolve or are swept away. The process is tailored to provide enhanced material removal rate from high points on surfaces (compared to low areas), thus affecting the planarization. Note chemistry alone will not achieve planarization because most chemical actions are isotropic. Mechanical grinding alone, theoretically, may achieve the desired planarization but is not desirable because of extensive associated damage of the material surfaces. Details of the process are discussed in subsequent chapters. Here it is pointed out that there are three main players in this process:

1. The surface to be polished;
2. The pad — the key media enabling the transfer of mechanical forces to the surface being polished; and
3. The slurry — that provides both chemical and mechanical effects.

Each of the above are extremely important and briefly discussed here. Most of the variables discussed in Chapter 3 could be categorized in one of the above groups. Temperature, pressure, relative velocity of the surface being polished with respect to pad (which is usually rotating), and pre- and post-CMP cleaning that may affect the final acceptance criteria for the polished surface are other parameters that play important roles.

The key knowledge of the chemical, structural, and mechanical properties of the surface to be polished establishes the polishing parameter space including the chemistry and mechanical force. CMP of a single material is thus easier compared to that of a surface consisting of different materials spaced at different surface coverages. In a damascene polishing,[3] the metal wires and posts buried in the ILD are polished and a strong feature size dependence has been seen.[8] A complex set of phenomena occurs that control this feature size dependence, the most important of which is related to the elastic behavior of the pad.

The role of pad and its mechanical properties are discussed in Chapter 4. Ideally one would expect the pad to be rigid and chemically inert so that it can carry abrasives and chemicals (the slurry ingredients) all across the surface being polished. In this case, the surface to be planarized must be kept aligned and parallel with respect to the rigid pad at all times during planarization. For real situations pads are not rigid, leading to several issues: changes occurring in pad properties as polishing continues, cyclic changes, solvent/chemical effects on rigidity, and erosion. Similarly pads are not chemically and physically inert materials, thus leading to the following changes in surface and possibly bulk chemistry of the pad ingredients (changes affected by mechanical forces and changes that affect mechanical properties), surface bonding between abrasive and pad, electrochemical effects, and the necessity to recondition or regenerate the pad to cause reproducible polishing behavior. Thus there is a need for understanding these changes in pads as a function of the use and during actual use.

The slurry is the third important key player among the three listed above. Key slurry parameters that affect CMP are discussed in Chapter 3. Slurries provide both the chemical action through the solution chemistry and the mechanical action through the abrasives. High polishing rates, planarity, selectivity, uniformity, post-CMP ease of cleaning including environmental health and safety issues, shelf-life, and dispersion ability are the factors considered to optimize the slurry performance. For hard materials like W and Ta mechanical effects are more important. On the other hand for soft

materials like aluminum and polymers chemical effects may be more important. Similarly a polycrystalline film may require different chemistry compared to amorphous or single crystalline films due to enhanced chemical action at the grain boundaries or at a given grain orientation.

Abrasives in the slurry play the very important role of transferring mechanical energy to the surface being polished. Commonly used abrasives are SiO_2 and Al_2O_3, although CeO_2 is one of the most popular abrasive used for the polishing of the glass. The abrasive-liquid interactions, through chemical and physical actions which precede the abrasive-substrate surface and liquid-substrate surface interactions, play an important role in determining the optimum abrasive type, size, shape, and concentration.

Finally the last important step of the complete CMP-process sequence is the cleaning. Removal of the slurry from the surface without leaving any macroscopic, microscopic, or electrically active defects is very important in making the process useful. CMP slurries and post chemical cleans should not introduce any chemical or particulate contamination. Thus, cleaning processes must be designed for specific materials surfaces. A final in-situ dry clean (or wet clean) prior to the deposition of the next film, usually the ILD, may be necessary to optimize the interface between polished surfaces and the new deposit. In specific cases the cleaning process could be designed to leave the metallic surfaces protected from corrosion, such as by using benzotriazole (BTA).[9,10] Note the particle size and density requirements in Table 1.3. Most of the standard cleans can easily remove more than 99% to 99.95% of the surface particles. However, the leftovers (0.05% or more) require additional cleaning which must be developed. The smaller the particles the more difficult it is to achieve the required cleaning. Understanding the particle-surface adhesion forces and how to overcome these forces are key to developing a good process. Both chemical and mechanical environments may be necessary to loosen the particle from the surface and sweep it away from the surface. Typical cleaning tool functions can be summarized as:[11]

Buff and brush: mechanical and hydrodynamic

Megasonic:	acoustic streaming (hydrodyn-amic) and cavitation
Chemistry:	etching, electrostatic repulsion
Marangoni:	surface tension, surface tension gradient, induced flow; and
Various jets:	water, ice, dry ice.

Considerable research employing the abovementioned tools is being carried out to study and understand the cleaning of surfaces (and to study methods to keep them clean) that could consist of one or multiple materials with and without topography. CMP researchers must keep in touch with this research to provide the optimized cleaning of a variety of surfaces at the end of the planarization.

1.4 CMP TOOLS

Tools are essential in delivering the right process to the sample surface without affecting the underlying materials, yield, and cost-of-ownership (COO).[12] As mentioned earlier, a large variety of tools have been available for polishing of surfaces where the thickness (or the amount) of material removed was generally not critical. In microelectronic applications tools are needed for planarizing thin films, usually less than μm thick. Several vendors have tools (in the market that are used in both research and manufacturing environments. IPEC/WESTECH tools are the most common. Other tool manufacturers include Strasbaugh, Speedfam, Cybeq, On-Trak, and Applied Materials, although the last two have tools in development at this time. Discussion of these tools, their definition, and their effectiveness is beyond the scope of this book. It is, however, mentioned that there are equipment related effects to the process. Table 1.5, adopted from a presentation by Holland,[13] lists some of these equipment contributions to the final process, tool reliability, yield, and throughput, and thus COO.

Table 1.5 Equipment Contributions to Process[13]

- Oxide Planarization Requirements
  - — Reproducible pad conditioning
  - — pH <13
  - — Heat exchange platens
  - — Carriers compensate for wafer flats, etc.
  - — Precise control of surface speeds and downforce
  - — Automatic loading/unloading
  - — Slurry removal (cleaning)
    - – elimination of brush cleaning in some applications
  - — Error recovery software
  - — Accurate wafer sensing
  - — Planarization detector or oxide removal insitu
- Metal Planarization Additional Requirements
  - — pH >0.6
  - — Microscratch reduction (oxide buff after metal polish)
  - — End point detect with polish stop

1.5 PROCESS INTEGRATION

As discussed in earlier sections, CMP process involves the surfaces to be polished, pads,slurries which are composed of chemicals, abrasives, and fluids, slurry dispensing tools, CMP tools, cleaning tools, and finally metrology tools to measure the thickness and quality of the processed (or unprocessed) surfaces of films. Figure 1.1 shows a diagram of CMP process integration.[2] Final manufacturability of a given CMP process will be determined by the need, performance, and cost per die.

1.6 CONCLUSION AND BOOK OUTLINE

In order to decrease the cost and delay impacts of the interconnect layers, new materials and processing schemes must be chosen to decrease processing complexity, defect density, and inter-

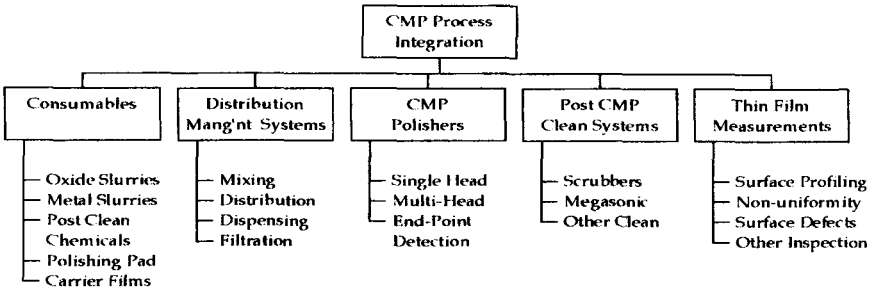

Figure 1.1 Showing the materials and tool sets required for complete CMP- process integration.[2]

connect delay. In addition, these new materials and processing schemes must be extendible to very fine dimensions to meet requirements of future IC manufacturing. To meet the requirements of low-cost, high performance IC manufacturing, current investigations include copper metal[14] and low dielectric polymers[15] materials sets and CMP of metal and ILDs.[16] CMP of several layers (trench isolation, ILD, tungsten plugs) is already occurring in manufacturing at several companies. Future processing technologies are likely to expand the use of CMP to the planarization of a variety of materials.The intent of this book is to investigate the current understanding and utilization of CMP as well as the challenges of integrating CMP into future metallization schemes. Chapter 2 discusses in detail the need for CMP planarization, low-ε_r ILDs, and low resistivity metals. Chapter 3 gives a brief overview of the important variables to consider in a CMP process. Chapter 4 discusses the fundamental chemical, electrochemical, and mechanical principles necessary to discuss CMP mechanisms. Chapters 5, 6, and 7 discuss oxide CMP, tungsten, aluminum, and other metal CMP, and copper CMP, respectively. Chapter 8 discusses the CMP of other materials such as low-ε_r ILDs.

This book attempts to strike a balance between fundamental understanding and practical application of CMP. We believe that a fundamental understanding of CMP is critical to the success of CMP in practice.

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