Nanoscale CMOS
Nanoscale CMOS

Innovative Materials, Modeling and Characterization

Edited by
Francis Balestra

ISTE
WILEY
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Introduction

Microelectronics, based on CMOS (complementary metal oxide semiconductor) technology, is the essential hardware enabler for electronic product and service innovation in key growth markets, such as communications, calculating, consumer electronics, automotive, avionics, automated manufacturing, health and environment. The global semiconductor industry underpins 16% of the world’s total economy and is growing every year. The worldwide market for electronic products is estimated at more than $1,100 billion, and the related electronics services market at more than $6,500 billion. These product and service markets are enabled by a $280 billion market for semiconductor components and an associated $80 billion market for semiconductor equipment and materials. The new era of nanoelectronics, which started at the beginning of the current millennium with the smallest patterns in state-of-the-art silicon-based devices below 100 nanometers, is enabling an exponential increase in system complexity and functionality.

Nanoelectronics enables the development of smart electronic systems by switching, storing, receiving and transmitting information. In respect to its societal relevance, the ubiquitous nanoelectronics is also closely linked to the notion of ambient intelligence, which is a vision of the future where people are surrounded by intelligent intuitive interfaces that are embedded in all kinds of objects and an environment that is capable of recognizing and responding to the presence of different individuals in a seamless way.

Since the invention of the transistor in 1947 at Bell Labs, followed by the first silicon transistor in 1954 and the concept of integrated circuits in 1958 in Texas Instruments, progress in the field of microelectronics has been tremendous, which has revolutionized the society. In these last 50 years, dramatic advances have been achieved in the packing density of transistors, resulting since the 1970s in a density of transistors on an integrated chip (IC) will doubles every two years (Moore’s law). At the beginning of the 1970s, the first microprocessor had only about 2,000
transistors (10 μm gate length), the world’s first two-billion transistor processor was reported in 2008 in 65 nm CMOS technology. The technology node will drop down to 9 nm in 2024. Meanwhile, development goes on apace with the 32 nm node coming on stream in late 2009. Today, the annual fabrication of MOSFET (metal oxide semiconductor field effect transistor) per person is about one billion.

The same trend is observed for memories. The DRAM (dynamic random access memory) capacity has been raised from 1 kb in 1970 to more than 2 Gb at present. Three billion transistor SRAM test chips have also been recently announced. For nonvolatile memories, a recent record of 64 Gb has been demonstrated. This increase in transistor count and memory capacity has led to increased processing power, measured now in thousands of MIPS (millions of instructions per second).

A dramatic increase in the transistor performance, measured as the ON to OFF ratio of drain current in DC mode, while lowering the supply voltage, has been obtained during recent decades. In AC mode, cut-off frequencies of several hundred GHz have been recently measured in bulk and SOI (silicon-on-insulator) CMOS technologies.

Moore’s law also means decreasing cost per function, the transistor price has dropped at an average rate of about 1.5 per year (about $10^8$ since the beginning of the semiconductor industry).

However, according to the International Technology Roadmap for Semiconductors [ITR 09] and ENIAC Strategic Research Agenda [SRA 07], there are big challenges to overcome in order to continue progress in the same direction. Si will remain the main semiconductor material for the foreseeable future, but the required performance improvements for the end of the roadmap for high performance, low and ultra-low power applications as well as memories will lead to a substantial enlargement of the number of new materials, technologies and device architectures.

SOI substrates are interesting candidates for the manufacturing of mainstream semiconductor products such as microprocessors, low-power devices or memories [CRI 09]. The classic CMOS architecture is approaching its scaling limits, “end-of-roadmap” alternative devices are also being investigated. Amongst the different types of SOI-based devices proposed, one clearly stands out for the end of the roadmap: the multigate field-effect transistor (multigate- or double-gate- or gate-all-around- or Fin-FET), enabling better electrostatic control of the channel(s), hence a more aggressive scalability and reduced leakage currents, higher driving currents and speed, reduced variability and enriched functionality. The
International Technology Roadmap for Semiconductors recognizes the importance of these devices.

In the sub-10 nm range, “beyond-CMOS” devices, based on nanowires, nanodots, carbon electronics or other nanodevices, could play an important role and could be integrated on CMOS platforms in order to pursue integration down to nanometer structures.

Therefore, new generations of nanoelectronic ICs present increasingly formidable multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, etc.). This long-term research is fundamental to prepare the path for future nanoelectronic technologies, as a 15 to 20 year time frame is usually necessary between the first validation of a new innovative idea and its full demonstration and acceptance into complex systems.

The three parts of this book have been written by scientists, from universities and research centers, strongly involved in teaching and research programs related to nanoelectronic devices; because of their expertise and international commitment, they are very well informed on the state-of-the-art of the physics and technologies and the evolution of nanoelectronic materials and components.

This book offers a comprehensive review of the state-of-the-art in innovative materials, advanced modeling and novel characterization methods for nanoscale CMOS dedicated to researchers, engineers and students. In the field of new materials, which has been a major drive to find new ways to enhance the performance of semiconductor technologies, this text covers three areas that will provide a dramatic impact on the approaches to future CMOS – global and local strained and alternative materials for high-speed channels on bulk substrate and insulator, very low access resistance and various high dielectric constant gate stacks for power scaling. It also focuses on the most reliable modeling and simulation methods of the electrical properties of ultimate MOSFETs, including ballistic transport, gate leakage, atomistic simulation and compact models for single- and multi-gate devices, nanowire and carbon-based FETs. Finally, the book presents an in-depth investigation of the main nanocharacterization techniques for an accurate determination of transport parameters, interface defects, channel strain as well as RF properties, including capacitance-conductance, improved split C-V, magnetoresistance, charge pumping, low frequency noise and Raman spectroscopy.

Part 1 reviews some of the progress being made in the key areas of new materials for nanoscale transistors that could be incorporated in future technology nodes. Chapter 2 focuses on general issues of high-\(k\) dielectrics and metal gates, and points out a range of different materials that will be able to circumvent fundamental
limitations in various applications. Chapter 3 reviews the current state-of-the-art for strained silicon and then discusses the route to higher strain and Ge channels, based on global strain tuning buffers. Interesting approaches for the realization of thin virtual substrates and strained silicon on oxide (SSOI) wafers and devices are described in Chapter 4. The conversion of the biaxial strain to uniaxial strain in order to develop nanowire FETs is also shown. The objective of Chapter 5 was to introduce recent developments in the field of Schottky barrier engineering and integration in nonconventional MOSFET architectures. Low temperature dopant segregation at the silicide-semiconductor interface is also analyzed as a useful methodology to lower the barrier height. Practical implementation scenarios are described for p- and n-type devices and both static and high frequency performances of Schottky-barrier MOSFETs are also presented.

Part 2 outlines some of the progress being made in the key areas of simulation of nanoscale transistors including the simulation of drain and gate leakage currents, the role of alternative channel materials, the application of a full-quantum transport approach in the simulation of ultimate silicon nanodevices, the progress in the field of compact models for nano-CMOS and the advanced simulation approaches for beyond-CMOS devices. Chapter 7 illustrates how to calculate gate current in nonconventional devices such as double gate SOI MOSFETs and addresses the problem of analyzing tunneling in 2D and 3D devices. An overview about trap-assisted tunneling is given. Finally, a comparison between different approaches for gate current computation applied to a template gate stack featuring high-k dielectric is reported. In Chapter 8, the general semi-classic modeling framework for drain current computation is introduced together with the methodology for the derivation of the moments of the Boltzmann transport equation. A systematic comparison of drain current simulations for long channel as well as nanoscale MOSFETs obtained either with the Monte Carlo method or with the moment-based models is also addressed. In Chapter 9, the results of the theoretical evaluation of the performance of ultra-scaled nMOSFET with alternative channel material are presented. Both results from efficient and accurate semi-analytical models and by using state-of-the-art simulation tools are investigated. The simplicity of analytical models enable a better understanding of the relative importance of the various mechanisms which contribute to the overall device performance. Chapter 10 deals with the investigation of interface roughness and random discrete dopants, and related variability in nanoscale MOSFETs, which requires fully 3D quantum transport simulations. Then, we review and present several recent developments in compact modeling of nanoscale MOSFETs, in particular multigate devices. Electrostatic and transport modeling issues as well as the development of unified charge control models for different types of multigate MOSFETs are considered. Specific compact modeling issues for ultimate MOSFETs, including velocity saturation, channel length modulation, ballistic transport and quantum confinement, are also discussed. In Chapters 11 and 12, two different types of beyond-CMOS devices, based on carbon
nanotubes or graphene and gate-all-around transistors based on silicon or 3C silicon carbide nanowires, are analyzed using 3D device simulator able to solve the full band Schrödinger equation with open boundary conditions in the nonequilibrium Green’s function (NEGF) framework coupled with the 3D Poisson equation.

In Part 3, the main nanocharacterization techniques for nanoscale devices are investigated. Chapter 14 shows the need to develop a reliable extraction method for transport parameters, which is playing a key role in device performance, and to correlate these electrical properties to materials and processing options. The aim of this chapter is to give an overview of how standard extraction methods have been progressively adapted to account for MOS transistors evolution, what their limits are, and which alternative methods may be used for highly scaled structures. In Chapter 15, we consider accurate methods for characterizing the density and energy distribution of interface states and trap density in the semiconductor/oxide system using measurements of capacitance or conductance of MOS structures, as well as charge pumping and low frequency noise. Chapter 16 shows the methods leading to a reliable evaluation of the channel strain for future nanoscale CMOS. In Chapter 17, we point out the importance of an accurate wideband characterization technique, well adapted to advanced MOS devices, in order to understand their static and dynamic behaviors, and thus to monitor and optimize the fabrication process steps for further reducing the impact of parasitic elements.

Francis Balestra

Acknowledgements

We would like to acknowledge David Leadley for coordinating Part 1, Enrico Sangiorgi for coordinating Part 2, and Denis Flandre for coordinating Part 3 of the book. All the Members of the Sinano Institute and the Partners of the Nanosil and Sinano Networks of Excellence are also gratefully acknowledged for their support.

Bibliography


Part 1

Novel Materials for Nanoscale CMOS
Chapter 1

Introduction to Part 1

1.1. Nanoscale CMOS requirements

The microelectronics industry was born in 1947 when scientists at Bell Labs invented the transistor, which revolutionized the world of electronics. Shortly after, it was realized that enhancements could be made with the research of semiconductors, leading to the formation of the semiconductor industry in 1960. In 2009 the industry was worth over $250 billion [SIA 08]. In 2000, silicon accounted for 98% of the industry [PAU 04]. Its dominance over other materials is due both to its abundance and hence low cost and secondly its native oxide, silicon dioxide (SiO₂) has excellent material properties which have been utilized in transistors over the years. The traditional method to enhance the performance of transistors is by simply scaling their dimensions, the most important of these dimensions was the gate length. By this method not only is the density of transistors on a chip increased but the performance of each transistor is also increased. The industry has grown by following Moore’s law, Figure 1.1, as a basis for expansion which predicts that “the density of transistors on an integrated chip (IC) will double every two years”.

However, despite the historical success of scaling, it is now very clear [INT 09] that the continued performance enhancements in complementary metal-oxide-semiconductor (CMOS) circuits that the industry has become accustomed to cannot be achieved by scaling alone. Indeed, a major concern is the cost of new fabrication plants, in excess of $10 billion each. Of even greater importance could be that MOSFET dimensions are rapidly approaching a regime where the key device features consist of just a few hundred atoms. Here quantum effects such as tunneling
become increasingly problematic, resulting in higher leakage currents and power consumption. In addition, other effects such as random dopant fluctuations are likely to become critical in achieving uniform characteristics across a wafer [ASE 03]. Ultimately the limit will be reached where the position of each atom is crucial and then variability will be the dominant issue.

![Figure 1.1. Moore’s law in action shown by plotting the number of transistors per chip against release date for commercial transistors [INT 05]](image-url)

Research into new materials has been a major drive to find new ways to enhance the performance of semiconductor technologies. This is indicated by the drop in the use of silicon within the industry to 93% [SIA 06] in 2006. However, most of the semiconductor industry utilizes silicon processing-based fabrication plants, so only silicon-based substrates are economically viable platforms. As germanium and silicon-germanium alloys can be processed with these fabrication facilities, their use in mainstream technologies is not excluded. Until the 90 nm node geometrical scaling has satisfied the ITRS performance requirements [ITR 09] using the same silicon/silicon dioxide transistors, although at this node the performance of the silicon channel started to be enhanced by straining (see section 1.3 below). For the 65 nm node the gate dielectric was modified to incorporate some nitrogen, and transistors with written gate lengths of 35 nm and 1.2 nm silicon oxynitride gate dielectrics entered high-volume production [TYA 05]. For the first time at the 45 nm node radically new materials such as high-κ dielectrics and metal gates have been incorporated in commercial processors. The 45 nm technology was demonstrated reliably by Intel in 2006 with one billion working SRAM transistors and now forms the mainstream product line, shipping hundreds of millions of CPUs. Meanwhile development goes on apace with the 32 nm node coming on stream in late 2009 incorporating 2 billion second-generation high-κ strained silicon transistors, still on a bulk silicon wafer [PAC 09]. In addition, 3 billion transistor SRAM test chips of
22 nm node material have been announced. It seems that the progress of Moore’s law is unstoppable and, although for each generation the industry must push the boundaries closer and closer to the fundamental limit, there still remains great optimism that continued performance enhancements can be maintained using silicon-based technologies for many years to come.

Part 1 will review some of the progress being made in the key areas of nanoscale transistors, highlighted in Figure 1.2, that could be incorporated in future technology nodes.

![Figure 1.2. Key aspects of nanoscale MOSFET, with numbers referring to the section where they are discussed](image)

### 1.2. The gate stack – high-$\kappa$ dielectrics

The quality of the Si/SiO$_2$ interface is arguably the single most important reason for the dominance of silicon in the microelectronics industry despite there being several known materials with superior electronic properties. However, the current ITRS scaling trend for CMOS devices dictates that the thickness of the gate dielectric should be reduced to below 1 nm by the end of the roadmap [ITR 09]. However, this results in a large increase in the gate leakage current due to quantum mechanical tunneling, increasing exponentially with decreasing oxide thickness $t_{ox}$ [PLU 01], approximately as

$$J_{DT} = \frac{A}{t_{ox}} \exp \left( -2t_{ox} \frac{2m^* \Phi_B}{\hbar^2} \right), \quad [1.1]$$

where $A$ is a constant, $m^*$ is the carrier effective mass and $\Phi_B$ is the barrier height.
Simulated results show that there exists a “crossover point” such that beyond 2008, the gate leakage limit cannot be met using silicon dioxide (or silicon oxynitride) because of direct tunneling. This means that silicon dioxide has to be replaced as gate dielectric by a material with higher permittivity than SiO$_2$, a so-called high-$\kappa$-dielectric in order to achieve the same capacitive coupling between the gate and the channel, but for a thicker physical thickness to suppress tunneling.

For high-$\kappa$-dielectrics, it is convenient to define an equivalent oxide thickness (EOT) as the theoretical physical thickness of SiO$_2$ required to achieve the same capacitance as that provided by the alternative dielectric. Thus, the EOT can be expressed in terms of its dielectric constant $\kappa_{hik}$ and physical thickness $t_{hik}$ [WIL 01]:

$$EOT = \frac{\kappa_{SiO_2} t_{hik}}{\kappa_{hik}} = 3.9 \frac{t_{hik}}{\kappa_{hik}}$$  \[1.2\]

This means, for example, that an alternative dielectric with a dielectric constant of 20 and a physical thickness of 5 nm could replace SiO$_2$ to achieve an EOT of 1 nm, providing a physically thicker barrier to suppress the gate leakage due to direct tunneling.

As the value of $\kappa_{hik}$ is often not well known, EOT must be determined from an electrical capacitance measurement. A second related quantity is the capacitance effective thickness (CET) which is measured on an actual device and depends also on the gate metal work function, substrate doping and the actual gate voltage of the measurement. CET is typically 0.3–0.4 nm larger than EOT.

In selecting an alternative high-$\kappa$-dielectric to replace silicon dioxide, there are several properties other than the dielectric constant itself, which must be given due consideration. Dielectric/semiconductor band offsets, thermodynamic stability, interface quality, film morphology, gate metal compatibility, process compatibility and reliability have all been shown to be important [WAL 05]. The most promising candidates appear to be transition metal oxides, such as hafnium oxide (HfO$_2$) or their silicates (HfSiO) and rare-earth oxides such as La$_2$O$_3$ or Gd$_2$O$_3$. Particular emphasis is placed on ternary rare-earth oxides, e.g. LaAlO$_3$ and LaLuO$_3$. Many other binary and ternary compounds have been considered, indeed most elements from the periodic table seem to get a look in!

For given values of MOS leakage current and insulator thickness, the dielectric constant, $\kappa$; and the offset value between oxide and silicon energy bands, $\Delta E$, are bound roughly by a hyperbolic relation $\kappa \times \Delta E = C_E$, where $C_E \approx \text{70 eV}$ is necessary for the 22 nm bulk LSTP node [ENG 07], while for SOI $C_E = \text{30 – 40 eV}$ [ENG 07]. For binary metal oxides, $C_E$ values in the higher range have only been found for
La$_2$O$_3$ [IWA 02] but this highly hygroscopic material cannot yet be handled in a production environment. To find other solutions we may study ternary compounds. Examples are the following: HfSiO, which gives a lower $\kappa$ and a higher $\Delta E$ than for HfO$_2$, thus preserving the tunneling leakage, while at the same time increasing the thermal stability of the dielectric; LaLuO$_3$, which can be prepared with low hygroscopicity, high thermal stability and with $C_E \approx 65$ eV for electrons as well as for holes [LOP 06], looks to be capable of satisfying the ITRS 22 nm node LSTP target with a gate leakage of 0.3 A/cm$^2$ for an EOT of 0.9 nm (CET 1.2 nm); another material of particular interest is GdSiO, where the silicidation of Gd$_2$O$_3$ slightly decreases the $\kappa$-value, increases $\Delta E$, and improves stability. The unexplored potential of ternary rare-earth compounds is presently of large interest within the high-$k$ research community. A detailed consideration of high-$k$ dielectrics for nanoscale CMOS devices will be given in Chapter 2, alongside the intimately connected gate metal materials.

In the industrial development of the 45 nm node, Intel have stated that a “hafnium-based” gate dielectric is used [INT 07], but do not specify if that means HfO$_2$, HfSiO or some other ternary compound based on hafnium. They have now shipped millions of 45 nm chips running with high-$k$ dielectrics. Future generations may also employ a similar “hafnium-based material”. For the 22 nm node both bulk and SOI CMOS approaches are being developed and whilst the dielectric properties of HfO$_2$ seem good enough for SOI, they are probably not for bulk which means further dielectric development will be required.

1.3. Strained channels

Applying strain to the silicon channel has been demonstrated to provide significant performance advantages [TAK 96] without having to change the basic channel material and has been incorporated as a technology booster since the 90 nm node. There follows a brief discussion of how strain boosts performance.

1.3.1. Carrier mobility

The carrier mobility $\mu$ characterizes the ease with which a charged carrier (electron or hole) can travel through a material and is defined as the carrier velocity acquired per unit applied electric field. In a relaxation time approximation $\mu = e\tau/m^*$, with mean free time between scattering events $\tau$ and carrier effective mass $m^*$. Hence, $\mu$ can be increased by either increasing the time between scattering events and/or decreasing the effective mass of the carriers. This can be accomplished by changing the properties of the channel material and one way to do this is to strain it.
In bulk silicon, the conduction band is composed of a set of sixfold degenerate bands, $\Delta_6$, associated with electron transport along the six <001> crystal directions (Figure 1.3(a)). Intervalley scattering occurs between all six ellipsoids as they are degenerate in energy. The application of strain in the $x-y$ plane (Figure 1.3(b)) deforms the crystal and breaks the degenerate state into a fourfold ($\Delta_4$) and a twofold set ($\Delta_2$) [RIM 03]. Under tensile strain $\Delta_4$ is reduced in energy, resulting in an energy gap between $\Delta_4$ and $\Delta_2$, which becomes larger with more strain. Under compressive strain $\Delta_2$ becomes the lower energy state. In each case the total number of states an electron can scatter into is reduced and hence the scattering time increases. The combination of strain and vertical confinement in the electric field of a MOSFET also has the effect of distorting the electronic bandstructure such that the in plane effective mass is reduced and the out of plane ($z$-direction) mass is increased. Both the increased scattering time and reduced effective mass serve to increase the mobility in strained layers.

![Figure 1.3. Schematic representation of the conduction band occupations in (a) bulk silicon and (b) tensile strained silicon. Adapted from [RIM 03]](image)

Strain has a similar effect on increasing the mobility of holes in the valence band in bulk silicon. Initially there are two degenerate bands of light holes (LH) and heavy holes (HH) and a nearby spin-orbit (SO) band (Figure 1.4). Tensile strain shifts the LH band to a lower energy (for holes energy is taken in the opposite sense to electrons) resulting in a strain-dependant energy gap which reduces intervalley scattering. Again the distortions also serve to reduce the in-plane effective mass responsible for transport. The spin-orbit (SO) band is also shifted to higher energy than the LH and HH bands, further reducing scattering.

Compressive strain on the valence band decreases the HH energy and increases the LH energy thereby mainly populating the HH band and reducing the inter-valley scattering. This increases the mean free time between scattering effects. An additional effect of strain is that the curvature of the bands is changed by