Handbook of 3D Integration

3D Process Technology

Volume 3
Edited by
Philip Garrou, Mitsumasa Koyanagi, and Peter Ramm

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Contents

List of Contributors   XVII

1 3D IC Integration Since 2008   1
Philip Garrou, Peter Ramm, and Mitsumasa Koyanagi
1.1 3D IC Nomenclature   1
1.2 Process Standardization   2
1.3 The Introduction of Interposers (2.5D)   4
1.4 The Foundries   6
1.4.1 TSMC   6
1.4.2 UMC   7
1.4.3 GlobalFoundries   7
1.5 Memory   7
1.5.1 Samsung   7
1.5.2 Micron   8
1.5.3 Hynix   9
1.6 The Assembly and Test Houses   9
1.7 3D IC Application Roadmaps   10
References   11

2 Key Applications and Market Trends for 3D Integration and Interposer Technologies   13
Rozalia Beica, Jean-Christophe Eloy, and Peter Ramm
2.1 Introduction   13
2.2 Advanced Packaging Importance in the Semiconductor Industry is Growing   16
2.3 3D Integration-Focused Activities – The Global IP Landscape   18
2.4 Applications, Technology, and Market Trends   22
References   32

3 Economic Drivers and Impediments for 2.5D/3D Integration   33
Philip Garrou
3.1 3D Performance Advantages   33
3.2 The Economics of Scaling   33
### Contents

3.3 The Cost of Future Scaling 34
3.4 Cost Remains the Impediment to 2.5D and 3D Product Introduction 37
3.4.1 Required Economics for Interposer Use in Mobile Products 38
3.4.2 Silicon Interposer Pricing 38
References 40

### Interposer Technology

Venky Sundaram and Rao R. Tummala

4.1 Definition of 2.5D Interposers 41
4.2 Interposer Drivers and Need 42
4.3 Comparison of Interposer Materials 44
4.4 Silicon Interposers with TSV 45
4.5 Lower Cost Interposers 48
4.5.1 Glass Interposers 48
4.5.1.1 Challenges in Glass Interposers 49
4.5.1.2 Small-Pitch Through-Package Via Hole Formation and Ultrathin Glass Handling 49
4.5.1.3 Metallization of Glass TPV 51
4.5.1.4 Reliability of Copper TPVs in Glass Interposers 52
4.5.1.5 Thermal Dissipation of Glass 53
4.5.1.6 Glass Interposer Fabrication with TPV and RDL 53
4.5.2 Low-CTE Organic Interposers 53
4.5.3 Polycrystalline Silicon Interposer 55
4.5.3.1 Polycrystalline Silicon Interposer Fabrication Process 56
4.6 Interposer Technical and Manufacturing Challenges 57
4.7 Interposer Application Examples 58
4.8 Conclusions 60
References 61

### TSV Formation Overview

Dean Malta

5.1 Introduction 65
5.2 TSV Process Approaches 67
5.2.1 TSV-Middle Approach 68
5.2.2 Backside TSV-Last Approach 68
5.2.3 Front-Side TSV-Last Approach 69
5.3 TSV Fabrication Steps 70
5.3.1 TSV Etching 70
5.3.2 TSV Insulation 71
5.3.3 TSV Metallization 71
5.3.4 Overburden Removal by CMP 72
5.3.5 TSV Anneal 73
5.3.6 Temporary Carrier Wafer Bonding and Debonding 74
5.3.7 Wafer Thinning and TSV Reveal 74
5.4 Yield and Reliability 75
References 76

6 TSV Unit Processes and Integration 79
Sesh Ramaswami
6.1 Introduction 79
6.2 TSV Process Overview 80
6.3 TSV Unit Processes 82
6.3.1 Etching 82
6.3.2 Insulator Deposition with CVD 83
6.3.3 Metal Liner/Barrier Deposition with PVD 84
6.3.4 Via Filling by ECD of Copper 84
6.3.5 CMP of Copper 85
6.3.6 Temporary Bonding between Carrier and Device Wafer 86
6.3.7 Wafer Backside Thinning 86
6.3.8 Backside RDL 87
6.3.9 Metrology, Inspection, and Defect Review 87
6.4 Integration and Co-optimization of Unit Processes in Via Formation Sequence 88
6.5 Co-optimization of Unit Processes in Backside Processing and Via-Reveal Flow 89
6.6 Integration and Co-optimization of Unit Processes in Via-Last Flow 91
6.7 Integration with Packaging 92
6.8 Electrical Characterization of TSVs 92
6.9 Conclusions 96
References 97

7 TSV Formation at ASET 99
Hiroaki Ikeda
7.1 Introduction 99
7.2 Via-Last TSV for Both D2D and W2W Processes in ASET 103
7.3 TSV Process for D2D 105
7.3.1 Front-Side Bump Forming 106
7.3.2 Attach WSS and Thinning 106
7.3.3 Deep Si Etching from the Backside 107
7.3.4 Liner Deposition 107
7.3.5 Removal of SiO2 at the Bottom of Via 107
7.3.6 Barrier Metal and Seed Layer Deposition by PVD 110
7.3.7 Cu Electroplating 110
7.3.8 CMP 110
7.3.9 Backside Bump 111
7.3.10 Detach WSS 111
7.3.11 Dicing 112
7.4 TSV Process for W2W 113
7.4.1 Polymer Layer Coat and Development 114
### Section 7.4: TSV and Redistribution Process Flow

- **7.4.2 Barrier Metal and Seed Layer Deposition**
- **7.4.3 Cu Plating**
- **7.4.4 CMP**
- **7.4.5 First W2W Stacking (Face to Face)**
- **7.4.6 Wafer Thinning and Deep Si Etching**
- **7.4.7 TSV Liner Deposition and SiO₂ Etching of Via Bottom**
- **7.4.8 Barrier Metal and Seed Layer Deposition and Cu Plating**
- **7.4.9 CMP**
- **7.4.10 Next W2W Stacking**

### Section 7.5: Conclusions

### References

### Section 8: Laser-Assisted Wafer Processing: New Perspectives in Through-Substrate Via Drilling and Redistribution Layer Deposition

- **Marc B. Hoppenbrouwers, Gerrit Oosterhuis, Guido Knippels, and Fred Roozeboom**

#### 8.1 Introduction

#### 8.2 Laser Drilling of TSVs

- **8.2.1 Cost of Ownership Comparison**
- **8.2.2 Requirements for an Industrial TSV Laser Driller**

#### 8.2.3 Drilling Strategy

- **8.2.3.1 Mechanical**
- **8.2.3.2 Optical**

#### 8.2.4 Experimental Drilling Results

#### 8.3 Direct-Write Deposition of Redistribution Layers

- **8.3.1 Introduction on Redistribution Layers**
- **8.3.2 Direct-Write Characteristics**

#### 8.3.3 Direct-Write Laser-Induced Forward Transfer

#### 8.3.4 LIFT Results

#### 8.4 Conclusions and Outlook

### References

### Section 9: Temporary Bonding Material Requirements

- **Rama Puligadda**

#### 9.1 Introduction

#### 9.2 Technology Options

- **9.2.1 Tapes and Waxes**
- **9.2.2 Chemical Debonding**

#### 9.2.3 Thermoplastic Bonding Material and Slide Debonding

#### 9.2.4 Debonding Using Release Layers

#### 9.3 Requirements of a Temporary Bonding Material

#### 9.4 Considerations for Successful Processing

#### 9.4.1 Application of the Temporary Bonding Adhesive to the Device Wafer and Bonding to Carrier

#### 9.4.2 Moisture and Contaminants on Surface

### References
9.4.3 Total Thickness Variation 140
9.4.4 Squeeze Out 140
9.5 Surviving the Backside Process 141
9.5.1 Edge Trimming 142
9.5.2 Edge Cleaning 142
9.5.3 Temperature Excursions in Plasma Processes 143
9.5.4 Wafer Warpage due to CTE Mismatch 143
9.6 Debonding 144
9.6.1 Debonding Parameters in Slide-Off Debonding 144
9.6.2 Mechanical Damage to Interconnects 144
References 145

10 Temporary Bonding and Debonding – An Update on Materials and Methods 147
Wilfried Bair
10.1 Introduction 147
10.2 Carrier Selection for Temporary Bonding 148
10.3 Selection of Temporary Bonding Adhesives 151
10.4 Bonding and Debonding Processes 152
10.5 Equipment and Process Integration 155
References 156

11 ZoneBOND®: Recent Developments in Temporary Bonding and Room-Temperature Debonding 159
Thorsten Matthias, Jürgen Burggraf, Daniel Burgstaller, Markus Wimplinger, and Paul Lindner
11.1 Introduction 159
11.2 Thin Wafer Processing 159
11.2.1 Thin Wafer Total Thickness Variation 161
11.2.2 Wafer Alignment 163
11.3 ZoneBOND Room-Temperature Debonding 163
11.4 Conclusions 165
References 166

12 Temporary Bonding and Debonding at TOK 167
Shoji Otaka
12.1 Introduction 167
12.2 Zero Newton Technology 168
12.2.1 The Wafer Bonder 168
12.2.2 The Wafer Debonder 170
12.2.3 The Wafer Bonder and Debonder Equipment Lineups 170
12.2.4 Adhesives 170
12.2.5 Integration Process Performance 172
12.3 Conclusions 174
References 174
13 The 3M™ Wafer Support System (WSS) 175
Blake Dronen and Richard Webb
13.1 Introduction 175
13.2 System Description 175
13.3 General Advantages 177
13.4 High-Temperature Material Solutions 178
13.5 Process Considerations 180
13.5.1 Wafer and Adhesive Delamination 180
13.5.2 LTHC Glass Delamination 181
13.6 Future Directions 181
13.6.1 Thermal Stability 181
13.6.2 Elimination of Adhesion Control Agents 182
13.6.3 Laser-Free Release Layer 183
13.7 Summary 183
Reference 184

14 Comparison of Temporary Bonding and Debonding Process Flows 185
Matthew Lueck
14.1 Introduction 185
14.2 Studies of Wafer Bonding and Thinning 186
14.3 Backside Processing 186
14.4 Debonding and Cleaning 188
References 189

15 Thinning, Via Reveal, and Backside Processing – Overview 191
Eric Beyne, Anne Jourdain, and Alain Phommahaxay
15.1 Introduction 191
15.2 Wafer Edge Trimming 192
15.3 Thin Wafer Support Systems 194
15.3.1 Glass Carrier Support System with Laser Debonding Approach 196
15.3.2 Thermoplastic Glue Thin Wafer Support System – Thermal Slide Debondable System 196
15.3.3 Room-Temperature, Peel-Debondable Thin Wafer Support Systems 197
15.4 Wafer Thinning 198
15.5 Thin Wafer Backside Processing 202
15.5.1 Via-Middle Thin Wafer Backside Processing: “Via-Reveal” Process 202
15.5.1.1 Mechanical Via Reveal 202
15.5.1.2 “Soft” Via Reveal 202
15.5.2 Via-Last Thin Wafer Backside Processing 203
References 205
18.2.3.2 Edge Trimming 247
18.2.3.3 Grinding to Improve Flatness 248
18.2.3.4 Higher Level of Cleanliness 248
18.2.3.5 Via Reveal 249
18.2.3.6 Planarization 249
18.3 Dicing 250
18.3.1 Blade Dicing General 250
18.3.1.1 Dicing Method 250
18.3.1.2 Blade Dicing Point 250
18.3.1.3 Blade 251
18.3.1.4 Optimization of Process Control 252
18.3.1.5 Dicer 252
18.3.1.6 Dual Dicing Applications 252
18.3.2 Thin Wafer Dicing 253
18.3.3 Low-k Dicing 254
18.3.4 Other Laser Dicing 254
18.3.4.1 Ablation 254
18.3.4.2 Laser Full Cut Application 255
18.3.4.3 Stealth Dicing (SD) 256
18.3.5 Dicing Topics for 3D-IC Such as TSV 257
18.3.5.1 Cutting of Chip on Chip (CoC) and Chip on Wafer (CoW) 258
18.3.5.2 Singulation of CoW and Wafer on Wafer (WoW) 259
18.4 Summary 260
Further Reading 260

19 Overview of Bonding and Assembly for 3D Integration 261
James J.-Q. Lu, Dingyou Zhang, and Peter Ramm
19.1 Introduction 261
19.2 Direct, Indirect, and Hybrid Bonding 262
19.3 Requirements for Bonding Process and Materials 263
19.4 Bonding Quality Characterization 267
19.5 Discussion of Specific Bonding and Assembly Technologies 269
19.6 Summary and Conclusions 273
References 274

20 Bonding and Assembly at TSMC 279
Douglas C.H. Yu
20.1 Introduction 279
20.2 Process Flow 280
20.3 Chip-on-Wafer Stacking 281
20.4 CoW-on-Substrate (CoWoS) Stacking 283
20.5 CoWoS Versus CoCoS 283
20.6 Testing and Known Good Stacks (KGS) 284
20.7 Future Perspectives 285
References 285
21 TSV Packaging Development at STATS ChipPAC 287
Rajendra D. Pendse
21.1 Introduction 287
21.2 Development of the 3DTSV Solution for Mobile Platforms 289
21.3 Alternative Approaches and Future Developments 293
References 294

22 Cu–SiO₂ Hybrid Bonding 295
Léa Di Cioccio, S. Moreau, Loïc Sanchez, Floriane Baudin, Pierric Gueguen, Sebastien Mermoz, Yann Beilliard, and Rachid Taibi
22.1 Introduction 295
22.2 Blanket Cu–SiO₂ Direct Bonding Principle 296
22.2.1 Chemical–Mechanical Polishing Parameters 296
22.3 Aligned Bonding 299
22.3.1 Wafer-to-Wafer Bonding 299
22.3.2 Die-to-Wafer Bonding in Pick-and-Place Equipment 299
22.3.3 Die-to-Wafer by the Self-Assembly Technique 300
22.4 Blanket Metal Direct Bonding Principle 302
22.5 Electrical Characterization 304
22.5.1 Wafer-to-Wafer and Die-to-Wafer Copper-Bonding Electrical Characterization 304
22.5.2 Reliability 307
22.5.3 Thermal Cycling 307
22.5.4 Stress Voiding (SIV) Test on 200 °C Postbonding Annealed Samples 308
22.5.5 Package-Level Electromigration Test 309
22.6 Conclusions 310
References 311

23 Bump Interconnect for 2.5D and 3D Integration 313
Alan Huffman
23.1 History 313
23.2 C4 Solder Bumps 315
23.3 Copper Pillar Bumps 316
23.4 Cu Bumps 319
23.5 Electromigration 320
References 322

24 Self-Assembly Based 3D and Heterointegration 325
Takafumi Fukushima and Jicheol Bea
24.1 Introduction 325
24.2 Self-Assembly Process 325
24.3 Key Parameters of Self-Assembly on Alignment Accuracies 327
28 Implications of Stress/Strain and Metal Contamination on Thinned Die 379
Kangwook Lee and Mariappan Murugesan
28.1 Introduction 379
28.2 Impacts of Cu Contamination on Device Reliabilities in Thinned 3DLSI 379
28.3 Impacts of Local Stress and Strain on Device Reliabilities in Thinned 3DLSI 386
28.3.1 Microbump-Induced Stresses in Stacked LSIs 387
28.3.2 Microbump-Induced TMS in LSI 388
28.3.3 Microbump-Induced LMS 389
References 391

29 Metrology Needs for 2.5D/3D Interconnects 393
Victor H. Vartanian, Richard A. Allen, Larry Smith, Klaus Hummler, Steve Olson, and Brian Sapp
29.1 Introduction: 2.5D and 3D Reference Flows 393
29.2 TSV Formation 394
29.2.1 TSV Etch Metrology 395
29.2.2 Liner, Barrier, and Seed Metrology 397
29.2.3 Copper Fill Metrology (TSV Voids) 399
29.2.4 Cross-Sectional SEM (Focused Ion Beam Milling Sample Preparation) 400
29.2.5 X-Ray Microscopy and CT Inspection 400
29.2.6 Stress Metrology in Cu and Si 402
29.3 MEOL Metrology 404
29.3.1 Edge Trim Inspection 405
29.3.2 Bond Voids and Bond Strength Metrology 406
29.3.2.1 Acoustic Microscopy: Operation 407
29.3.2.2 Acoustic Microscopy for Defect Inspection and Review 407
29.3.2.3 Other Bond Void Detection Techniques 408
29.3.3 Bond Strength Metrology 409
29.3.4 Bonded Wafer Thickness, Bow, and Warp 410
29.3.4.1 Chromatic White Light 411
29.3.4.2 Infrared Interferometry 412
29.3.4.3 White Light Interferometry (or Coherence Scanning Interferometry) 414
29.3.4.4 Laser Profiling 415
29.3.4.5 Capacitance Probes 416
29.3.4.6 Differential Backpressure Metrology 417
29.3.4.7 Acoustic Microscopy for Measuring Bonded Wafer Thickness 417
29.3.5 TSV Reveal Metrology 418
29.4 Assembly and Packaging Metrology 420
29.4.1 Wafer-Level C4 Bump and Microbump Metrology and Inspection 421
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>29.4.2</td>
<td>Package-Level Inspection: Scanning Acoustic Microscopy</td>
<td>422</td>
</tr>
<tr>
<td>29.4.3</td>
<td>Package-Level Inspection: X-Rays</td>
<td>424</td>
</tr>
<tr>
<td>29.5</td>
<td>Summary</td>
<td>426</td>
</tr>
<tr>
<td></td>
<td>References</td>
<td>427</td>
</tr>
</tbody>
</table>

Index 431
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3D IC Integration Since 2008

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In Volume 1, we covered some of the history of the development of the 3D integrated circuit (3D IC) concept and we direct you to that chapter for such content [1].

Since the first two volumes of the Handbook of 3D Integration appeared in 2008, significant progress has been made to bring 3D IC technology to commercialization. This chapter will attempt to summarize some of the key developments during that period.

We previously described 3D IC integration as “an emerging, system level integration architecture wherein multiple strata (layers) of planar devices are stacked and interconnected using through-silicon (or other semiconductor material) vias (TSV) in the Z direction” as depicted schematically in Figure 1.1a and in cross section in Figure 1.1b [1].

With the continued pressure to miniaturize portable products and the near universal agreement that scaling as we have known it is soon coming to an end [2], a perfect storm has been created. The response to this dilemma at both the device and the package level has been to move into the third dimension.

It is commonly accepted that chip stacks wire-bonded down to a common laminate base and stacked packages such as package-on-package (PoP) are categorized as “3D packaging.” Transistor design has also gone vertical [3] as Intel [4] and others move to “finfet” stacked transistor structures at the 22 nm generation. These are compared pictorially in Figure 1.2.

In Figure 1.3, we compare system-on-chip (SoC), 3D packaging, and 3D IC with through-silicon via (TSV) in various performance categories [5].

1.1

3D IC Nomenclature

Since 2008 there have been attempts to further refine the nomenclature for 3D IC integration, although it has not yet been universally adopted in publications. In 2009 the International Technology Roadmap for Semiconductors (ITRS)
proposed the following nomenclature in an attempt to define the possible different levels of connections possible as circuits are deconstructed onto separate strata (see Table 1.1) [6].

1.2 Process Standardization

3D IC requires three new pieces of technology: (1) insulated conductive vias through a thinned silicon substrate (i.e., TSV); (2) thinning and handling technology for wafers as thin as 50 μm or less; (3) technology to assemble and package such thinned chips.
### Figure 1.3  Comparison of SoC, 3D packaging, and 3D IC [5].

<table>
<thead>
<tr>
<th>Level</th>
<th>Suggested name</th>
<th>Supply chain</th>
<th>Key characteristics</th>
</tr>
</thead>
</table>
| Package      | 3D packaging (3D-P)             | OSAT assembly printed circuit board (PCB) | • Traditional packaging of interconnect technologies, for example, wire-bonded die stacks, package-on-package stacks  
• Also includes die in PCB integration  
• No through-Si vias  
• WLP infrastructure, such as RDL and bumping  
• 3D interconnects are processed after the IC fabrication, “post IC passivation” (via-last process). Connections on bond-pad level  
• TSV density requirements follow bond-pad density roadmaps  
• Stacking of large circuit blocks (tiles, IP blocks, memory banks), similar to an SoC approach but having circuits physically on different layers  
• Unbuffered I/O drivers (low C, little or no ISD protection on TSVs)  
• TSV density requirement significantly higher than 3D-WLP: Pitch requirement down to 4–16 μm |
| Bond-pad     | 3D wafer-level packaging (3D-WLP) | Wafer-level packaging |                                                                                  |
| Global       | 3D stacked integrated circuit/3D system-on-chip (3D-SIC/3D-SoC) | Wafer fab |                                                                                  |
In the mid-2000s, practitioners were bewildered by the multitude of proposed technical routes to 3D IC. It has become clear, since then, that for most applications, the preferred process flow is what has been called a “via-middle” approach, where the TSVs are inserted after front-end transistor formation and early on during the on-chip interconnect process flow. This requires that TSVs are manufactured in back end of fab, not during or after the assembly process. This requires that TSV fabrication will be done by vertically integrated IDMs or foundries. TSV technology appears to be stabilized as depicted in Figure 1.4 and Table 1.2.

1.3
The Introduction of Interposers (2.5D)

Many believe the introduction of interposers (also known as 2.5D) was due to the failure of 3D IC, but this is not the case. Interposers were and are needed due to the lack of chip interface standardization and the need for a better thermal solution than is currently available for some 3D stacking situations.

The term “2.5D” is usually credited to Ho Ming Tong from Advanced Semiconductor Engineering (ASE), who in 2009 (or even earlier) declared that we might need an intermediate step toward 3D since the infrastructure and standards were not ready yet. The silicon interposer, Tong felt, would get us a major part of the way there, and could be ready sooner than 3D technology, thus the term “2.5D,” which immediately caught on with other practitioners [7].

2.5D interposers resemble silicon multichip module technology of the 1990s, with the addition of TSV [8]. In today’s applications, they provide high-density redistribution layers (RDLs), so the chips can be connected either through the interposer or next to each other on the top surface of the interposer as shown in
The latter is the superior thermal solution since all chips can be attached to a heat sink for cooling. Interposers will add cost and probably will not be a broadly accepted solution for low-cost mobile products, which would prefer straight 3D stacking [9].

Table 1.2  Standard 3D IC process flow options.

<table>
<thead>
<tr>
<th>Process</th>
<th>Preferred option</th>
<th>Alternative options available</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV formation</td>
<td>Bosch deep reactive ion etching (DRIE)</td>
<td>Laser</td>
</tr>
<tr>
<td>TSV Insulation</td>
<td>SiO₂</td>
<td>Polymer W</td>
</tr>
<tr>
<td>Conductor</td>
<td>Cu</td>
<td>pSi</td>
</tr>
<tr>
<td>Process flow</td>
<td>Via-middle</td>
<td>Via-first (for pSi)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Via-last (backside)a)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(front side)</td>
</tr>
<tr>
<td>Stacking Bonding</td>
<td>IMC</td>
<td>Cu–Cu</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Oxide bonding</td>
</tr>
<tr>
<td>Thin wafer handling</td>
<td>On carrier</td>
<td>Polymer bonding</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hybrid bonding</td>
</tr>
</tbody>
</table>

a) Preferred flow for CMOS image sensors.
1.4 The Foundries

1.4.1 TSMC

In October 2012, TSMC announced the readiness of their 2.5D CoWoSTM (chip-on-wafer-on-substrate) technology within their “Open Innovation Platform” and made public their reference flows supporting CoWoS. Several EDA companies including Cadence, Mentor, Synopsys, and Ansys were announced as partners in the CoWoS reference flow [10]. Their first public CoWoS demonstrator vehicle (Figure 1.6) included logic and DRAM in a single module using the wide I/O interface [11].

Early TSMC customers reportedly included Xilinx, AMD, Nvidia, Qualcomm, Texas Instruments, Marvell, and Altera [12], with Xilinx being the first to production in late 2011.

Figure 1.5 Interposer configurations.

Figure 1.6 2.5D TSMC demonstrator vehicle [11].