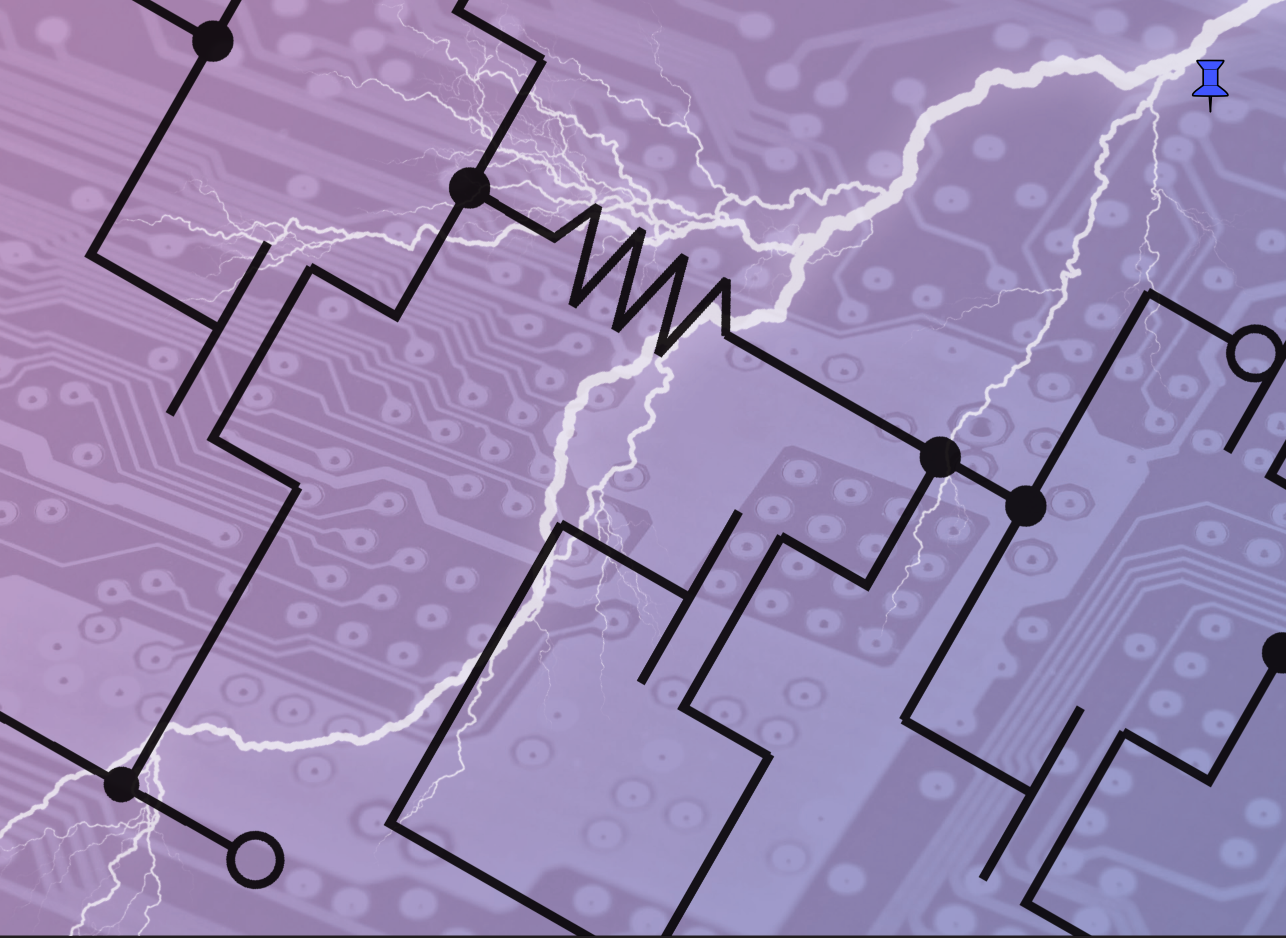
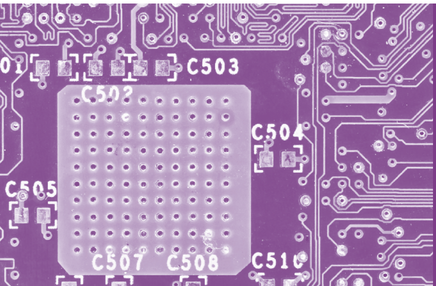


ESD

ANALOG CIRCUITS AND DESIGN

STEVEN H. VOLDMAN



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About the Author

Dr. Steven H. Voldman is the first IEEE Fellow in the field of electrostatic discharge (ESD) for "Contributions in ESD protection in CMOS, Silicon on Insulator and Silicon Germanium Technology." He received his B.S. in Engineering Science from the University of Buffalo (1979), a first M.S. EE (1981) from Massachusetts Institute of Technology (MIT), a second EE Degree (Engineer Degree) from MIT, a M.S. Engineering Physics (1986), and a Ph.D. in Electrical Engineering (EE) (1991) from University of Vermont under IBM's Resident Study Fellow program.

Voldman was a member of the semiconductor development of IBM for 25 years. He was a member of the IBM's Bipolar SRAM, CMOS DRAM, CMOS logic, Silicon on Insulator (SOI), 3-D memory team, BiCMOS and Silicon Germanium, RF CMOS, RF SOI, smart power technology development, and image processing technology teams. In 2007, Voldman joined the Qimonda Corporation as a member of the DRAM development team, working on 70, 58, 48, and 32 nm CMOS DRAM technology. In 2008, Voldman worked as a full-time ESD consultant for Taiwan Semiconductor Manufacturing Corporation (TSMC) supporting ESD and latchup development for 45 nm CMOS technology and a member of the TSMC Standard Cell Development team in Hsinchu, Taiwan. From 2009 to 2011, Steve was a Senior Principal Engineer working for the Intersil Corporation working on analog, power, and RF applications in RF CMOS, RF Silicon Germanium, and SOI. From 2013 to 2014, Dr. Voldman was a consultant for the Samsung Electronics Corporation in Dongtan, South Korea.

Dr. Voldman was the chairman of the SEMATECH ESD Working Group, from 1995 to 2000. In his SEMATECH Working Group, the effort focused on ESD technology benchmarking, the first transmission line pulse (TLP) standard development team, strategic planning, and JEDEC-ESD Association standards harmonization of the human body model (HBM) Standard. From 2000 to 2013, as Chairman of the ESD Association Work Group on TLP and very-fast TLP (VF-TLP), his team was responsible for initiating the first standard practice and standards for TLP and VF-TLP. Steve Voldman has been a member of the ESD Association Board of Directors, and Education Committee. He initiated the "ESD on Campus" program which was established to bring ESD lectures and interaction to university faculty and students internationally; the ESD on Campus program has reached over 40 universities in the United States, Korea, Singapore, Taiwan, Malaysia, Philippines, Thailand, India, and China. Dr. Voldman has taught short courses and tutorials on ESD, latchup, patenting, and invention.

He is a recipient of 250 issued US patents and has written over 150 technical papers in the area of ESD and CMOS latchup. Since 2007, he has served as an expert witness in patent litigation and has also founded a limited liability corporation (LLC) consulting business supporting patents, patent writing, and patent litigation. In his LLC, Voldman served as an expert witness for cases on DRAM development, semiconductor development, integrated circuits, and electrostatic discharge. He is presently writing patents for law firms. Steven Voldman provides tutorials and lectures on inventions, innovations, and patents in Malaysia, Sri Lanka, and the United States.

Dr. Voldman has also written many articles for *Scientific American* and is an author of the first book series on ESD and latchup (eight books): *ESD: Physics and Devices*, *ESD: Circuits and Devices*, *ESD: Radio Frequency (RF) Technology and Circuits, Latchup, ESD: Failure Mechanisms and Models, ESD Design and Synthesis, ESD Basics: From Semiconductor Manufacturing to Product Use*, and *Electrical Overstress (EOS): Devices, Circuits and Systems*, as well as a contributor to the book *Silicon Germanium: Technology, Modeling and Design* and *Nanoelectronics: Nanowires, Molecular Electronics, and Nano-devices*. In addition, the International Chinese editions of book *ESD: Circuits and Devices, ESD: Radio Frequency (RF) Technology and Circuits*, and *ESD Design and Synthesis* (2014) are also released.

Preface

This book *Electrostatic Discharge (ESD): Analog Circuits and Design* was initiated based on the need to produce a text that addresses the fundamentals of electrostatic discharge (ESD) requirements for analog and power electronic devices, components and systems. As the manufacturing world evolves, semiconductor devices are scaling and systems are changing. As a result, the needs and requirements of reliability and ESD robust products are increasing. A text is required that connects and synthesizes the fundamentals of analog design discipline and the ESD discipline. Whereas significant texts are available today to teach experts on ESD on-chip design for digital design discipline and radio frequency (RF) design discipline, there is no single textbook devoted to ESD on-chip design dedicated to analog design.

With the growth of mixed signal applications that integrate both the digital and analog circuitries on a common semiconductor chip, there is a growing interest in the concerns associated with ESD design and protection within a digital–analog application. New issues arise by the integration of two separate cores within a chip, where the digital and the analog domains are separated spatially and electrically. As a result, new problems arise with the design synthesis and architecture of an analog–digital mixed signal semiconductor chip.

With the growth of power management and power devices, there is an additional challenge in providing ESD protection within a power application. In power technology, the number of allowed power conditions has grown significantly, leading to a significant difficulty to provide ESD protection.

In addition, there is a growing interest in electrical overstress (EOS). Today, there is a need for understanding the fundamentals of EOS. Necessarily experts, non-experts, non-technical staff and layman should understand the problems that the world faces today. Today, real-world EOS issues surround us; this occurs in manufacturing environments, power sources, machinery, actuators, solenoids, soldering irons, cables, and lightning. When there is switching, poor grounding, ground loops, noise and transient phenomena, there is a potential for EOS of devices, components, and printed circuit boards. Hence, there is a need for experts and non-experts to understand the issues that revolve around us and the steps to be taken to avoid them. At present, this book is the only textbook on the issues of EOS. In this book, EOS issues for analog and power applications are emphasized.

Hence, there is an opportunity to intermix the analog design discipline and the ESD design discipline to produce a synthesized "ESD analog design discipline" that utilizes analog design techniques and ESD protection techniques.

This book has multiple goals and are as follows.

The first goal is to teach the basic and fundamental concepts of the analog design discipline.

The second goal is to review the analog circuit building blocks used in analog design, such as current mirrors, error amplifiers, feedback loops, and comparators, and to discuss the bandgap reference circuits and low dropout regulators.

The third goal is to discuss EOS and ESD, that is to explain the practices, devices, and novel concepts to address both ESD and EOS on-chip and off-chip.

The fourth goal is to discuss the needs for analog circuits and design associated with CMOS latchup. This involves understanding of latchup in a mixed signal digital–analog environment.

The fifth goal is to explain the semiconductor chip floorplanning to address ESD, EOS and latchup in an analog–digital mixed signal environment. Latchup issues, placement, and guard ring requirements will be highlighted.

The sixth goal is to describe the novel concepts that provide both analog and ESD advantages.

And, the last goal is to highlight the electrical design automation (EDA) methods for analog, analog–digital mixed signal, and power electronics to provide ESD and EOS robust products.

This book is organized as to allow the reader to learn the fundamentals of ESD analog design.

In Chapter 1, analog design principles associated with matching and design symmetry are discussed, and EOS and its relationship with other phenomena, such as ESD, electromagnetic interference, electromagnetic compatibility, and latchup are explained. EOS is defined as well in terms of electrical over-current, electrical over-power, and other concepts. ESD and EOS events on analog applications are also emphasized. As a result, we will draw distinctions through the text on difference of failure analysis, time constants, and other means of identification and classification. A plan to define safe operating area and its role in EOS is also emphasized.

In Chapter 2, the analog design layout practices of interdigitated design layout and common centroid concepts in one- and two dimensions are discussed. These concepts are implemented into ESD networks and the cosynthesis of analog circuits and ESD networks.

In Chapter 3, examples of analog building blocks and circuits that exist in analog designs are provided for readers unfamiliar with analog circuit networks. The analog circuit examples include single-ended receivers, differential receivers, comparators, current mirrors, bandgap regulators, and voltage converters. Voltage regulators of interest include buck, boost, buck–boost, and other circuit topologies.

In Chapter 4, the analog ESD design discipline is introduced, applying both the ESD requirements and the layout concepts of analog circuitry. This includes the digital ESD design discipline, in contrast to the analog ESD design discipline.

In Chapter 5, the analog design synthesis on a high level, by addressing the floorplanning of a mixed signal chip application is discussed. This includes the digital and analog power domain floorplanning, digital and analog power grid, digital to analog breaker cells, and ESD concerns in digital–analog mixed signal chips. Additionally, the guard ring and moats within the chip architecture are discussed, and active and passive guard ring concepts are shown.

In Chapter 6, the signal line ESD failures in digital and analog domains where they are required to be decoupled due to noise are addressed. ESD solutions between the ground connections include coupling using resistors, diode elements, as well as third-party functional blocks. ESD solutions along the signal lines include the ground connections as well as the ESD networks on the signal lines that cross the digital to analog domain.

In Chapter 7, the analog and ESD signal pin cosynthesis that introduces the usage of inter-digitated layout and common centroid concepts to provide ideal matching, low capacitance, and small area in differential signal pins is addressed. Using interdigitated designs, the parasitic elements are utilized for signal pin-to-signal pin ESD protection. In conclusion, the issue of common centroid design of ESD protection networks which integrates signal pin-to-signal pin ESD protection with the inter-digitation pattern for ESD pin-to-rail protection network for differential pair circuitry is discussed for the first time. With integration of the ESD pin-to-rail solution and the ESD signal pin solution, a significant reduction in the area and loading effect for CMOS differential circuits is established. This novel concept will provide significant advantage for present and future high-performance analog and RF design for matching, area reduction, and performance advantages.

In Chapter 8, analog and ESD integration is focused. Topics such as analog signal pin input circuitry and ESD power clamps are discussed, and ESD power clamp issues and solutions are explained in more details. Significant discussion is provided due to the importance of ESD power clamps in analog and digital ESD design.

In Chapter 9, the system-level issues associated with EOS in chips, printed circuit boards, and systems are discussed. EOS protection device classifications, symbols, and types for both over-voltage or over-current conditions are highlighted. System-level and system-like testing methods, such as IEC 61000-4-2, IEC 61000-4-5, and human metal model waveforms and methods, are reviewed. Examples for printed circuit board design for digital–analog systems are also provided. The EDA techniques and methods for ESD in analog design are also discussed. Methods such as design rule checking (DRC), layout versus schematic (LVS), and electrical rule checking (ERC) are used for both ESD and EOS checking and verification.

In Chapter 10, latchup in analog design is discussed and solutions to avoid digital noise from impacting analog circuitry are addressed. The spatial placement of digital and analog cores in a mixed signal chip as well as the guard rings between these domains are also explained. Moats, guard rings, and through-silicon via advantages and disadvantages as possible solutions to minimize both noise and latchup are highlighted. Special features, such as grounded wells, and decoupling capacitor issues and how they can lead to latchup in analog applications are also reviewed. In conclusion, I/O to I/O interactions as a function of standard cell-to-standard cell spacings are discussed. As technology spacings are reduced, cell-to-cell latchup will increase in importance in analog design.

In Chapter 11, ESD and EOS libraries and documents for an analog or mixed signal technology are discussed. The discussion includes a plethora of items, from analog libraries, ESD library elements, Cadence™-based parameterized cells, Cadence-based hierarchical ESD designs, to ESD cookbooks. ESD and EOS documents for technology design manual, cookbooks, checklists, and design release processes are discussed. Control programs and documents for analog ESD design are highlighted. This includes ESD analog design “cookbooks” to assist design teams to determine the correct elements to use for a given circuit.

In Chapter 12, EDA techniques and methods for ESD, EOS, and latchup are discussed. Methods such as DRC, LVS and ERC are used for ESD, latchup, and EOS checking and verification. As time progresses, ESD CAD methods are being propagated to EOS CAD methods, to address ESD and EOS in the same design tool. The example of Calibre PERC™ shows how the methods of ESD are being extended to the EOS issue. A key issue is the checking and verification of analog-to-digital cross domain sign lines. This trend will continue in the future.

This introductory text will hopefully open your interest in the field of ESD in analog design. To establish a stronger knowledge of ESD protection, it is advisable to read other texts such as *ESD Basics: From Semiconductor Manufacturing to Product Use*, *ESD: Physics and Devices, ESD: Circuits and Technology, ESD: RF Circuits and Technology, ESD: Failure Mechanisms and Models, ESD: Design and Synthesis, EOS: Devices, Circuits and Systems,* and *Latchup.*

Enjoy the text, and enjoy the subject of ESD design in analog devices, circuitry, and systems.

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1 Analog, ESD, and EOS

In 1993, I was invited to consult for two days with a well-known semiconductor analog corporation on electrostatic discharge (ESD) protection of analog components. A vice president of the corporation sat with me and said, "Our analog products are superior to any of our competitors. As a result, no one cared about the level of our ESD protection results! All of our products did not achieve 2000 V HBM or 4000 V HBM levels. Today, with growth of competition in the analog business sector, overnight, 75% of our customers want us to achieve better than 2000 V HBM levels on all of our products! How do I build a corporate ESD strategy for this analog corporation ?…"

This was my first introduction to the world of ESD in analog design.

1.1 ESD IN ANALOG DESIGN

In every technology sector, electrostatic discharge (ESD) protection was not an issue when there was a sole supplier of critical products and the customer was willing to accept the product. Eventually, as the technology or application space matured, customers wanted better ESD protection as both technology and application became mainstream or high volume. This was true historically in digital and analog applications with CMOS, bipolar, silicon on insulator (SOI), silicon germanium (SiGe), and gallium arsenide (GaAs) technologies. With mainstream introduction of a technology, it is desirable not to have customer field returns from ESD or electrical overstress (EOS).

As a result of the unique needs of analog design, there are a significant number of issues to be addressed in analog ESD design. These issues extend from chip design to system-level design in both architecture and layout, which consist of the following:

- Matching and layout issues
- Matching requirements in differential receivers

ESD: Analog Circuits and Design, First Edition. Steven H. Voldman.

- Domain-to-domain separation and ESD coupling
- Circuit topology chip architecture and ESD
- Interdomain digital-to-analog ESD failures
- Semiconductor chip layout floor planning
- Printed circuit board (PCB) design floor planning
- High-voltage applications
- Ultrahigh-voltage applications

In this text, examples will be provided of ESD failures and problems in past analog applications to modern-day practices in analog design. The text will discuss how the present-day architecture of mixed-signal chips evolved and its implications.

1.2 ANALOG DESIGN DISCIPLINE AND ESD CIRCUIT TECHNIQUES

In analog design, unique design practices are used to improve the functional characteristics of analog circuitry [1–10]. In the ESD design synthesis of analog circuitry, the ESD design practices must be suitable and consistent with the needs and requirements of analog circuitry [11, 12] (Figure 1.1). Fortunately, many of the analog design practices are aligned with ESD design practices.

In the analog design discipline, there are many design techniques to improve tolerance of analog circuits [10]. Analog design techniques include the following:

- Local matching: Placement of elements close together for improved tolerance
- Global matching: Placement in the semiconductor die
- Thermal symmetry: Design symmetry

A key analog circuit design requirement is matching. To avoid semiconductor process variations, matching is optimized by the local placement. Placement within the die location also is an analog concern due to mechanical stress effects. In analog design, there is a concern of the temperature field within the die and the effect of temperature distribution within the die.

Many of the analog design synthesis and practices are also good ESD design practices. The design practices of matching and design symmetry are also suitable practices for

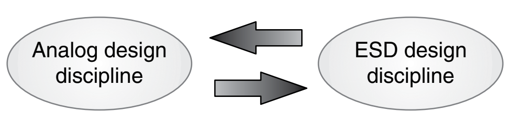

Figure 1.1 Analog and ESD design.

ESD design. But there are some design practices where a trade-off exists between the analog tolerance and ESD; this occurs when parasitic devices are formed between the different analog elements within a given circuit or circuit to circuit.

1.2.1 Analog Design: Local Matching

Matching is important in analog design due to the usage of many circuit blocks that require good matching characteristics. The matching is important locally in a semiconductor device or within a circuit. In this case, "local matching" is needed to provide the ideal characteristics of an analog network. Local matching is critical in multifinger structures, where mismatch can occur between two adjacent structures. In future sections, discussion of semiconductor processes such as photolithography and etching influences the local matching.

1.2.2 Analog Design: Global Matching

Matching is important in analog design due to the usage of many circuit blocks that require good matching characteristics from circuit to circuit. Many functional analog circuit blocks are repeated within a semiconductor chip. In this case, "global matching" is needed to avoid mismatch between two circuits. Global matching is influenced by spatial separation of two circuits, global density variations, arrangement, and orientation. Global matching is influenced by across chip linewidth variation (ACLV).

1.2.3 Symmetry

Symmetry is critical to establish matching within a semiconductor device or an analog circuit (Figure 1.2). Symmetry is influenced by design layout, current distribution, temperature field, and thermal distribution [10].

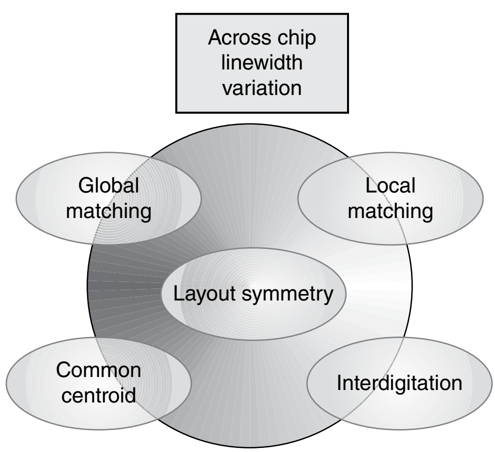

Figure 1.2 Symmetry and layout.

1.2.3.1 Layout Symmetry

Layout symmetry is a form of symmetry through physical design. Layout symmetry establishes matching within a semiconductor device or an analog circuit [10].

1.2.3.2 Thermal Symmetry

Thermal symmetry is a form of symmetry through the temperature field and thermal distribution. Thermal symmetry establishes matching within a semiconductor device or an analog circuit [10].

1.2.4 Analog Design: Across Chip Linewidth Variation

In semiconductor development, semiconductor process variation can introduce structural and dimensional nonuniformity which influences both analog circuits and ESD devices [13–22]. Photolithography and etch tools can introduce these nonuniformities that exist on a local and global design level. These variations can manifest themselves by introducing variations in both active and passive elements. For MOSFET transistors, variation in the MOSFET channel length in single-finger and multifinger MOSFET layouts can lead to nonuniform "turn-on"; this effect can influence both active functional circuits and ESD networks. In bipolar transistors, the linewidth variation can lead to different sizes in emitter structures, leading to nonuniform current distribution in multifinger bipolar transistors. For resistor elements, resistor elements that are utilized for ballasting in multifinger structures can also lead to nonuniform current in the different fingers in the structure.

Design factors that influence the lack of variation are the following semiconductor process and design variables:

- Linewidth
- Line-to-line space
- "Nested-to-isolated" ratio
- Orientation
- Physical spacing between identical circuits

It is a circuit design practice and an ESD design synthesis practice to provide a linewidth which is well controlled. For line-to-line space, in an array of lines, the spacing is maintained to provide maximum matching between adjacent lines. For example, in a multifinger MOSFET structure, the spacing between the polysilicon lines is equal to provide the maximum matched characteristics.

Given any array of parallel lines, the characteristics of the "end" or edges of the array can have different characteristics than the other lines. In an array of lines, whereas one edge is adjacent to another line, the other edge is not; this leads to one line-to-line edge space to appear "nested" and the outside line-to-line edge space to appear "semi-infinite"