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Bottom right: Dual-axis acceleration sensor
ADXL-203 by Analog Devices Inc., USA.
Top left: Packaged pressure sensor KP-100 by
Infineon Technologies AG, Germany.
We, the CMOS-MEMS volume editors, welcome you to this second installment of Advanced Micro & Nanosystems. Today's microelectromechanical systems (MEMS) are built much the same way as silicon integrated circuits (ICs) are, borrowing a variety of materials and processes from the IC industry. It is thus not surprising that from the early days of MEMS more than three decades ago, researchers have tried to co-integrate microelectromechanical devices with bipolar or CMOS circuitry. The challenges, achievements and prospects of the research and development work in the area of CMOS-integrated MEMS, or for short CMOS-MEMS, are the topics of the present book. CMOS technology and micromachining techniques are combined to fabricate a wide spectrum of microsystems ranging from physical sensors, e.g., pressure and inertial sensors, to chemical and biochemical sensing systems.

The field of CMOS-MEMS dates back to the mid 1980s, but has grown substantially in the past decade. An early example of CMOS-integrated MEMS is the CMOS-based piezoresistive pressure sensing system developed by NEC and published 1987 in the IEEE Journal of Solid-State Circuits. Integrated pressure sensors using bipolar instead of CMOS technologies were developed already in the late 1970s, e.g., at the University of Michigan and Case Western University. In 1993, Analog Devices introduced the first CMOS-integrated surface-micromachined accelerometer, the ADXL-50, to the commercial market. Recently, the same company has released the first CMOS-integrated gyroscope with on-chip circuitry capable of detecting capacitance changes in the zepto-F (10^{-21} F) range. Another exemplary integrated microsystem is the Texas Instruments Digital Micromirror Device (DMD™) featuring up to 1.3 million individually addressable micromirrors on a single chip, which would hardly be feasible without the underlying CMOS addressing electronics. Established fabrication processes, co-integration of powerful analog and digital circuitry, and the possibility of large sensor arrays are the clear benefits of using CMOS technologies to develop MEMS. Besides the above mentioned, by now almost classical applications, CMOS-MEMS have in recent years also found their way into new areas, including chemical and biochemical sensing, biomimetics, acoustics, and RF components.

The present volume of Advanced Micro & Nanosystems has been divided into eleven chapters, providing a broad overview on current and past activities in the area.
of CMOS-MEMS. To our best knowledge, it is the first book dedicated to CMOS-MEMS and hopefully will serve as a valuable reference for you, our reader.

The volume starts off with Oliver Brand’s overview chapter on CMOS-MEMS fabrication approaches, organizing the different process flows according to where the micromachining process steps are added to the CMOS base line, i.e., pre-CMOS, intermediate-CMOS, and post-CMOS approaches. Design of CMOS-MEMS requires not only the knowledge of electrical, but also thermal and mechanical material properties.

In the second chapter, Patrick Ruther and Oliver Paul present a detailed overview on measurement techniques used to extract relevant properties of mainly thin film materials and have assembled a large amount of material property data in a valuable tabular format.

Chapter 3 by Gary Fedder, Junseok Chae, Haluk Kulah, Khalil Najafi, Tim Denison and Steve Lewis takes a close look at CMOS-integrated accelerometers and gyroscopes, including some of the commercially most successful CMOS-MEMS products. Miniaturized acoustic devices, namely loudspeakers and microphones, have become ubiquitous in our daily life; we find them in our phones, computers and our children’s toys. Recent advances in the area of CMOS-based acoustic devices are discussed by John Neumann and Kaigham Gabriel in Chapter 4.

With CMOS transistors reaching ever higher frequencies with each new technology cycle, the use of CMOS-MEMS approaches to build RF MEMS devices, such as switches or high-frequency variable capacitors, has potential to create wholly on-chip wireless systems. Chapter 5 by Tamal Mukherjee and Gary Fedder gives an overview on recently developed RF CMOS-MEMS components and circuits.

Pressure sensors were the first commercially available high-volume MEMS product, and thus it is not surprising that a large number of CMOS-integrated pressure sensors have been demonstrated over the past 20 years. In Chapter 6, Hans-Jörg Timme reviews the theoretical background for micromachined pressure sensors and compares different CMOS-based implementation strategies.

The following three chapters concentrate on chemical and biological applications of CMOS-MEMS. Keeping in mind the possibility of sensor arrays and on-chip analog and digital electronics, CMOS-based microsystems are especially suited for small, hand-held devices in applications ranging from chemical safety, security and access control to biomedical diagnostics. In Chapter 7, Andreas Hierlemann discusses basic chemical sensor concepts and reviews chemical sensors based on CMOS technology. Access control is an important aspect in our daily life and there is hope that secure biomimetic access control systems will at some point diminish the need to memorize dozens of passwords. In Chapter 8, Christopher Hierold, Gerd Hribernig, and Thomas Scheiter take a close look at capacitive fingerprint sensor systems, discussing not only the actual CMOS-based fingerprint sensors, but all the system aspects that need to be addressed while developing a biometric authentication system. Finally, Jan Lichtenberg and Henry Baltes discuss in Chapter 9 the relatively young field of CMOS-based biochemical sensing systems, including biosensor arrays and cell-based assays.
Micromachining techniques are used to machine, e.g., the silicon substrate and can provide microstructures with excellent thermal isolation. Besides this, thermal sensors often require only resistive elements and can be readily integrated with CMOS technology. Chapter 10 by Tayfun Akin discusses new developments in the areas of CMOS-based thermal radiation sensors, thermal flow sensors and thermal converters. The present AMN volume closes with a chapter by Christoph Hagleitner and Kay-Uwe Kirstein on circuit and system integration, taking an in-depth look at all the relevant aspects, including common analog front-end circuitry architectures for integrated microsensors, and important building blocks for CMOS-MEMS, such as filters, analog-to-digital converters, current/voltage references and calibration/data interfaces.

Last but not least, this is the time and place to thank our authors for their hard work and timely chapter contributions. The editors are grateful to the publisher, Wiley-VCH, for the support of the book series. In particular, we thank the publishing editor, Dr. Martin Ottmar, for the management of AMN and the project editor, Dr. Waltraud Wüst, for her never-ending support in carrying this volume from the early concept phase all the way to the actual printing.

This book will be the last in the series for which we benefit from having Henry Baltes as a co-editor. We are deeply grateful to Henry for his many contributions to the new AMN series and its precursor, Sensors Update. As one of the leaders in the CMOS-MEMS field, it is fitting that this volume be on the topic that Henry helped to pioneer. Thank you, Henry!

Oliver Brand and Gary K. Fedder, Volume Editors

November 2004
Atlanta and Pittsburgh
Foreword

We are proud to present the second volume of Advanced Micro & Nanosystems (AMN), entitled CMOS-MEMS and entirely dedicated to this topic. It examines and illustrates the recent, significant advances in the field of CMOS-integrated microelectromechanical systems. With all of the series editors having a background in using CMOS processes for microsystem development, a book like this has been on our minds for quite some time. Oliver Brand and Gary Fedder as volume editors have now assembled an international team of experts from academia and industry as chapter authors to cover all the facets of CMOS-MEMS, and also act as chapter contributors themselves in this work that we believe you will find useful and exciting.

Covering recent advances from the world of micro and nanosystems, future AMN issues will either focus on a particular subject, such as the present CMOS-MEMS, or be a carefully chosen set of cutting-edge overview and review articles like the first AMN volume on Enabling Techniques for MEMS and Nanodevices.

Looking ahead, we hope to welcome you back, dear reader, to the upcoming third member of the AMN series, in which we leave the area of silicon-based micro- and nanosystems to take a close look at the fascinating field of Microengineering of Metals and Ceramics. The articles will range from the design, tooling, advanced replication techniques, automation and quality assurance all the way to the resulting properties of materials and microcomponents. To cover such a wide spectrum, we are very glad to have the support of two well-known experts in the field, Prof. Detlef Löhne from the University of Karlsruhe, Germany, and Prof. Jürgen Haßelt from the University of Freiburg, Germany, who will edit this volume together.

Henry Baltes, Oliver Brand, Gary K. Fedder, Christofer Hierold, Jan G. Korvink, and Osamu Tabata, Series Editors

November 2004
Zurich, Atlanta, Pittsburgh, Freiburg and Kyoto
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1

Fabrication Technology

Abstract
This chapter provides an overview on fabrication technologies for CMOS-based microelectromechanical systems (MEMS). The first part briefly introduces the basic microfabrication steps, highlights a CMOS process sequence and how CMOS materials can be used for microsystems design. While a number of microsystems can be fabricated within the regular CMOS process sequence, the focus of the chapter is on combining CMOS technology with micromachining process modules. CMOS-compatible bulk and surface micromachining techniques are introduced in the second part of the chapter together with an overview of the design challenges faced when combining mechanical microstructures and electronics on the same substrate. The micromachining modules can either precede (pre-CMOS), follow (post-CMOS) or be performed in between (intra-CMOS) the regular CMOS process steps. The last part of the chapter provides an extensive overview on the different CMOS-based MEMS approaches found in the literature.

Keywords
Micromachining; CMOS-based MEMS; MEMS fabrication; microsystem fabrication

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1.1.1.1 Thin Film Deposition  5
1.1.1.2 Patterning  6
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1.1 CMOS Technology

State-of-the-art CMOS processes, such as IBM’s 9S2 process based on SOI (silicon-on-insulator) technology on 300 mm wafers, feature a minimal physical gate length of less than 100 nm and up to eight (copper) metallization levels (see Fig. 1.1, [1]). Such advanced CMOS processes are required for the fabrication of today’s and tomorrow’s microprocessors comprising tens of millions of transistors on a single chip. An example is Apple Computer’s 64-bit PowerPC-G5 processor with more than 58 million transistors [2], manufactured using IBM’s 90 nm CMOS technology.

Researchers at IBM’s T.J. Watson Research Center have recently used the copper-based interconnect technology of such modern CMOS processes to fabricate microelectromechanical devices, namely r.f. switches and resonators [3, 4]. Up to now, however, most commercially available microsystems combining (micromachined) transducer elements and integrated electronics on a single chip rely on CMOS or BiCMOS processes with minimum feature sizes typically between 0.5 and 3 μm and 4 or 6 in wafer sizes. While the underlying CMOS technologies are between 10 and 15 years old, their capabilities are sufficient for most microsystem applications. An example is the pressure sensor KP100 by Infineon Technologies, a surface micromachined pressure sensor array with on-chip circuitry for signal conditioning, A/D conversion, calibration and system diagnostic, which is based on a 0.8 μm BiCMOS technology on 6 in wafers [5].

A typical cross-section of a sub-μm (0.5–1.0 μm) CMOS technology used for CMOS-based microelectromechanical systems (MEMS) is shown in Fig. 1.2 [6].
The twin-well technology is based on 6 in p-type wafers and uses a polysilicon/silicide gate, low-doped drain (LDD) technology for source and drain formation, silicid e source/drain contacts and a two-level metallization based on tungsten plugs and aluminum interconnects. A thermal oxide separates adjacent transistors, chemical vapor deposition (CVD) silicon dioxide layers are used as dielectric layers between the metallization levels and a PECVD (plasma enhanced CVD) silicon nitride layer or a silicon dioxide, silicon nitride sandwich are employed as pas-

---

**Fig. 1.1** Cross-section of IBM's 90 nm CMOS technology with 8-level copper metallization (labeled M1–M8) with close-up of three metal–oxide–semiconductor field effect transistors (MOSFETs). Images courtesy of International Business Machines Corporation; unauthorized use not permitted.

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**Fig. 1.2** Schematic cross-section of typical sub-μm (0.5–1.0 μm) CMOS technology with two-level aluminum metallization and TiN local interconnects. Adapted from [6].
sivation layer. The CMOS fabrication sequence is briefly highlighted in Section 1.1.2. More detailed process descriptions can be found in a number of microelectronics textbooks, e.g. [6–8].

When designing CMOS-based MEMS or microsystems, the designer must adhere, to a great extent, to the chosen CMOS process sequence in order not to sacrifice the functionality of the on-chip electronics. This limits the available ‘design space’ for the integrated microsystems, as e.g. materials, material properties and layer thicknesses are determined by the CMOS process. In the following, a brief introduction into integrated circuit fabrication will be given: the basic fabrication steps are highlighted (Section 1.1.1) and a CMOS process sequence is summarized (Section 1.1.2). Section 1.1.3 discusses how the different CMOS materials and layers can be used in micro- and nanosystems and Section 1.1.4 depicts a few microsystems that can be completely formed within a regular CMOS sequence.

1.1.1

Basic Microfabrication Steps

The fabrication of integrated circuits (ICs) using CMOS or BiCMOS technology is based on four basic microfabrication techniques: deposition, patterning, doping and etching. Fig. 1.3 illustrates how these techniques are combined to build up an IC layer by layer: a thin film, such as an insulating silicon dioxide film, is deposited on the substrate, a silicon wafer. A light-sensitive photoresist layer is then deposited on top and patterned using photolithography. Finally, the pattern is transferred from the photoresist layer to the silicon dioxide layer by an etching process. After removing the remaining photoresist, the next layer is deposited and struc-

![Fig. 1.3 Flow diagram of IC fabrication process using the four basic microfabrication techniques: deposition, photolithography, etching and doping. Adapted from [8]](image-url)
Doping of a semiconductor material by ion implantation, the key step for the fabrication of diodes and transistors, can be performed directly after photolithography, i.e. using a photoresist layer as mask, or after patterning an implantation mask (e.g. a silicon dioxide layer).

Silicon is the standard substrate material for IC fabrication and, hence, the most common substrate material in microfabrication in general. It is supplied as single-crystal wafers with diameters between 100 and 300 mm. In addition to its favorable electrical properties, single-crystal silicon also has excellent mechanical properties [9], which enable the design of micromechanical structures. CMOS processes for digital electronics typically use low-doped (doping concentration in the $10^{16} \text{ cm}^{-3}$ range) silicon wafers, whereas processes for mixed-signal or analog electronics are often based on high-doped (doping concentration in the $10^{19} \text{ cm}^{-3}$ range) wafers with a low-doped epitaxial layer to minimize latch-up. The choice of the substrate material might already require a compromise between the requirements for the MEMS part and the on-chip electronics: the fabrication of membrane structures for, e.g., pressure sensors is typically based on anisotropic silicon etching in a potassium hydroxide (KOH) solution (see Section 1.2). High p-type doping ($N_A \geq 10^{19} \text{ cm}^{-3}$) substantially reduces the silicon etch rates in KOH solutions, thus preventing the use of highly p-doped CMOS substrates in combination with KOH etching.

In the following, a brief overview on the four basic microfabrication steps will be given. More details can be found in textbooks and reference books on semiconductor processing [6–8, 10, 11].

### 1.1.1 Thin-film Deposition

The two most common thin-film deposition methods in microfabrication are chemical vapor deposition (CVD), performed at low pressure (LPCVD), atmospheric pressure (APCVD) or plasma-enhanced (PECVD), and physical vapor deposition (PVD), such as sputtering and evaporating. Typical CVD and PVD film thicknesses are in the range of tenths of nanometers up to a few micrometers. Other film deposition techniques include electroplating of metal films (e.g. the copper metallization in state-of-the-art CMOS processes) and spin- or spray-coating of polymeric films such as photoresist. Both processes can yield film thicknesses from less than 1 μm up to several hundreds of micrometers.

Dielectric layers, predominantly silicon dioxide, SiO$_2$, and silicon nitride, SiN$_x$, are used as insulating material, as mask material and for device passivation. Silicon dioxide is either thermally grown on top of a silicon surface (thermal oxide) at high temperatures (900–1200 °C) in an oxidation furnace or it is deposited in a CVD system (CVD oxide). CVD oxides can be deposited at temperatures between 300 and 900 °C, with the high-temperature depositions usually yielding better film properties. Low-temperature CVD oxide films are typically deposited in PECVD systems and high-temperature CVD oxide films in LPCVD equipment. Silicon nitride layers deposited in LPCVD furnaces are commonly used as masking...
material during local oxidation of silicon (LOCOS process), while PECVD silicon nitride films are used for e.g. device passivation.

Highly doped polycrystalline silicon (polysilicon) is used as gate material for metal oxide semiconductor field effect transistors (MOSFETs), as electrode and resistor materials, for piezoresistive sensing structures, as thermoelectric material, and for thermistors. Polysilicon microstructures released by sacrificial layer etching are also widely used in sensor applications (see Section 1.4). Polysilicon is usually deposited in an LPCVD furnace using silane (SiH₄) as gaseous precursor.

*Metal* layers are used, e.g., for electrical interconnects, as electrode material, for resistive temperature sensors (thermistors) or as mirror surfaces. Metals, which are widely used in the microelectronics industry, such as aluminum, titanium and tungsten, are routinely deposited by sputtering. Depending on the application, a large number of other metals, including gold, palladium, platinum, silver or alloys, can be deposited with PVD methods. A number of metals and metal compounds, such as Cu, WSi₂, TiSi₂, TiN and W, can be deposited by CVD. Metal CVD processes are less common, but can provide improved step coverage or local deposition of metals. Whereas aluminum has been the standard metallization in IC fabrication for many years, the state-of-the-art sub-0.25 μm CMOS technologies often feature copper as interconnect material, owing to its lower resistivity and higher electromigration resistance as compared with aluminum. An example is IBM’s interconnect metallizations based on the so-called damascene process [12], which employ copper films electroplated in a dielectric mold. After each metallization step, planarization is achieved with a chemical–mechanical polishing (CMP) step.

*Polymers* such as photoresist are commonly deposited by spin- or spray-coating. Polymers can be used as dielectric materials, passivation layers, and as chemically sensitive layers for chemical and biosensors ([13]; see also Chapter 7).

### 1.1.1.2 Patternning

Photolithography is the standard process to transfer a pattern, which has been designed with computer-aided-engineering (CAE) software packages, on to a certain material. The process sequence is illustrated in Fig. 1.4. A mask with the desired pattern is created. The mask is a glass plate with a patterned opaque layer (typically chromium) on the surface. Electron-beam lithography is used to write the mask pattern from the CAE data. In the photolithographic process, a photoresist layer (photostructurable polymer) is spin-coated on to the material to be patterned. Next, the photoresist layer is exposed to ultraviolet (UV) light through the mask. This step is done in a mask aligner, in which mask and wafer are aligned with each other before the subsequent exposure step is performed. Depending on the mask aligner generation, mask and substrate are brought in contact or close proximity (contact and proximity printing) or the image of the mask is projected (projection printing) on to the photoresist-coated substrate. Depending on whether positive or negative photoresist was used, the exposed or the unexposed photoresist areas, respectively, are removed during the resist development process.
The remaining photoresist acts as a protective mask during the subsequent etching process, which transfers the pattern onto the underlying material. Alternatively, the patterned photoresist can be used as a mask for a subsequent ion implantation. After the etching or ion implantation step, the remaining photoresist is removed, and the next layer can be deposited and patterned.

The so-called lift-off technique is used to structure a thin-film material, which would be difficult to etch. Here, the thin-film material is deposited on top of the patterned photoresist layer. In order to avoid a continuous film, the thickness of the deposited film must be less than the resist thickness. By removing the underneath photoresist, the thin-film material on top is also removed by ‘lifting it off’, leaving a structured thin film on the substrate.

Thick photostructurable polymer layers, such as SU-8 [14], can be used as a mold for electroplating metal structures. A thick polymer layer is deposited on top of a metallic seed layer and photostructured. During the subsequent electroplating process, the metal is only deposited in the areas where the seed layer is exposed to the plating solution, i.e. the polymer layer acts as a plating mold.

Recently, microcontact printing or soft lithography [15] has been introduced as an additional method for pattern transfer. A soft polymeric stamp is used to reproduce a desired pattern directly on a substrate. Routinely, feature sizes on the order of 1 μm can be achieved with this technique. The polymer stamp, often made from poly(dimethylsiloxane) (PDMS), is formed by a molding process using a master fabricated with conventional microfabrication techniques. After ‘inking’ the stamp with the material to be printed, the stamp is brought in contact with the substrate material, and the pattern of the stamp is reproduced. Surface proper-
ties of the substrate can therefore be modified to, e.g., locally promote or prevent molecule adhesion. Soft lithography has been specifically developed for biological applications such as patterning cells or proteins with the help of, e.g., self-assembled monolayers (SAMs) [15].

1.1.1.3 **Etching**

The two different categories of etching processes include wet etching using liquid chemicals and dry etching using gas-phase chemistry. Both methods can be either isotropic, i.e. provide the same etch rate in all directions, or anisotropic, i.e. provide different etch rates in different directions (see Fig. 1.5). The important criteria for selecting a particular etching process encompass the material etch rate, the selectivity for the material to be etched, and the isotropy/anisotropy of the etching process. An overview on various etching chemistries used in microfabrication can be found in [16].

Wet etching is usually isotropic with the important exception of anisotropic silicon wet etching in, e.g., alkaline solutions, such as potassium hydroxide (see Section 1.2). Moreover, wet etching typically provides a better etch selectivity for the material to be etched in comparison with neighboring other materials. An example includes wet etching of silicon dioxide using hydrofluoric acid-based chemistries. SiO₂ is isotropically etched in dilute hydrofluoric acid (HF–H₂O) or buffered oxide etch, BOE (HF–NH₄F). Typical etch rates for high-quality (thermally grown) silicon dioxide films are 0.1 μm/min in BOE.

Dry etching, on the other hand, is often anisotropic, resulting in a better pattern transfer, as mask underetching is avoided (see Fig. 1.5). Therefore, anisotropic dry etching processes, such as reactive ion etching (RIE), of thin-film materials are very common in the microelectronics industry. In an RIE system, reactive ions are generated in a plasma and are accelerated towards the surface to be etched, thus providing directional etching characteristics. Higher ion energies typically result in more anisotropic etching characteristics, but also in reduced etching selectivity.

![Fig. 1.5 Schematic of isotropic and anisotropic thin-film etching](image-url)
1.1.1.4 Doping

Doping is used to modify the electrical conductivity of semiconducting materials such as silicon or gallium arsenide. It is hence the key process step for fabricating semiconductor devices such as diodes and transistors. In the case of silicon, doping with phosphorus or arsenic yields n-type silicon, whereas p-type silicon results from boron doping. By varying the dopant concentration of n-type silicon from $10^{14}$ to $10^{20}$ cm$^{-3}$, the resistivity at room temperature can be tuned from approximately 40 to $7 \times 10^{-4} \Omega$ cm.

Dopant atoms are introduced by either ion implantation or diffusion from a gaseous, liquid or solid source. Ion implantation has become the key process to introduce precisely defined quantities of dopants in the microelectronics industry. The substrate material, i.e. a silicon wafer, is bombarded with accelerated ionized dopant atoms in an ion implanter. The result is approximately a Gaussian distribution of the dopant atoms in the substrate wafer with a mean penetration depth controlled by the acceleration voltage. A high-temperature diffusion process can then be used to additionally ‘drive-in’ the dopant until a desired doping profile has been achieved.

1.1.2 CMOS Process Sequence

To be able to integrate microelectromechanical devices with CMOS circuitry, the designer must have an excellent understanding of the underlying CMOS process sequence. The particular process flow is, of course, strongly dependent on the chosen CMOS technology and a detailed description of a CMOS technology goes way beyond the scope of this chapter. Nevertheless, we briefly summarize a typical CMOS process sequence in the following, highlighting the main process steps and their importance for co-integration of CMOS and MEMS. We thereby follow the CMOS process sequence described in detail in [6] (see schematic cross-section in Fig. 1.2), which is typical for a sub-μm technology with minimal feature sizes between 0.5 and 1 μm.

The starting wafer material is a lightly p-doped (100) wafer with a typical doping concentration of $N_A \approx 10^{15}$ cm$^{-3}$. The first step is the definition of the active areas by local oxidation of silicon (LOCOS), thus growing a thick (~ 0.5 μm) field oxide in the areas between the individual transistors. Next, the p-wells for the n-channel MOSFETs and the n-wells for the p-channel MOSFETs are implanted. A joint drive-in for both wells establishes the desired junction depth of 2–3 μm. Typical drive-in times are 4–6 h at 1000–1100°C. We will see later (Section 1.2) that the n-well diffused in the p-substrate can be used to define accurately the thickness of a silicon membrane. Such membranes are commonly released by anisotropic wet etching from the back of the wafer using an electrochemical etch-stop technique at the p–n junction between n-well and p-substrate [17, 18].

After n- and p-well formation, the MOSFET gate and channel regions are engineered. First, channel implants for the n- and the p-channel transistors are implanted to adjust their threshold voltages to the desired values. After removing the
implantation oxides in the active area, the gate oxide with a thickness \( \leq 10 \text{ nm} \) in modern CMOS processes is thermally grown in the active areas. Next, a 0.3–0.5 \( \mu \text{m} \) thick polysilicon layer for the gate electrodes is deposited across the wafer in an LPCVD furnace operating at about 600 °C and doped by ion implantation. Finally, the polysilicon layer is patterned to define the actual gate regions. In MEMS, the gate polysilicon can also be used for resistors, piezoresistors, thermopiles, electrodes and as structural materials. The last application often requires a high-temperature anneal of the polysilicon to reduce its residual stress to values acceptable for the microstructures. Such a high-temperature step can be critical at this stage in the CMOS process, as it might effect previous doping distributions and, hence, the CMOS device characteristics.

After gate formation, the source/drain regions are implanted. In typical sub-\( \mu \text{m} \) CMOS technologies, this is done using a LDD (lightly doped drain) process. It provides a gradient in the doping of the source/drain regions towards the channel region, reducing the peak value of the electric field close to a channel and, hence, increasing device reliability. First, phosphorus (or arsenic as alternative n-type dopant) is implanted in the source/drain of the NMOS transistors to form n\(^-\) regions, followed by a boron implantation of the source/drain of the PMOS transistors to form p\(^-\) regions. Next, a conformal spacer dielectric layer is deposited on the wafer and anisotropically etched back, leaving sidewall spacers along the edges of the polysilicon gates. After growing a thin screen oxide for the following implantation, the source/drain regions of the NMOS and PMOS transistors not protected by the sidewall spacer are successively implanted to form n\(^+\) and p\(^+\) regions, respectively. The final step of the source/drain engineering is a furnace anneal, typically at \( \sim 900 \text{ °C} \) for 30 min, to activate the implants, anneal implant damage and drive the junctions to their final depth. Alternatively to the furnace anneal, a much shorter rapid thermal anneal at higher temperatures can be performed (e.g. 1 min at 1000–1050 °C).

The fabrication of the active devices is now completed. Any subsequent high-temperature step (above 700–800 °C) necessary for the MEMS fabrication must be carefully qualified, as it might affect the doping distributions in the active devices, thus potentially changing the device characteristics.

In the back end of the process, the individual active devices are interconnected on the wafer to form circuits and pads for input/output connections off the chip are created. Although a large number of back-end metallization process flows with up to eight metallization levels exist, the exemplary CMOS process described in [6] uses three metallization levels with a local interconnect level based on titanium nitride and two wiring levels based on aluminum. The contacts to the source/drain regions and to the gate polysilicon are based on titanium silicide (TiSi\(_2\)). To this end, a thin titanium layer (50–100 nm) is sputtered on the wafer after removal of the implantation oxide. During an annealing step at about 600 °C in \( \text{N}_2 \), the titanium reacts with Si where they are in contact (e.g. source, drain and gate polysilicon) to form TiSi\(_2\) and with \( \text{N}_2 \) to form TiN elsewhere. The resulting TiN layer is patterned to create a local interconnect. Subsequently, the wafer surface is typically planarized using a PSG (phosphosilicate glass) or BPSG (borophosphosilicate glass) layer reflowed at 800–900 °C. Modern CMOS processes often
use chemical mechanical polishing (CMP) for interconnect and interconnect dielectric planarization. In the process described in [6], each of the following wiring levels uses CVD tungsten vias with a TiN adhesion/barrier layer and an aluminum (with a small percentage of Si and Cu) interconnect layer. Finally, the passivation layer is deposited (typically by PECVD) and patterned to form the pad openings necessary to contact the device from the outside. The composition of the passivation layer and especially its residual stress can be adapted according to the needs of the microstructures (see Section 1.3.1). After passivation, the wafers are annealed at low temperatures \((400–450°\text{C})\) for about 30 min in forming gas (10% \(\text{H}_2\) in \(\text{N}_2\)) to alloy the metal contacts.

The CMOS process presented in [6] and briefly described here requires 16 masks. A schematic device cross-section is shown in Fig. 1.2.

### 1.1.3 CMOS Materials for Micro- and Nanosystems

The particular CMOS technology chosen for the implementation of a micro- or nanoelectromechanical system (MEMS or NEMS) dictates the overall process sequence, the doping profiles and junction depths of doped silicon regions, and the material properties and thicknesses of the different thin-film layers. In general, only minimal adaptations can be made in order not to compromise the performance of the CMOS circuits (see Section 1.3). However, the different layers of the CMOS process can be used for the fabrication of the microstructures themselves. Tab. 1.1 summarizes the different doping regions and layers of a typical CMOS process and their use in MEMS and NEMS.

Two examples, namely a CMOS-based mass-sensitive chemical sensor [19–21] and a CMOS-based thermal imager [22, 23], will be discussed in the following. The mass-sensitive chemical sensor (see Fig. 1.6) is based on a 150 μm long and 140 μm wide cantilever beam consisting of the n-well of the CMOS process covered by the CMOS dielectrics [21]. Thus, the n-well and the CMOS dielectrics are used as structural materials. The cantilever is released after completion of the CMOS process by three post-CMOS micromachining steps: first, a silicon membrane is formed by anisotropic wet etching from the back of the wafer in combination with an electrochemical etch-stop technique at the p–n junction between p-substrate and n-well; thereafter, the cantilever is released by two reactive ion etching (RIE) steps. The two aluminum metallization layers are used to form a planar coil on top of the cantilever, enabling the generation of transverse vibrations in the presence of an external DC magnetic field parallel to the cantilever length. The transverse vibration are detected with stress-sensitive diode-connected PMOS transistors, arranged in a Wheatstone bridge configuration at the cantilever’s clamped edge. Alternatively, piezoresistors can be formed using either the p+-source/drain implantation of a PMOS transistor or the n+-doped gate polysilicon. The cantilever beam is coated with a chemically sensitive polymer layer. Upon absorption of analyte in the polymer layer, the cantilever’s mass increases and, hence, its resonance frequency decreases. The change of resonance frequency is
sensed by incorporating the resonant cantilever into an amplifying feedback loop [20, 21].

The thermal imager shown in Fig. 1.7 is based on a ~3×3 mm² membrane consisting of the dielectric layers of the CMOS process [22, 23]. The membrane is released by wet anisotropic silicon etching from the back of the wafer after completion of the regular CMOS process sequence. The thick field oxide is used as an intrinsic etch-stop layer. The CMOS dielectrics, i.e. the field oxide, the contact oxide, the intermetal oxide and the passivation, are used as structural materials. A grid of electroplated gold lines provides additional structural support to the membrane and divides it into 100 pixels. The gold lines are electroplated after the CMOS process in a standard process step normally preparing the wafers for TAB (tape automated bonding). Sandwiched in between the CMOS dielectrics on each pixel is a polysilicon/aluminum thermopile and a polysilicon heating resistor.

<table>
<thead>
<tr>
<th>CMOS layer/structure</th>
<th>Use in MEMS and NEMS</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-well/p-well</td>
<td>Structural material</td>
</tr>
<tr>
<td></td>
<td>Thermal conductor/mass</td>
</tr>
<tr>
<td>Source/drain implantation</td>
<td>Resistor</td>
</tr>
<tr>
<td></td>
<td>Piezoresistor</td>
</tr>
<tr>
<td></td>
<td>Thermopile</td>
</tr>
<tr>
<td></td>
<td>Electrode</td>
</tr>
<tr>
<td>Field oxide</td>
<td>Structural material</td>
</tr>
<tr>
<td></td>
<td>Thermal insulator</td>
</tr>
<tr>
<td></td>
<td>Sacrificial material</td>
</tr>
<tr>
<td>Gate polysilicon (and optional 2nd polysilicon)</td>
<td>Resistor</td>
</tr>
<tr>
<td></td>
<td>Piezoresistor</td>
</tr>
<tr>
<td></td>
<td>Thermopile</td>
</tr>
<tr>
<td></td>
<td>Electrode</td>
</tr>
<tr>
<td></td>
<td>Structural material</td>
</tr>
<tr>
<td></td>
<td>Sacrificial material</td>
</tr>
<tr>
<td>Contact and intermetal oxides</td>
<td>Structural material</td>
</tr>
<tr>
<td></td>
<td>Thermal insulator</td>
</tr>
<tr>
<td></td>
<td>Sacrificial material</td>
</tr>
<tr>
<td>Metallization (and optional multi-level metallizations)</td>
<td>Conductor</td>
</tr>
<tr>
<td></td>
<td>Mirror</td>
</tr>
<tr>
<td></td>
<td>Thermal conductor</td>
</tr>
<tr>
<td></td>
<td>Electrode</td>
</tr>
<tr>
<td></td>
<td>Structural material</td>
</tr>
<tr>
<td></td>
<td>Sacrificial material</td>
</tr>
<tr>
<td>Passivation</td>
<td>Structural material</td>
</tr>
<tr>
<td></td>
<td>Thermal insulator</td>
</tr>
<tr>
<td></td>
<td>Stress compensation</td>
</tr>
<tr>
<td></td>
<td>Infrared radiation absorber</td>
</tr>
</tbody>
</table>

Tab. 1.1 Common CMOS materials and their use in micro- and nanoelectromechanical systems (MEMS and NEMS)
incoming infrared (IR) radiation is absorbed in the CMOS thin-film sandwich

(a)

(b)

Fig. 1.6 (a) Photograph and (b) schematic cross-section of a cantilever-based mass-sensitive gas sensor. The cantilever structure features an integrated planar coil for electromagnetic excitation of transverse vibrations in the presence of a DC magnetic field and PMOS transistors in a Wheatstone bridge arrangement for deflection detection [21]. Photograph courtesy of C. Vancura, ETH Zurich, Switzerland.

(a)

(b)

Fig. 1.7 (a) Photograph and (b) schematic cross-section of a CMOS-based infrared radiation sensor array. The sensor array is located on a micromachined membrane consisting of the dielectric layers of the CMOS process. An electroplated gold grid divides the membrane in a 10×10 array of pixels, each incorporating a thermopile with 16 polysilicon/aluminum thermocouples for temperature sensing. On-chip circuitry includes a multiplexer and a low-noise chopper amplifier [22, 23]. Photograph courtesy of Prof. H. Baltes, ETH Zurich, Switzerland.
A number of microsensors can be completely formed within the regular CMOS process sequence, typically not requiring any additional process steps. Well-known examples include temperature sensors [24, 25], magnetic field sensors (especially Hall sensors) [26] and CMOS imagers [27, 28]. An additional subset of CMOS-based microsystems only requires either the modification of a CMOS layer or the deposition and patterning of additional layers, but no micromachining steps. A few selected examples will be given in the following.

Chemical sensors and biosensors relying on an electrochemical sensing principle require an electrode in contact with the sample to be sensed. Examples include amperometric sensors, palladium-gate FET and ISFET (ion-sensitive field-effect transistor) structures, and also chemoresistors and chemocapacitors. A number of these electrochemical sensors have been co-integrated with CMOS circuitry (see Chapter 7), typically requiring deposition and patterning of special metal electrodes and/or passivation layers in addition to the regular CMOS process sequence.

Examples are the CMOS-based biosensor arrays developed recently for DNA analysis [29, 30] and recording of neural activity [31]. The sensor arrays are based on a standard 0.5 μm CMOS process optimized for analog applications [30]. After deposition and patterning of the second aluminum layer, a silicon dioxide layer is deposited, followed by a planarization step using CMP and the deposition of a silicon nitride passivation. The actual sensor electrodes are fabricated on top of the nitride passivation. First, vias are etched to enable contacts to the aluminum metallization and are filled with a Ti/TiN barrier layer and CVD tungsten [30]. In the case of the DNA arrays, the final interdigitated gold electrodes are deposited by evaporation of a Ti/Pt/Au electrode stack, which is patterned using a lift-off technique ([30]; see Fig. 1.8). In the case of the sensor arrays for neural activity recording, the sensor electrodes and the contact pads are defined by depositing and lift-off patterning of a Ti/Pt layer. Subsequently, a dielectric layer sandwich consisting of different TiO₂ and ZrO₂ layers is deposited and opened at the location of the bond pads. Neural activity is recorded capacitively with the sensor electrodes covered by the protective dielectric layer sandwich. Finally, a gold layer is deposited on the Pt pads and structured using a lift-off process [31].

Researchers at ETH Zurich have recently reported a CMOS-integrated microelectrode array for stimulation and recording of natural neural networks [32]. The microsystem is fabricated using a 0.6 μm CMOS process in combination with a two-mask post-CMOS process sequence to deposit and pattern biocompatible platinum electrodes. The post-CMOS process sequence starts with the deposition and patterning of 50 nm TiW and 270 nm Pt. The metal layer sandwich is structured